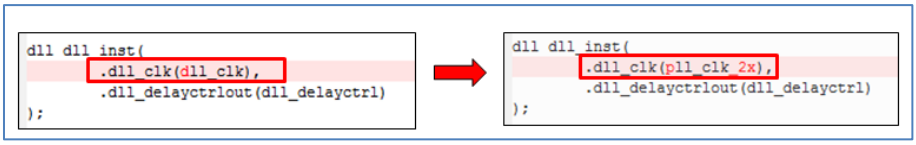
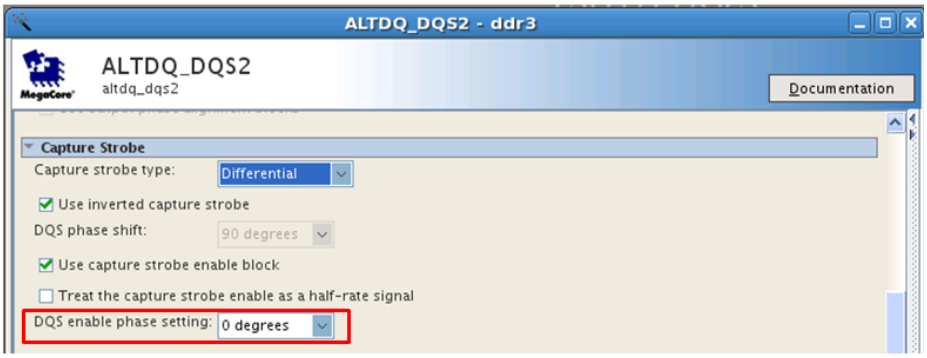
The following extra steps are required for customers using strobe-based ALTDQ_DQS2 IP targeting Stratix V, Arria V and Cyclone V.

1. Refer to Appendix and determines which solution is required in customer designs.
2. i) Solution A: Change the DLL input frequency
    a. Open Altera PLL megafunction and create an extra output clock that is used to clock DLL. Set the **Desired Frequency** to a frequency value which doubles your memory frequency
    b. In your top level file, search for DLL instance. Manually connect the generated output clock to dll_clk.



ii) Solution B: For bypass DQS delay chain
    a. Set **DQS enable phase setting** to **0 degrees** in **ALTDQ_DQS2** IP



Appendix:

Cyclone V

Frequency/ Memory	DDR3/DDR3L/DDR2	LPDDR2
f>= 450 MHz	No change	No change
400 MHz<f<450MHz	Bypass DQS Delay Chain	Bypass DQS Delay Chain
250 MHz <= f <= 400 MHz	Change the DLL input frequency	Bypass DQS Delay Chain
f<250 MHz	Bypass DQS Delay Chain	Bypass DQS Delay Chain

Arria V

Frequency/ Memory	DDR3/DDR3L/DDR2	LPDDR2
f>= 450 MHz	No change	No change
250 MHz <= f < 450 MHz	Change the DLL input frequency	Bypass DQS Delay Chain
f<250 MHz	Bypass DQS Delay Chain	Bypass DQS Delay Chain

Stratix V (-1/-2 speedgrade)

Frequency/ Memory	DDR3/DDR3L/DDR2
f>= 480 MHz	No change
240 MHz <= f < 479 MHz	Change the DLL input frequency
f<240 MHz	Bypass DQS Delay Chain

Stratix V (-3/-4 speedgrade)

Frequency/ Memory	DDR3/DDR3L/DDR2
f>= 445 MHz	No change
223 MHz <= f < 444 MHz	Change the DLL input frequency
f<223 MHz	Bypass DQS Delay Chain