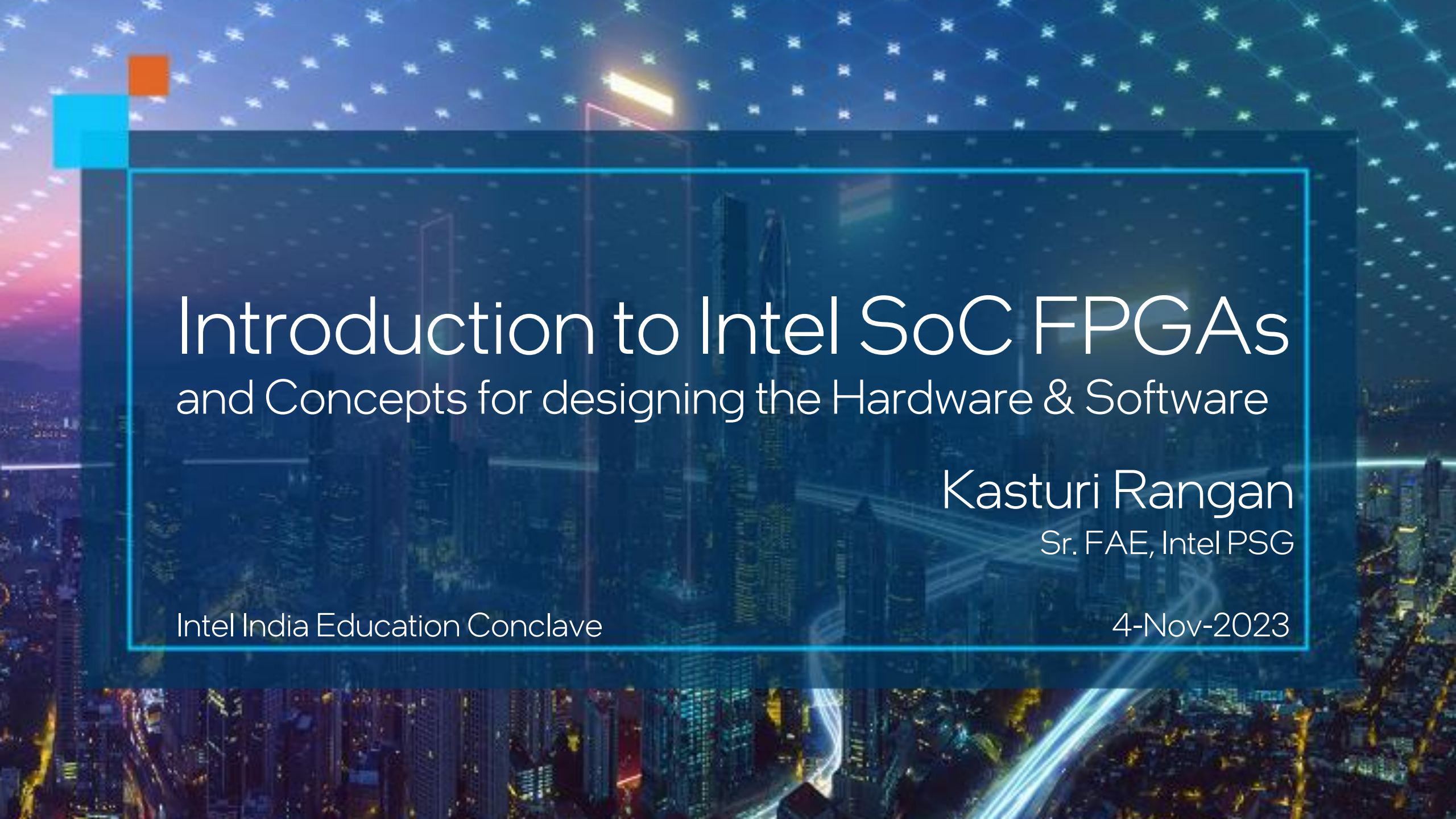


# Introduction to Intel SoC FPGAs

## and Concepts for designing the Hardware & Software

Kasturi Rangan

Sr. FAE, Intel PSG

Intel India Education Conclave

4-Nov-2023

# Agenda

- Why SoC FPGAs?
- Intel SoC FPGAs HPS architectures
- Differences in HPS of various SoC FPGAs
- Intel SoC FPGA Device Families & variants
- Development tool flow & Ecosystem (h/w & s/w)
- Development Kits & SoM solutions
- Q&A

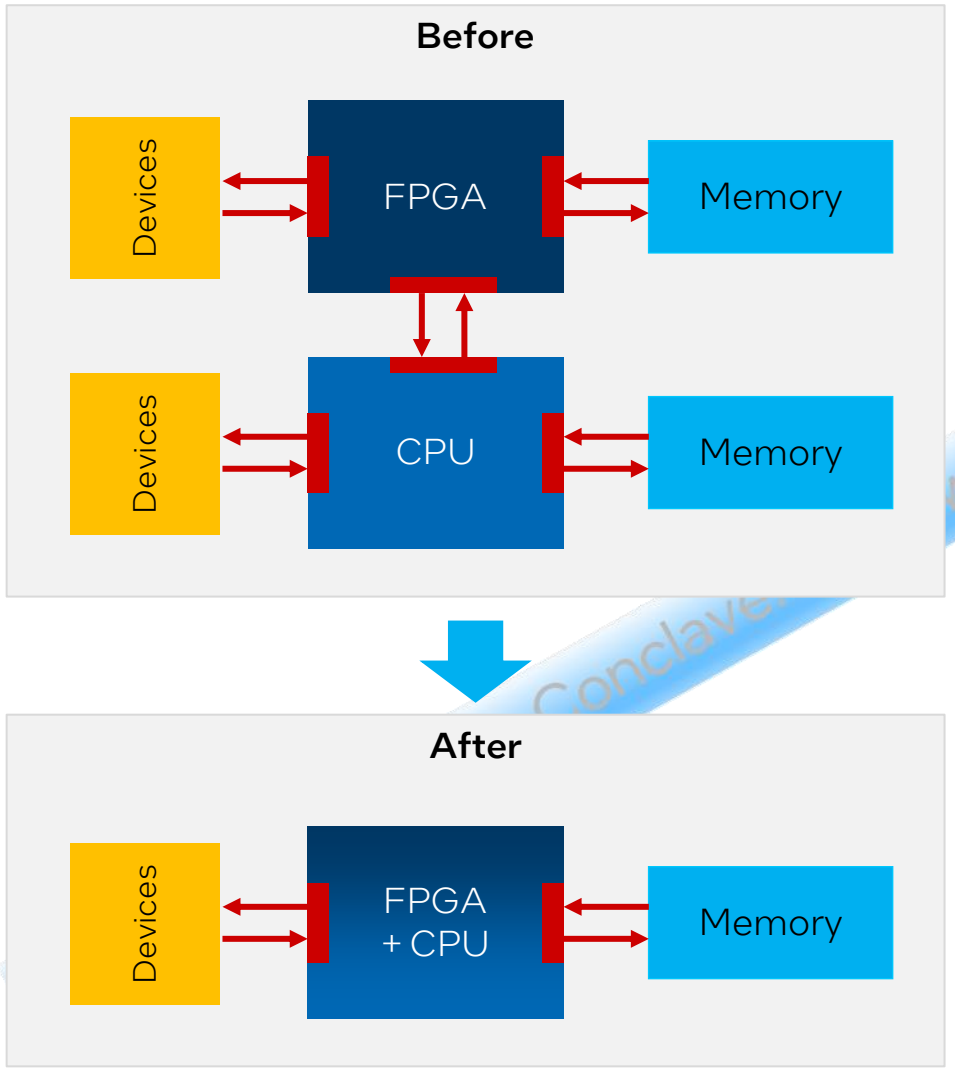


* Bonus section – HPS Architecture Deep Dive & Booting concepts of a popular SoC FPGA

# Why SoC FPGAs?

## what Intel has to offer as SoC FPGAs

# The Promise of FPGA or CPU Integration




## Increased system performance

- On-chip FPGA or CPU interconnect

## Reduced power consumption

- On-chip FPGA or CPU interconnect
- Single memory shared by FPGA and CPU

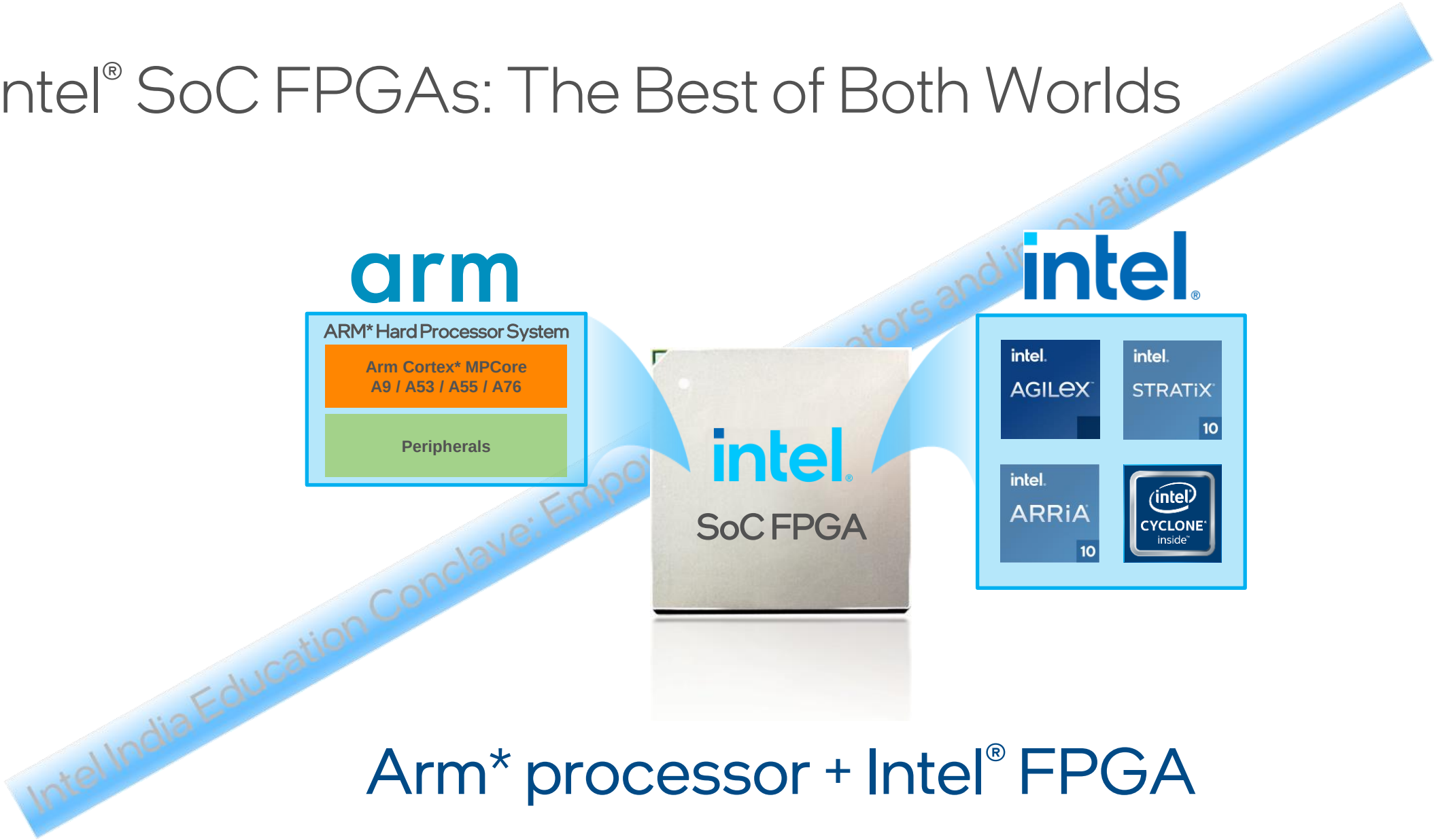
## Reduced board size

- Fewer components:
  FPGA or CPU, memory, power supply, passives

## Reduced system costs

- Fewer components > lower BOM cost
- Reduced PCB routing > lower PCB costs

# Intel® SoC FPGAs: The Best of Both Worlds

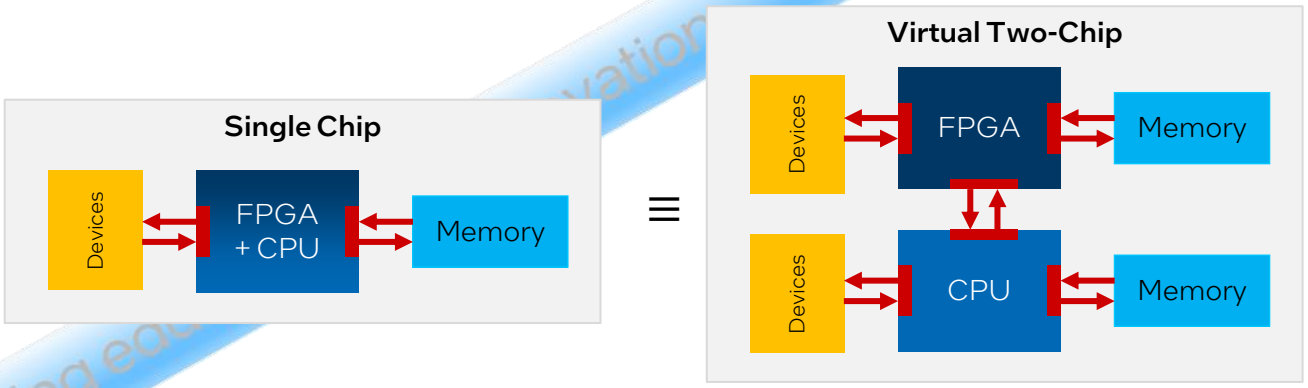



## Arm* processor + Intel® FPGA

# Architecture Matters

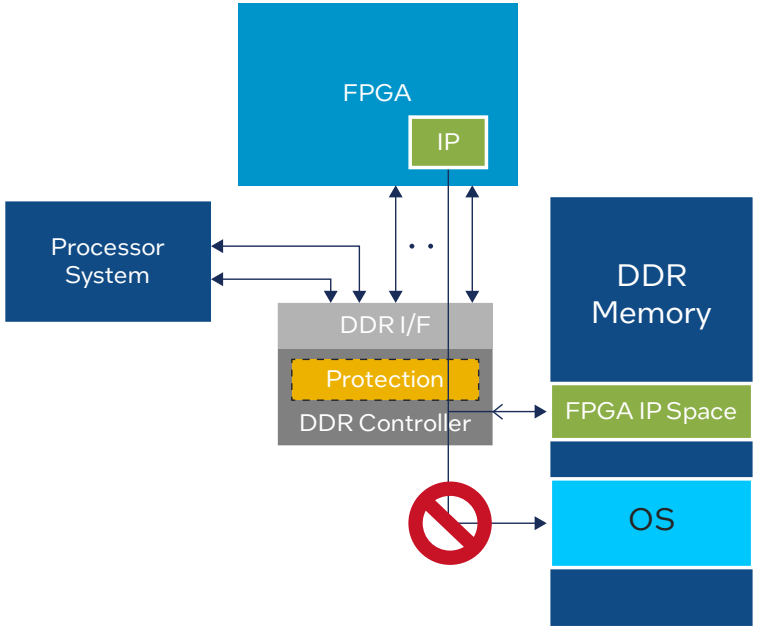
## Preserve Independence (virtual 2-chip operation)

- Processor boot or FPGA configuration
- FPGA operates even with CPU reset
- Independent FPGA or CPU memories



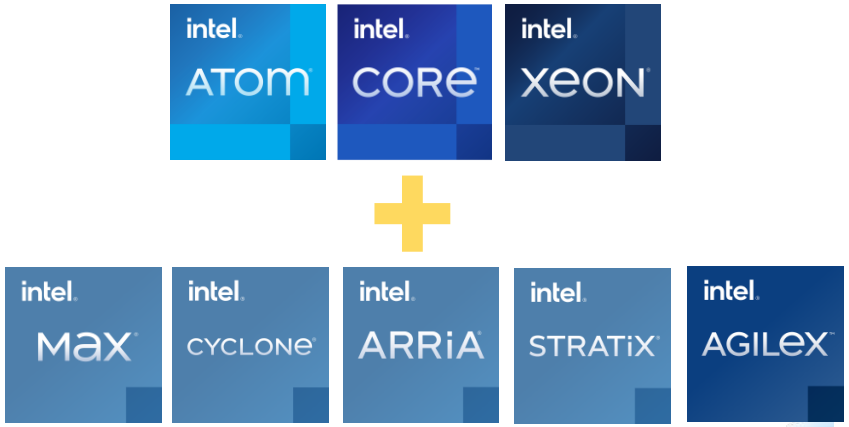

## Protect Memory When Shared

- CPU memory protected from FPGA IP



# Industry's Broadest Customizable Processor Portfolio

## Discrete




- High performance/watt
- Co-processing & acceleration
- I/O Expansion, features

## Integrated Arm or IA


SoC FPGA SoC FPGA SoC FPGA SoC FPGA

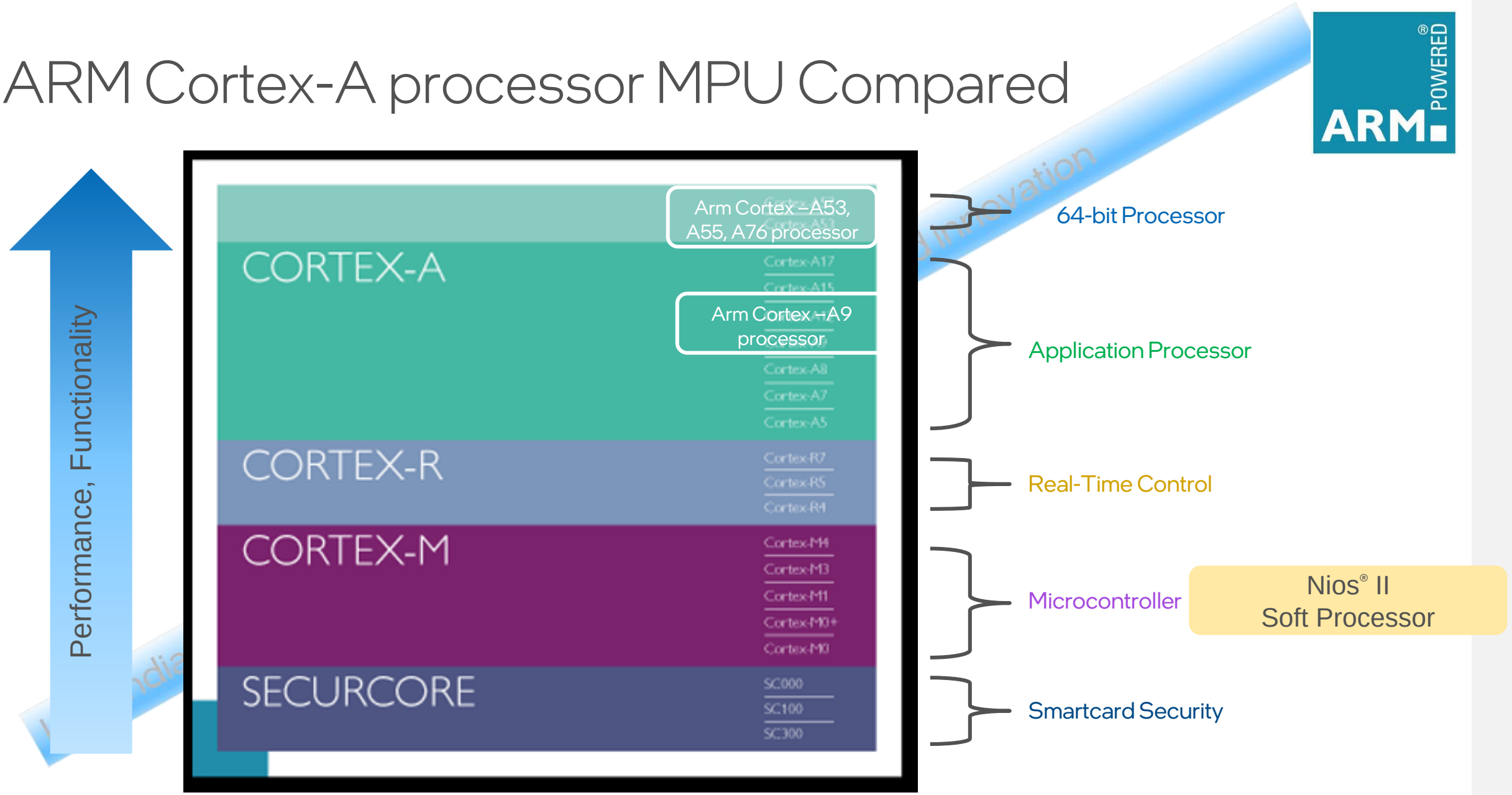
- Size/space constraints
- Low latency high throughput interconnect
- Robust security

## Soft CPU


- One or many CPU cores
- Works with any FPGA or SoC FPGA
- Configurable: real time MCU, Linux MPU

**High Performance / Watt** **Integration** **Ultimate Flexibility**

# ARM Cortex-A processor MPU Compared



# Cloud to Edge is Powered by Intel® Technology

Cloud Data Center

Things & Devices

## Examples

### Discrete

intel Atom | intel Core | intel Xeon + intel Max | intel Cyclone | intel ARRIA | intel STRATIX | intel AGILEX

| | | | |
|---|---|---|---|
| Acceleration | Network Video Recorders | Cloud Gaming | Smart Cars |
| Cloud Computing | Video Transcode | Car Infotainment | Smart Cameras |
| Artificial Intelligence | Analytics | End to end Media Processing | L3/4 Autonomous Automated Driving |

### Integrated

intel Cyclone ARM SoC FPGA | intel ARRIA ARM SoC FPGA | intel STRATIX ARM SoC FPGA | intel AGILEX ARM SoC FPGA

| | | | |
|---|---|---|---|
| Acceleration | Line Cards, Bridging & Aggregation | Remote Radio Heads/Mobile Backhaul | Broadcast Studio Distribution |
| Flash Cache | Muxponders/Transponders, ODU | L2 ADAS (Driver Assist) | Headend Encoder |
| Diagnostic Imaging | Packet Processing | Radar/Electronic Warfare/Secure comms | ProAV/Videoconferencing |

### Soft CPU

Nios® II Nios® V FPGA

| | | |
|---|---|---|
| Solar Inverter | PLC | Video Surveillance |
| Smart Grid | Motor Control | Machine Vision |

# Hard Processor System Architectures

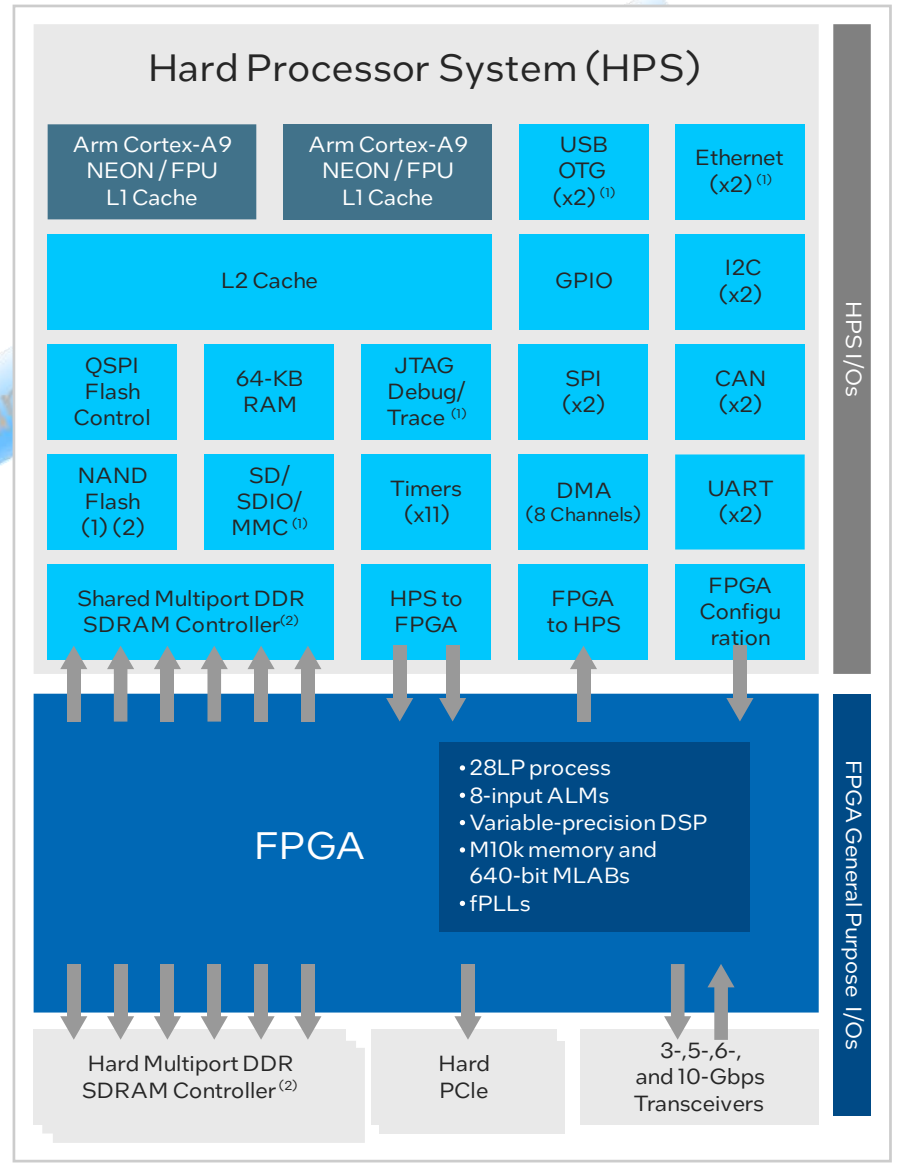
## of Intel SoC FPGAs

# Hard Processor System Architecture-1

## Cyclone V SoC / Arria V SoC / Arria 10 SoC

- Processor
  - Dual-core Arm Cortex-A9 MPCore processor
  - Up to 5,250 MIPS (1,050 MHz per core maximum)
  - NEON coprocessor with double-precision FPU
  - 32-KB/32-KB L1 caches per core
  - 512-KB shared L2 cache
- Multiport SDRAM controller
  - DDR3, DDR3L, DDR2, LPDDR2
  - Integrated ECC support
- High-bandwidth on-chip interfaces
  - HPS-to-FPGA
  - FPGA-to-HPS
  - FPGA-to-SDRAM interface
- Cost- and power-optimized FPGA fabric
  - Optimized power transceivers
  - DSP Blocks: Up to 1,600 GMACS, 300 GFLOPS
  - Up to 25Mb on-chip RAM
  - PCIe and memory controllers



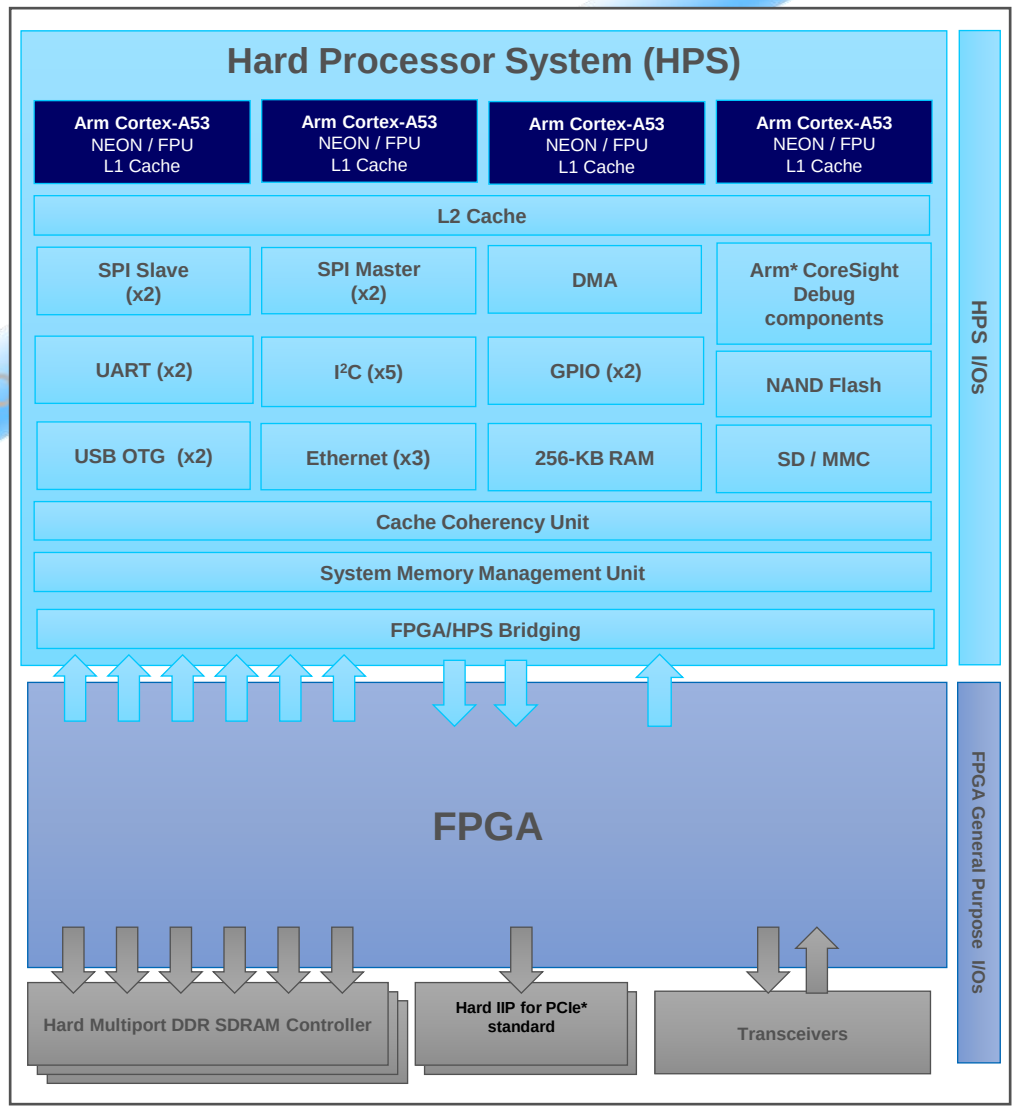



Notes:
(1) Integrated direct memory access (DMA)
(2) Integrated ECC

# Hard Processor System Architecture-2

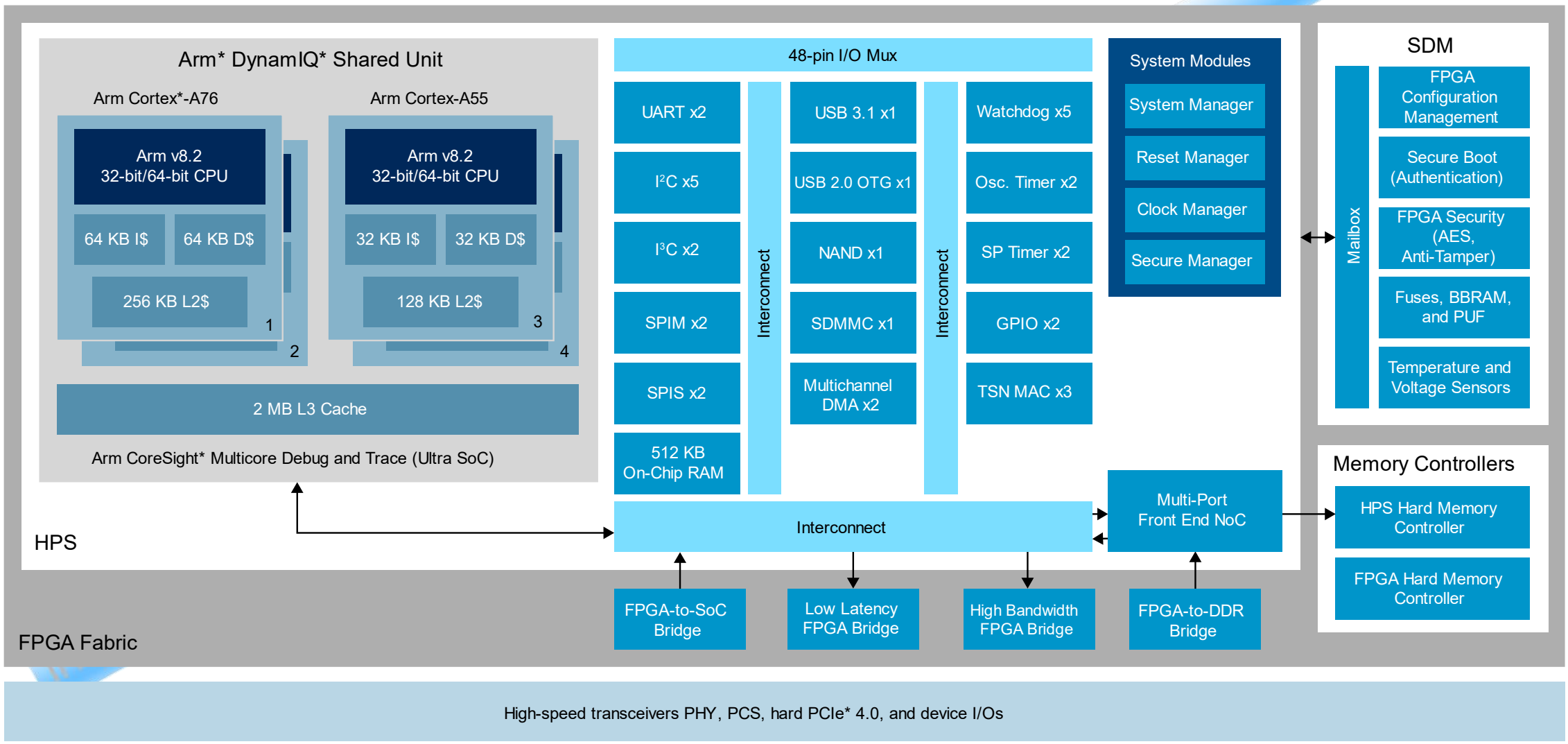
## Stratix 10 SoC / Agilex-7 SoC

- Processor
  - Quad-core Arm* Cortex*-A53 MPCore*
  - 64-bit ARMv8 architecture
- FPGA Features
  - Hyperflex Architecture
  - 8 input Adaptive Logic Modules (ALM)
  - Variable precision DSP blocks
  - Hard IP for PCI Express*
  - High-Bandwidth on-chip interfaces



# Hard Processor System Architecture-3

## Agilex-5 SoC



# Hard Processor System Differences

## in Intel SoC FPGAs

# Hard Processor Subsystem Differences

| Feature | Cyclone®V/ Arria® V | Intel® Arria® 10 | Intel® Stratix® 10/ Intel Agilex® 7 | Intel Agilex® 5 |
|---|---|---|---|---|
| Micro Processor Unit (MPU) | Single/Dual Cortex-A9 | Dual Cortex-A9 | Quad Cortex-A53 | Dual Cortex-A76 and Dual Cortex-A55 with DynamIQ Shared Unit |
| Cache Coherency | Accelerator Coherency Port (ACP) | ACP | Cache Coherency Unit (CCU) | CCU, New/Upgraded |
| Generic Interrupt Controller (GIC) | Yes | Yes | Yes | Yes, New/Upgraded |
| System Memory Management Unit | No | No | Yes | Yes, New/Upgraded |
| On-Chip RAM | 64 KB | 256 KB | 256 KB | 512 KB |
| Ethernet Media Access Controller | 2 | 3 | 3 | 3, New/Upgraded |
| DMA Controller | 1 | 1 | 1 | 2, New/Upgraded |
| NAND Controller | Yes | Yes | Yes | Yes, New/Upgraded |
| SD/eMMC Host | Yes | Yes | Yes | Yes, New/Upgraded |
| Combo DLL PHY | No | No | No | Yes, New/Upgraded |

# Contd.. Hard Processor Subsystem Differences

| Feature | Cyclone® V/ Arria® V | Intel® Arria 10 | Intel® Stratix® 10/ Intel Agilex® 7 | Intel Agilex® 5 |
|---|---|---|---|---|
| Quad SPI Controller | Yes (inside HPS) | Yes (inside HPS) | No (uses SDM) | No (uses SDM) |
| USB 3.1 Gen 1 Controller | No | No | No | 1, New/Upgraded |
| USB 2.0 OTG Controller | 2 | 2 | 2 | 1 |
| I3C Controller | No | No | No | 2, New/Upgraded |
| I2C Controller | 4 | 5 | 5 | 5 |
| SPI Controller | 2 hosts and 2 agents | 2 hosts and 2 agents | 2 hosts and 2 agents | 2 hosts and 2 agents |
| Timers | 4 | 4 | 4 | 4 |
| Watchdog Timers | 2 | 2 | 4 | 5 |
| UART Controller | 2 | 2 | 2 | 2 |
| CAN | 2 | No | No | No |
| GPIO | Yes | Yes | Yes | Yes |

# Contd.. Hard Processor Subsystem Differences

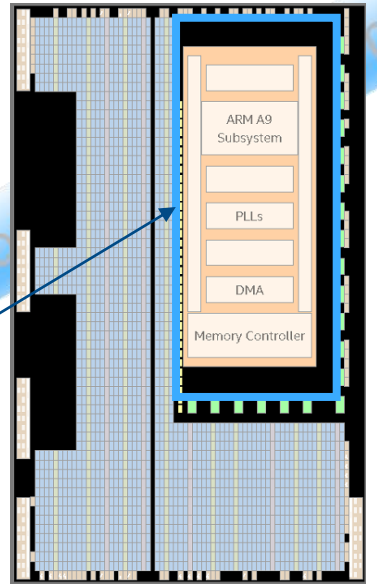
| Feature | Cyclone® V/ Arria® V | Intel® Arria® 10 | Intel ® Stratix® 10/ Intel Agilex® 7 | Intel Agilex® 5 |
|---|---|---|---|---|
| HPS I/O Pinmux | CV: 67 dedicated I/O with loaner<br>AV: 94 dedicated I/O with loaner | 17 dedicated I/O<br>48 shared I/O | 48 dedicated I/O | 48 dedicated I/O |
| System Manager | Yes | Yes | Yes | Yes, New/Upgraded |
| Clock Manager | Yes | Yes | Yes | Yes, New/Upgraded |
| Reset Manager | Yes | Yes | Yes | Yes, New/Upgraded |
| FPGA Manager | Yes | Yes | No (uses SDM) | No (uses SDM) |
| Scan Manager | Yes | No | No | No |
| Security Manager | No | Yes | No (uses SDM) | No (uses SDM) |
| HPS-FPGA Bridges | Yes | Yes | Yes | Yes, New/Upgraded |
| SDRAM Controller | Inside HPS | Outside HPS | Outside HPS | Outside HPS, New/Upgraded |

# Lastly.. Hard Processor Subsystem Differences

| Feature | Cyclone® V/ Arria® V | Intel ® Arria® 10 | Intel ® Stratix® 10/ Intel Agilex® 7 | Intel Agilex® 5 |
|---|---|---|---|---|
| System Interconnect | Yes | Yes | Yes | Yes, New/Upgraded |
| Error Checking and Correction Controller | No | Yes | Yes | Yes, New/Upgraded |
| CoreSight Debug and Trace | Yes | Yes | Yes | Yes, New/Upgraded |
| Secure Device Manager Interface | No | No | Yes | Yes |
| Booting and Configuration | 3 options:<br>1. HPS boot and FPGA configuration occur separately<br>2. FPGA configuration first<br>3. HPS boot first | 3 options:<br>1. HPS boot and FPGA configuration occur separately<br>2. FPGA configuration first<br>3. HPS boot first | 2 options:<br>1. FPGA configuration first<br>2. HPS boot first | 2 options:<br>1. FPGA configuration first<br>2. HPS boot first |

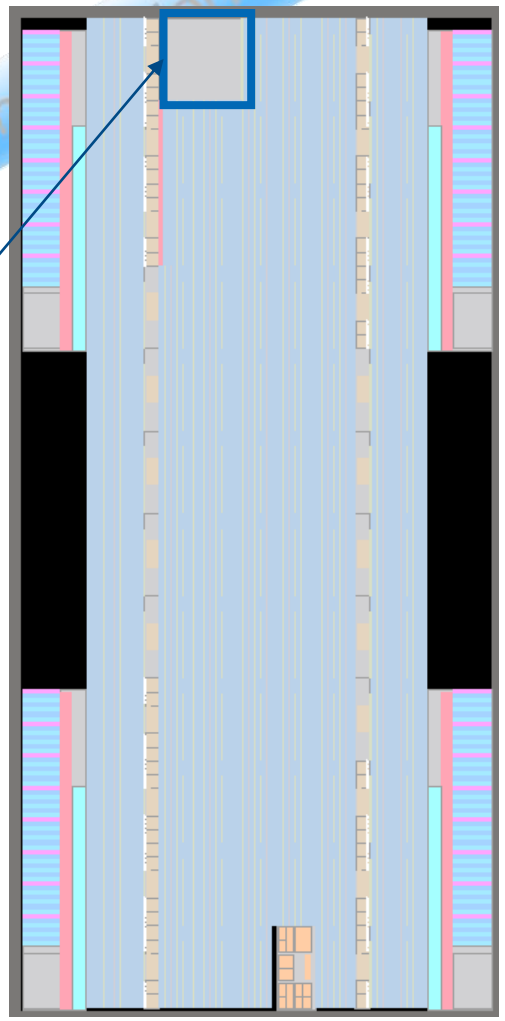
# HPS Proportional View (from Chip Planner)

The HPS is a dedicated physical portion of any Intel SoC FPGA.




HPS in Cyclone® V SoC (25 KLE)

HPS in Intel® Stratix® 10 SoC (2.75 MLE)



# Intel SoC FPGA Device Family

54+ device variants

# Intel SoC FPGA Device Family with Dual Cortex A9

| Family | HPS Max. Freq. | KLE | Block Memory Bits (Mb) | Var. Prec. Multiplier Blocks | Max. FPGA User I/Os | HPS Dedicated I/Os | Max. Transceivers (GP) | Per-Transceiver Max. Data Rate (Gbps) | SoC Hard Memory Controller | FPGA Hard Memory Controllers | Hard PCIe |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Cyclone V SoC | 925 MHz | 25 | 1.4 | 36 | 145 | 181 | 6 | 3 | 1 | 1 | 2 ea, Gen1 |
| | | 40 | 2.7 | 58 | 145 | 181 | 6 | 3 | 1 | 1 | 2 ea, Gen1 |
| | | 85 | 4.0 | 87 | 288 | 181 | 9 | 6.144 | 1 | 1 | 2 ea, Gen2 |
| | | 110 | 5.6 | 112 | 288 | 181 | 9 | 6.144 | 1 | 1 | 2 ea, Gen2 |
| Arria V SoC | 1.05 GHz | 350 | 17.3 | 809 | 528 | 208 | 30 / 16 | 6 / 10 | 1 | 3 | 2 ea, Gen2 |
| | | 460 | 22.8 | 1,068 | 528 | 208 | 30 / 16 | 6 / 10 | 1 | 3 | 2 ea, Gen2 |
| Arria 10 SoC | 1.50 GHz | 160 | 9 | 156 | 288 | 17 | 12 | 17.4 | 1 | 4 | 1 ea, Gen3 |
| | | 220 | 11 | 191 | 288 | 17 | 12 | 17.4 | 1 | 4 | 1 ea, Gen3 |
| | | 270 | 15 | 830 | 384 | 17 | 24 | 17.4 | 1 | 4 | 2 ea, Gen3 |
| | | 320 | 17 | 985 | 384 | 17 | 24 | 17.4 | 1 | 4 | 2 ea, Gen3 |
| | | 480 | 28 | 1,368 | 492 | 17 | 36 | 17.4 | 1 | 4 | 2 ea, Gen3 |
| | | 570 | 35 | 1,523 | 588 | 17 | 48 | 17.4 | 1 | 4 | 2 ea, Gen3 |
| | | 660 | 42 | 1,688 | 588 | 17 | 48 | 17.4 | 1 | 4 | 2 ea, Gen3 |

* 13 device variants

# Intel SoC FPGA Device Family with Quad Cortex A53

## Intel Stratix 10 SX SoC Features

| | Product Line | SX 400 | SX 650 | SX 850 | SX 1100 | SX 1650 | SX 2100 | SX 2500 | SX 2800 |
|---|---|---|---|---|---|---|---|---|---|
| Resources | Logic elements (LEs)[1] | 378,000 | 612,000 | 841,000 | 1,325,000 | 1,624,000 | 2,005,000 | 2,422,000 | 2,753,000 |
| | Adaptive logic modules (ALMs) | 128,160 | 207,360 | 284,960 | 449,280 | 550,540 | 679,680 | 821,150 | 933,120 |
| | ALM registers | 512,640 | 829,440 | 1,139,840 | 1,797,120 | 2,202,160 | 2,718,720 | 3,284,600 | 3,732,480 |
| | Hyper-Registers from Intel Hyperflex FPGA Architecture | Millions of Hyper-Registers distributed throughout the monolithic FPGA fabric | | | | | | | |
| | Programmable clock trees synthesizable | Hundreds of synthesizable clock trees | | | | | | | |
| | M20K memory blocks | 1,537 | 2,489 | 3,477 | 5,461 | 5,851 | 6,501 | 9,963 | 11,721 |
| | M20K memory size (Mb) | 30 | 49 | 68 | 107 | 114 | 127 | 195 | 229 |
| | MLAB memory size (Mb) | 2 | 3 | 4 | 7 | 8 | 11 | 13 | 15 |
| | Variable-precision digital signal processing (DSP) blocks | 648 | 1,152 | 2,016 | 2,592 | 3,145 | 3,744 | 5,011 | 5,760 |
| | 18 x 19 multipliers | 1,296 | 2,304 | 4,032 | 5,184 | 6,290 | 7,488 | 10,022 | 11,520 |
| | Peak fixed-point performance (TMACS)[2] | 2.6 | 4.6 | 8.1 | 10.4 | 12.6 | 15.0 | 20.0 | 23.0 |
| | Peak floating-point performance (TFLOPS)[3] | 1.0 | 1.8 | 3.2 | 4.1 | 5.0 | 6.0 | 8.0 | 9.2 |
| I/O and Architectural Features | Secure device manager | AES-256/SHA-256 bitstream encryption/authentication, physically unclonable function (PUF), ECDSA 256/384 boot code authentication, side-channel attack protection | | | | | | | |
| | Hard processor system[4] | Quad-core 64-bit Arm Cortex-A53 up to 1.5 GHz with 32KB I/D cache, NEON coprocessor, 1 MB L2 cache, direct memory access (DMA), system memory management unit, cache coherency unit, hard memory controllers, USB 2.0 x2, 1G EMAC x3, UART x2, SPI x4, I2C x5, general purpose timers x7, watchdog timer x4 | | | | | | | |
| | Maximum user I/O pins | 374 | 392 | 688 | 688 | 704 | 704 | 1160 | 1160 |
| | Maximum LVDS pairs 1.6 Gbps (RX or TX) | 120 | 192 | 336 | 336 | 336 | 336 | 576 | 576 |
| | Total full duplex transceiver count | 24 | 24 | 48 | 48 | 96 | 96 | 96 | 96 |
| | GXT full duplex transceiver count (up to 28.3 Gbps) | 16 | 16 | 32 | 32 | 64 | 64 | 64 | 64 |
| | GX full duplex transceiver count (up to 17.4 Gbps) | 8 | 8 | 16 | 16 | 32 | 32 | 32 | 32 |
| | PCI Express hard intellectual property (IP) blocks (3.0 x16) | 1 | 1 | 2 | 2 | 4 | 4 | 4 | 4 |
| | Memory devices supported | DDR4, DDR3, DDR2, DDR, QDR II, QDR II+, RLDRAM II, RLDRAM 3, HMC, MoSys | | | | | | | |

* 8 device variants

# Intel SoC FPGA Device Family with Quad Cortex A53

## Intel Agilex 7 FPGA and SoC F-Series Features

View device ordering codes on page 55.

| Product Line | | AGF 006 | AGF 008 | AGF 012 | AGF 014 | AGF 019 | AGF 022 | AGF 023 | AGF 027 |
|---|---|---|---|---|---|---|---|---|---|
| Resources | Logic elements (LEs) | 573,480 | 764,640 | 1,178,525 | 1,437,240 | 1,918,975 | 2,208,075 | 2,308,080 | 2,692,760 |
| | Adaptive logic modules (ALMs) | 194,400 | 259,200 | 399,500 | 487,200 | 650,500 | 748,500 | 782,400 | 912,800 |
| | ALM registers | 777,600 | 1,036,800 | 1,598,000 | 1,948,800 | 2,602,000 | 2,994,000 | 3,129,600 | 3,651,200 |
| | High-performance crypto blocks | 0 | 0 | 0 | 0 | 2 | 0 | 2 | 0 |
| | eSRAM memory blocks | 0 | 0 | 2 | 2 | 1 | 0 | 1 | 0 |
| | eSRAM memory size (Mb) | 0 | 0 | 36 | 36 | 18 | 0 | 18 | 0 |
| | M20K memory blocks | 2,844 | 3,792 | 5,900 | 7,110 | 8,500 | 10,900 | 10,464 | 13,272 |
| | M20K memory size (Mb) | 56 | 74 | 115 | 139 | 166 | 212 | 204 | 259 |
| | MLAB memory count | 9,720 | 12,960 | 19,975 | 24,360 | 32,525 | 37,425 | 39,120 | 45,640 |
| | MLAB memory size (Mb) | 6 | 8 | 12 | 15 | 20 | 23 | 24 | 28 |
| | I/O PLL | 12 | 12 | 16 | 16 | 10 | 16 | 10 | 16 |
| | Variable-precision digital signal processing (DSP) blocks | 1,640 | 2,296 | 3,743 | 4,510 | 1,354 | 6,250 | 1,640 | 8,528 |
| | 18 x 19 multipliers | 3,280 | 4,592 | 7,486 | 9,020 | 2,708 | 12,500 | 3,280 | 17,056 |
| | Single-precision or half-precision tera floating point operations per second (TFLOPS) | 2.5 / 5.0 | 3.5 / 6.9 | 6.0 / 12.0 | 6.8 / 13.6 | 2.0 / 4.0 | 9.4 / 18.8 | 2.5 / 5.0 | 12.8 / 25.6 |
| | Maximum EMIF x72 | 2 | 2 | 4 | 4 | 2 | 4 | 2 | 4 |
| Maximum Available Device Resources | Maximum differential (RX or TX) pairs | 192 | 288 | 384 | 384 | 240 | 384 | 240 | 384 |
| | Maximum AIB interfaces | 2 | 2 | 2 | 2 | 4 | 4 | 4 | 4 |
| | Memory devices supported | DDR4, QDR IV | | | | | | | |
| | Secure Device Manager (SDM) | Provides SHA-384 bitstream integrity, ECDSA 256/384 bitstream authentication, AES-256 bitstream encryption, physically unclonable function (PUF) protected key storage, side-channel attack resistance, SPDM attestation, cryptographic services, physical anti-tamper support | | | | | | | |
| | Hard processor system | Quad-core 64 bit Arm Cortex-A53 up to 1.50 GHz with 32 KB I/D cache, NEON coprocessor, 1 MB L2 cache, direct memory access (DMA), system memory management unit, cache coherency unit, hard memory controllers, USB 2.0x2, 1G EMAC x3, UART x2, serial peripheral interface (SPI) x4, I2C x5, general purpose timers x7, watchdog timer x4 | | | | | | | |

## Intel Agilex 7 FPGA and SoC I-Series Features

View device ordering codes on page 55.

| Product Line | | AGI 019 | AGI 023 | AGI 022 | AGI 027 | AGI 035 | AGI 040 | AGI 041 |
|---|---|---|---|---|---|---|---|---|
| Resources | Logic elements (LEs) | 1,918,975 | 2,308,080 | 2,208,075 | 2,692,760 | 3,540,000 | 4,047,400 | 4,000,672 |
| | Adaptive logic modules (ALMs) | 650,500 | 782,400 | 748,500 | 912,800 | 1,200,000 | 1,372,000 | 1,356,160 |
| | ALM registers | 2,602,000 | 3,129,600 | 2,994,000 | 3,651,200 | 4,800,000 | 5,488,000 | 5,424,640 |
| | High-performance crypto blocks | 2 | 2 | 0 | 0 | 4 | 4 | 4 |
| | eSRAM memory blocks | 1 | 1 | 0 | 0 | 3 | 3 | 2 |
| | eSRAM memory size (Mb) | 18 | 18 | 0 | 0 | 54 | 54 | 36 |
| | M20K memory blocks | 8,500 | 10,464 | 10,900 | 13,272 | 14,931 | 19,908 | 17,136 |
| | M20K memory size (Mb) | 166 | 204 | 212 | 259 | 292 | 389 | 335 |
| | MLAB memory count | 32,525 | 39,120 | 37,425 | 45,640 | 60,000 | 68,600 | 67,808 |
| | MLAB memory size (Mb) | 20 | 24 | 23 | 28 | 37 | 42 | 42 |
| | Fabric PLL | 5 | 5 | 12 | 12 | 6 | 6 | 8 |
| | I/O PLL | 10 | 10 | 16 | 16 | 12 | 12 | 16 |
| | Variable-precision digital signal processing (DSP) blocks | 1,354 | 1,640 | 6,250 | 8,528 | 9,594 | 12,792 | 0 |
| | 18 x 19 multipliers | 2,708 | 3,280 | 12,500 | 17,056 | 19,188 | 25,584 | 0 |
| | Single-precison or half-precision tera floating point operations per second (TFLOPS) | 2.4 / 4.9 | 2.4 / 4.9 | 9.4 / 18.8 | 12.8 / 25.6 | 14.3 / 28.7 | 19.1 / 38.3 | 0 |
| Maximum Available Device Resources | Maximum EMIF x72[1] | 3 | 3 | 4 | 4 | 4 | 4 | 4 |
| | Maximum differential (RX or TX) pairs | 240 | 240 | 360 | 360 | 288 | 288 | 366 |
| | Maximum AIB Interfaces | 4 | 4 | 4 | 4 | 6 | 6 | 4 |
| | Memory devices supported | DDR4 and QDR IV | | | | | | |
| | Secure Device Manager (SDM) | Provides SHA-384 bitstream integrity, ECDSA 256/384 bitstream authentication, AES-256 bitstream encryption, physically unclonable function (PUF) protected key storage, side-channel attack resistance, SPDM attestation, cryptographic services, physical anti-tamper support | | | | | | |
| | Hard processor system | Quad-core 64 bit Arm Cortex-A53 up to 1.50 GHz with 32 KB I/D cache , NEON coprocessor, 1 MB L2 cache, direct memory access (DMA), system memory management unit, cache coherency unit, hard memory controllers, USB 2.0x2, 1G EMAC x3, UART x2, serial peripheral interface (SPI) x4, I2C x5, general purpose timers x7, watchdog timer x4 | | | | n/a | | HPS support[2] |

* 15 device variants

# Intel SoC FPGA Device Family with Dual Cortex A55 + A76

## Intel Agilex 5 FPGA and SoC D-Series Features

| | Product Line | A5D 010 | A5D 025 | A5D 031 | A5D 051 | A5D 064 |
|---|---|---|---|---|---|---|
| Resources | Logic elements (LEs) | 103,250 | 254,054 | 318,600 | 515,070 | 644,280 |
| | Adaptive logic modules (ALMs) | 35,000 | 86,120 | 108,000 | 174,600 | 218,400 |
| | ALM registers | 140,000 | 344,480 | 432,000 | 698,400 | 873,600 |
| | M20K memory blocks | 534 | 1,281 | 1602, | 2,563 | 3,204 |
| | M20K memory size (Mb) | 10.43 | 25.02 | 31.29 | 50.06 | 62.58 |
| | MLAB memory count | 1780 | 3420 | 5,400 | 8,440 | 10,920 |
| | MLAB memory size (Mb) | 1.09 | 2.09 | 3.30 | 5.15 | 6.67 |
| | I/O PLL | 8 | 8 | 8 | 8 | 8 |
| | Fabric-feeding I/O PLL[1] | 11 | 11 | 11 | 13 | 13 |
| | Variable-precision digital signal processing (DSP) blocks | 276 | 736 | 920 | 1,472 | 1,840 |
| | 18 x 19 multipliers | 552 | 1,472 | 1,840 | 2,944 | 3,680 |
| | Peak INT8 (TOPS) | 8.48 | 22.61 | 28.26 | 45.22 | 56.22 |
| Maximum Available Device Resources | LVDS pairs at 1.6 Gbps | 192 | 192 | 192 | 192 | 192 |
| | DDR4 interface (x64) | 2 | 2 | 2 | 2 | 2 |
| | DDR4/5 and LPDDR4/5 interfaces (x32) | 4 | 4 | 4 | 4 | 4 |
| | MIPI D-PHY interface | 28 | 28 | 28 | 28 | 28 |
| | Differential (RX or TX) pairs at 28 Gbps | 16 | 16 | 16 | 24 | 32 |
| | PCIe 4.0 x4 instance | 4 | 4 | 4 | 6 | 8 |
| | PCIe 4.0 x8 instance | 2 | 2 | 2 | 3 | 4 |
| | High-speed I/O (HSIO) | 384 | 384 | 384 | 384 | 384 |
| | High-voltage I/O (HVIO) | 60 | 60 | 60 | 60 | 60 |
| | Secure Device Manager (SDM) | Provides SHA-384 bitstream integrity, ECDSA 256/384 bitstream authentication, AES-256 bitstream encryption, physically unclonable function (PUF) protected key storage, side-channel attack resistance, SPDM attestation, cryptographic services, physical anti-tamper support | | | | |
| | Hard processor system | Multi-core with 32-bit/64-bit dual-core Arm Cortex-A55 up to 1.5 GHz with 32 KB I/D cache and 128 KB L2 cache, and dual-core Arm Cortex-A76 up to 1.8 GHz with 64 KB I/D cache and 256 KB L2 cache, and up to 2 MB L3 shared cache, multi-channels direct memory access (DMA), 512 KB on-chip RAM, USB3.1 x1, USB 2.0 OTG x2, TSN MAC x3, UART x2, SPI M x2, SPI S x2, I3C x2, I2C x5, NAND x1, SDMMC x1, Osc timer x2, SP timer x2, watchdog x5, GPIO x2. | | | | |
| | Transceiver | PCI Express (PCIe) hard IP up to PCIe 4.0 x8 EP and RP<br>Transceiver channel count: up to 32 channels at 28 Gbps (NRZ)<br>Ethernet IP: up to 16 x10/25 GbE hard IP (MAC, PCS, and FEC) | | | | |



* 5 device variants

# Intel SoC FPGA Device Family with Dual Cortex A55 + A76

## Intel Agilex 5 FPGA and SoC E-Series Features

| | Product Line | Device Group A FPGAs | | | | |
|---|---|---|---|---|---|---|
| | | A5E 013A | A5E 028A | A5E 043A | A5E 052A | A5E 065A |
| Resources | Logic elements (LEs) | 138,060 | 282,256 | 434,240 | 523,920 | 656,080 |
| | Adaptive logic modules (ALMs) | 46,800 | 95,680 | 147,200 | 177,600 | 222,400 |
| | ALM registers | 187,200 | 382,720 | 588,800 | 710,400 | 889,600 |
| | M20K memory blocks | 358 | 716 | 1,050 | 1,288 | 1,611 |
| | M20K memory size (Mb) | 6.99 | 13.98 | 20.51 | 25.16 | 31.46 |
| | MLAB memory count | 2,340 | 4,784 | 6,720 | 8,440 | 11,120 |
| | MLAB memory size (Mb) | 1.43 | 2.92 | 4.10 | 5.15 | 6.79 |
| | I/O PLL | 4 | 4 | 8 | 8 | 8 |
| | Fabric-feeding I/O PLL[1] | 8 | 10 | 11 | 13 | 13 |
| | Variable-precision digital signal processing (DSP) blocks | 188 | 376 | 564 | 676 | 846 |
| | 18 x 19 multipliers | 376 | 752 | 1,128 | 1,352 | 1,692 |
| | Peak INT8 (TOPS) | 5.78 | 11.55 | 17.33 | 20.78 | 25.99 |
| Maximum Available Device Resources | LVDS pairs at 1.6 Gbps | 96 | 96 | 192 | 192 | 192 |
| | DDR4/5 and LPDDR4/5 interfaces (x32) | 2 | 2 | 4 | 4 | 4 |
| | MIPI D-PHY interface | 14 | 14 | 28 | 28 | 28 |
| | Differential (RX or TX) pairs at 28 Gbps | 4 | 12 | 16 | 24 | 24 |
| | PCIe 4.0 x4 instance | 1 | 3 | 4 | 6 | 6 |
| | High-speed I/O (HSIO) | 192 | 192 | 384 | 384 | 384 |
| | High-voltage I/O (HVIO) | 200 | 200 | 120 | 120 | 120 |
| | Secure Device Manager (SDM) | Provides SHA-384 bitstream integrity, ECDSA 256/384 bitstream authentication, AES-256 bitstream encryption, physically unclonable function (PUF) protected key storage, side-channel attack resistance, SPDM attestation, cryptographic services, physical anti-tamper support | | | | |
| | Hard processor system | Multi-core with 32-bit/64-bit dual-core Arm Cortex-A55 up to 1.5 GHz with 32 KB I/D cache and 128 KB L2 cache, and dual-core Arm Cortex-A76 up to 1.8 GHz with 64 KB I/D cache and 256 KB L2 cache, and up to 2 MB L3 shared cache, multi-channels direct memory access (DMA), 512 KB on-chip RAM, USB 3.1 x1, USB 2.0 OTG x2, TSN MAC x3, UART x2, SPI M x2, SPI S x2, I3C x2, I2C x5, NAND x1, SDMMC x1, Osc timer x2, SP timer x2, watchdog x5, GPIO x2. | | | | |
| | Transceiver | PCI Express (PCIe) hard IP up to PCIe 4.0 x4 EP and RP<br>Transceiver channel count: up to 24 channels at 28 Gbps (NRZ)<br>Ethernet IP: up to 6 x10/25 GbE hard IP (MAC, PCS, and FEC) | | | | |

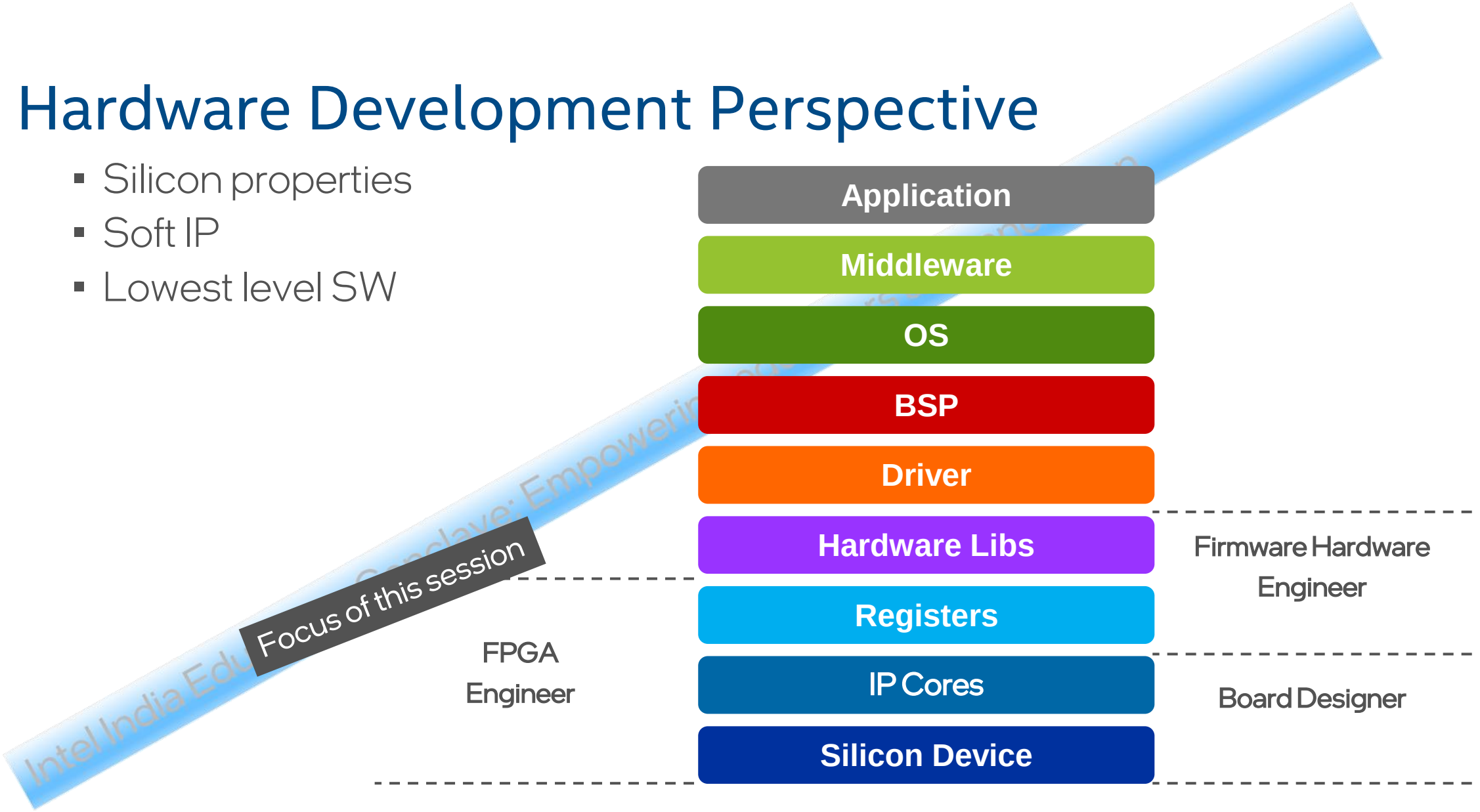
| | Product Line | Device Group B FPGAs | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | A5E 005B | A5E 007B | A5E 008B | A5E 013B | A5E 028B | A5E 043B | A5E 052B | A5E 065B |
| Resources | Logic elements (LEs) | 50,445 | 69,030 | 85,196 | 138,060 | 282,256 | 434,240 | 523,920 | 656,080 |
| | Adaptive logic modules (ALMs) | 17,100 | 23,400 | 28,880 | 46,800 | 95,680 | 147,200 | 177,600 | 222,400 |
| | ALM registers | 68,400 | 93,600 | 115,520 | 187,200 | 382,720 | 588,800 | 710,400 | 889,600 |
| | M20K memory blocks | 130 | 179 | 229 | 358 | 716 | 1,050 | 1,288 | 1,611 |
| | M20K memory size (Mb) | 2.54 | 3.50 | 4.47 | 6.99 | 13.98 | 20.51 | 25.16 | 31.46 |
| | MLAB memory count | 850 | 1,170 | 1,780 | 2,340 | 4,784 | 6,720 | 8,440 | 11,120 |
| | MLAB memory size (Mb) | 0.52 | 0.71 | 1.09 | 1.43 | 2.92 | 4.10 | 5.13 | 6.79 |
| | I/O PLL | 2 | 2 | 4 | 4 | 4 | 8 | 8 | 8 |
| | Fabric-feeding I/O PLL[1] | 5 | 5 | 8 | 8 | 10 | 11 | 13 | 13 |
| | Variable-precision digital signal processing (DSP) blocks | 65 | 94 | 116 | 188 | 376 | 564 | 676 | 846 |
| | 18 x 19 multipliers | 130 | 188 | 232 | 376 | 752 | 1,128 | 1,352 | 1,692 |
| | Peak INT8 (TOPS) | 1.7 | 2.46 | 3.05 | 4.93 | 9.85 | 14.78 | 17.72 | 22.17 |
| Maximum Available Device Resources | LVDS pairs at 1.6 Gbps | 48 | 48 | 96 | 96 | 96 | 192 | 192 | 192 |
| | DDR4 and LPDDR4/5 interfaces (x32) | 1 | 1 | 2 | 2 | 2 | 4 | 4 | 4 |
| | MIPI D-PHY interface | 7 | 7 | 14 | 14 | 14 | 28 | 28 | 28 |
| | Differential (RX or TX) pairs at 17 Gbps | 0 | 0 | 4 | 4 | 12 | 16 | 24 | 24 |
| | PCIe 4.0 x4 instance | 0 | 0 | 1 | 1 | 3 | 4 | 6 | 6 |
| | High-speed I/O (HSIO) | 96 | 96 | 192 | 192 | 192 | 384 | 384 | 384 |
| | High-voltage I/O (HVIO) | 160 | 160 | 200 | 200 | 200 | 120 | 120 | 120 |
| | Secure Device Manager (SDM) | Provides SHA-384 bitstream integrity, ECDSA 256/384 bitstream authentication, AES-256 bitstream encryption, physically unclonable function (PUF) protected key storage, side-channel attack resistance, SPDM attestation, cryptographic services, physical anti-tamper support | | | | | | | |
| | Hard processor system | NA | | Multi-core with 32-bit/64-bit dual-core Arm Cortex-A55 up to 1.33 GHz with 32 KB I/D cache and 128 KB L2 cache, and dual-core Arm Cortex-A76 up to 1.6 GHz with 64 KB I/D cache and 256 KB L2 cache, and up to 2 MB L3 shared cache, multi-channels direct memory access (DMA), 512 KB on-chip RAM, USB 3.1 x1, USB 2.0 OTG x2, TSN MAC x3, UART x2, SPI M x2, SPI S x2, I3C x2, I2C x5, NAND x1, SDMMC x1, Osc timer x2, SP timer x2, watchdog x5, GPIO x2. | | | | |
| | Transceiver | NA | | PCI Express (PCIe) hard IP up to PCIe 4.0 x4 EP and RP<br>Transceiver channel count: up to 24 channels at 17 Gbps (NRZ)<br>Ethernet IP: up to 6 x10 GbE hard IP (MAC, PCS, and FEC) | | | | | |

* 13 device variants

# Development Flow and Tools

# Hardware Development Perspective

- Silicon properties
- Soft IP
- Lowest level SW



# System Development Flow

## Standard FPGA Flow

**Intel® Quartus® Prime**
Design Software

**Hardware Development**

| | |
|---|---|
| ▪ Intel® Quartus® Prime Software<br>▪ Platform Designer<br>▪ Standard RTL flow<br>▪ Intel and partner IP | **Design** |
| ▪ QuestaSim*-Intel® FPGA, VCS, NCSim, etc.<br>▪ AMBA-AXI and Avalon® bus functional models (BFMs) | **Simulate** |
| ▪ Signal Tap II logic analyzer<br>▪ System Console | **Debug** |
| ▪ Intel Quartus Prime Software Programmer<br>▪ In-system Update | **Release** |

FPGA in the Loop

## Standard Software Flow

**Software Development**

arm

| | |
|---|---|
| **Design** | ▪ Arm* Development Studio for Intel® SoC FPGA<br>▪ GNU toolchain<br>▪ OS/BSP: Linux, VxWorks<br>▪ Etc... |
| **Debug** | ▪ GNU, Lauterbach, DS and Arm ecosystem |
| **Release** | ▪ Flash programmer |

# Getting the Intel® Quartus® Prime Software

**Intel® Quartus® Prime**
Design Software

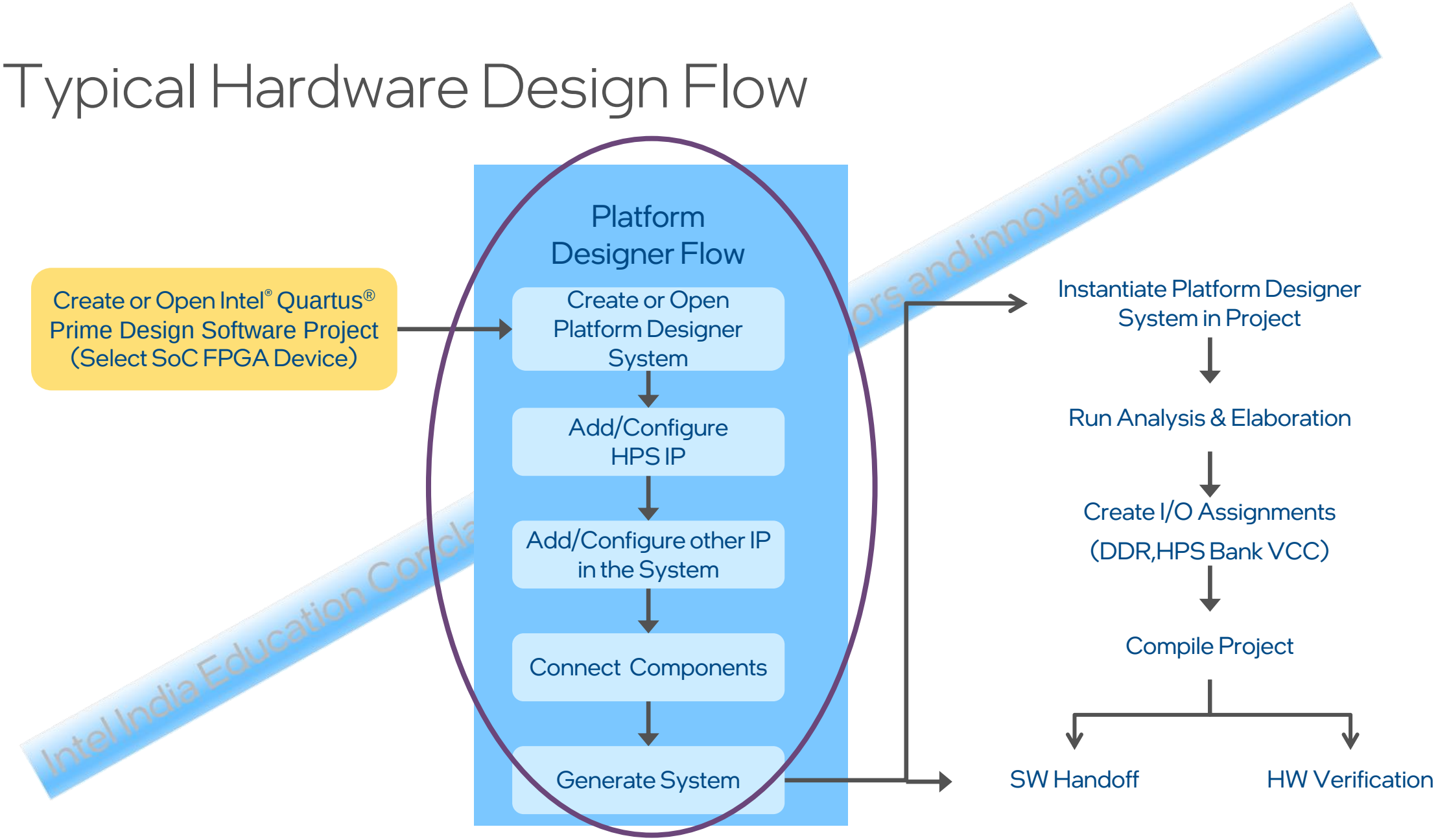
| | |
|---|---|
| **Lite Edition (LE)** | Cyclone® V |
| **Standard Edition (SE)** | Cyclone V, Arria® V, Intel® Arria 10 |
| **Pro Edition (PE)** | Intel Arria 10, Intel Stratix® 10, Intel Agilex™ |

3 editions of software

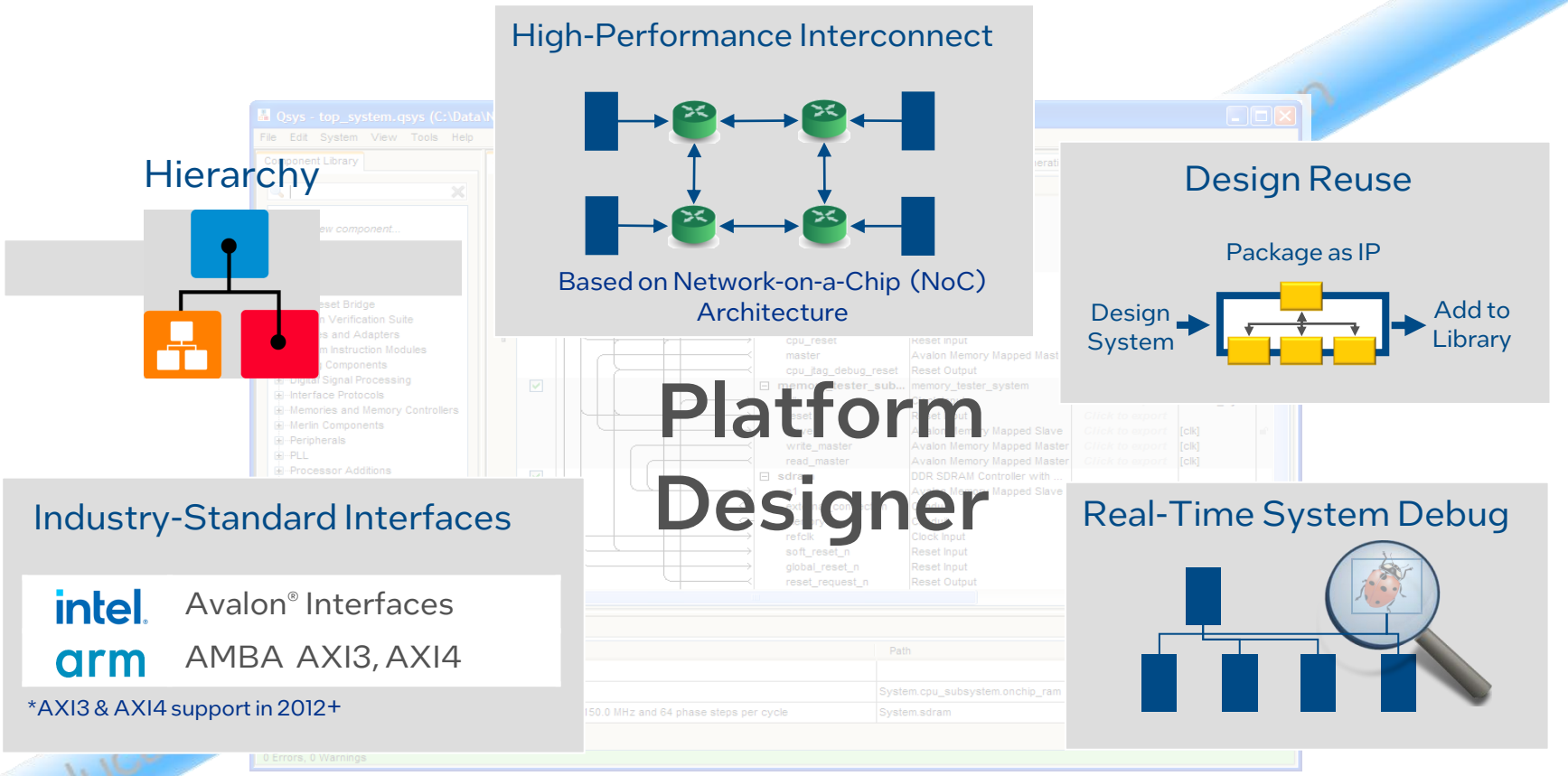
Your need will be based on the device family you are working with

Lite is free; other editions require a paid license

# Typical Hardware Design Flow

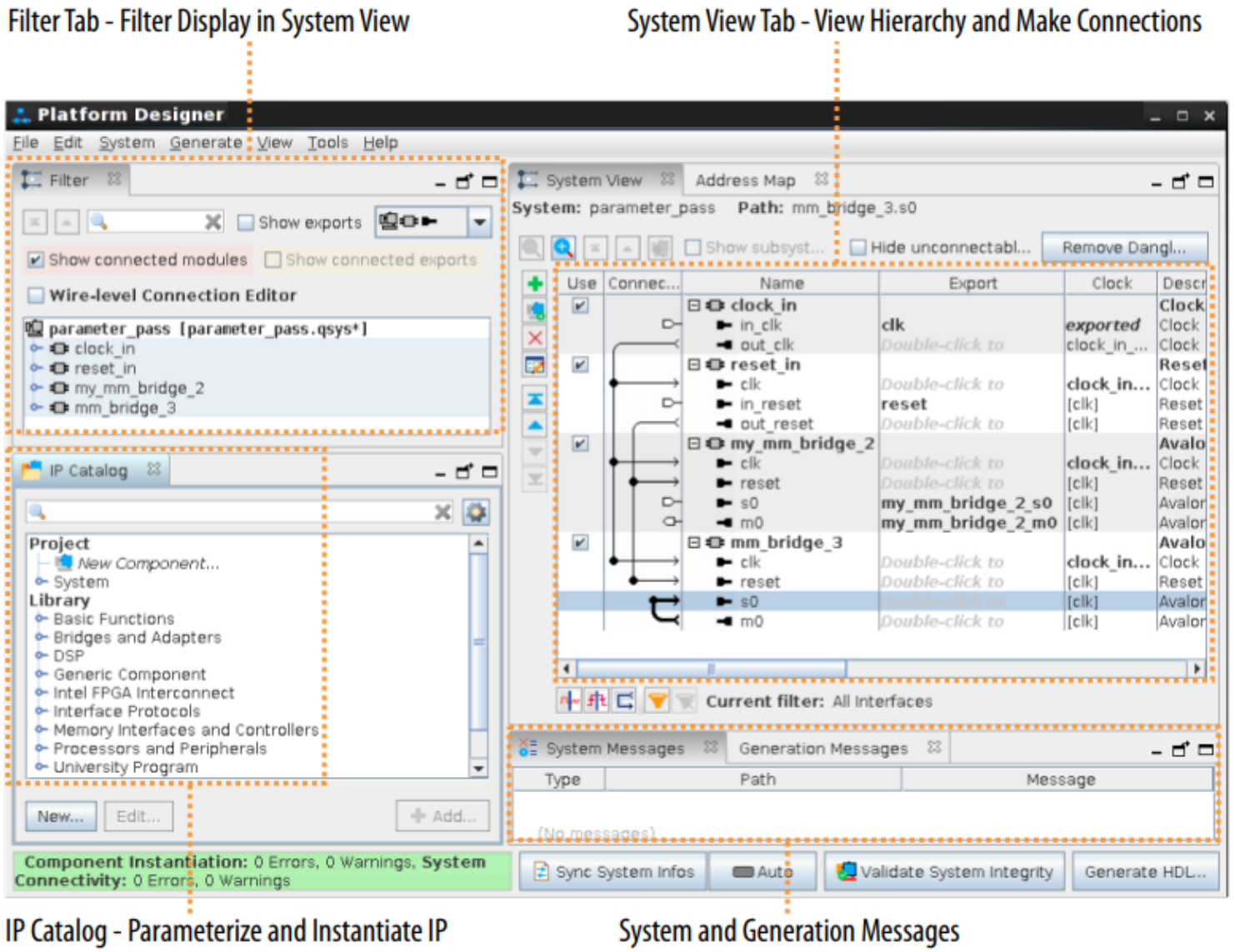


# Platform Designer

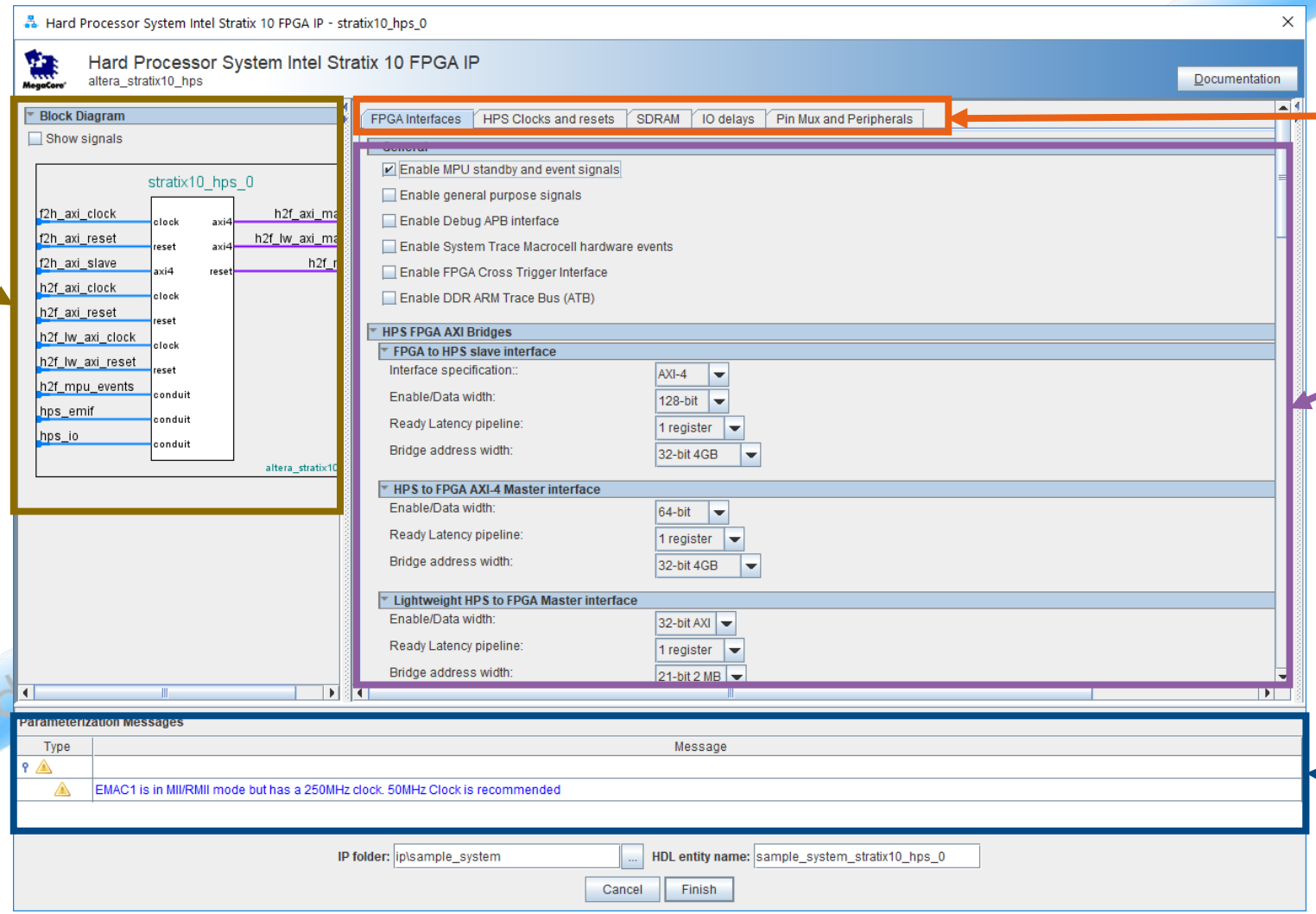



- Platform Designer is Intel's system integration tool for
  - Deployment of IP
  - Deployment of reference designs and example designs
  - Development platform for Intel custom solutions
  - Design platform for customers to quickly create system designs

# Platform Designer User Interface



# The HPS Component



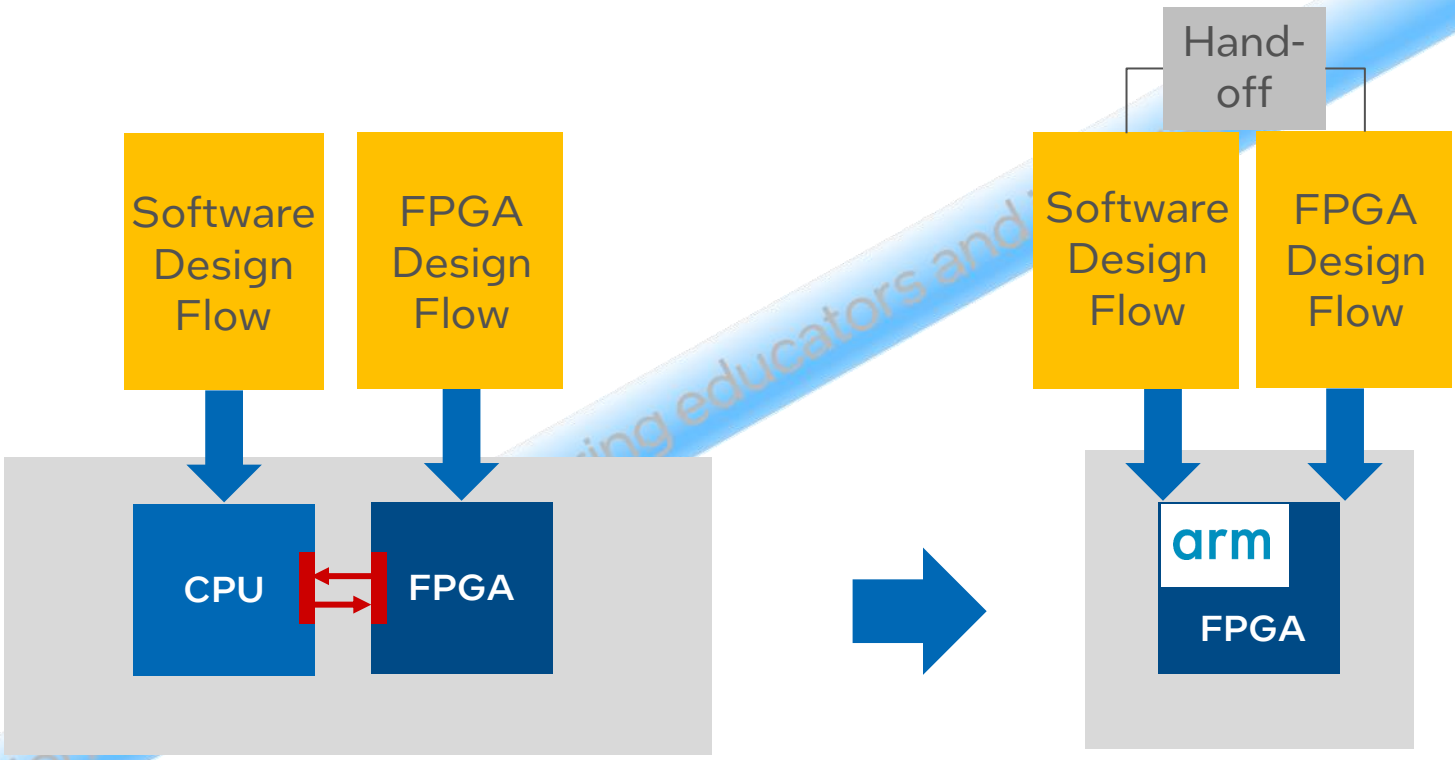

Block diagram interfaces change dynamically

Tabs with categories of settings

Individual setting selections

Dynamic messages with info, warnings, and errors

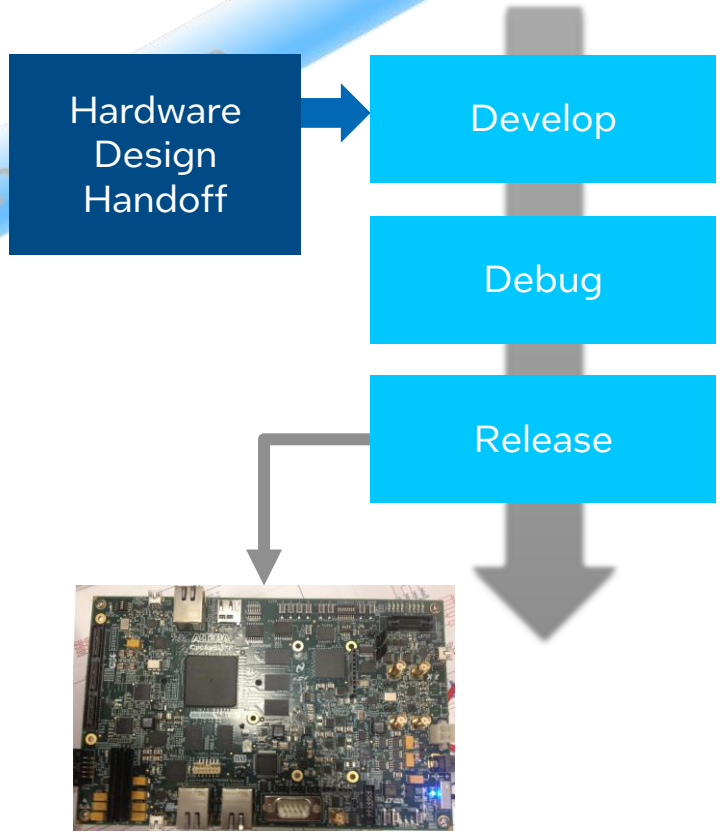
# Design Flow for Intel® SoCs




- Preserves standard design flow
- Automates hardware or software handoff
- Takes advantage of hardware integration

# Software Design Flow

- Standard development environment
  - Arm* Development Studio for Intel® SoC FPGA and/or partner IDE
- Standard software enablement
  - HWLIBs for use with or without operating system
- Standard design flow
  - No proprietary or additional tools required

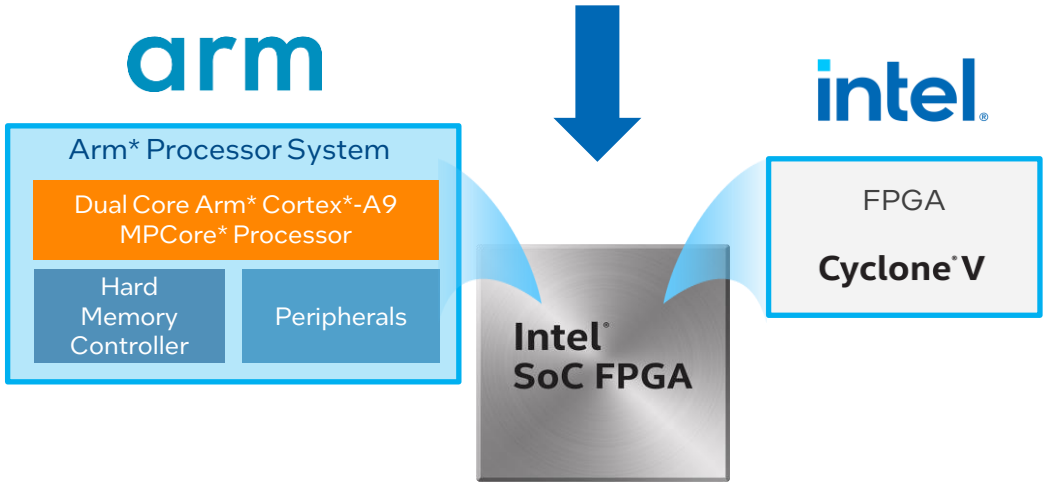





Intel SoCs provide high software developer productivity

# Arm* Development Studio for Intel® SoC FPGA Overview

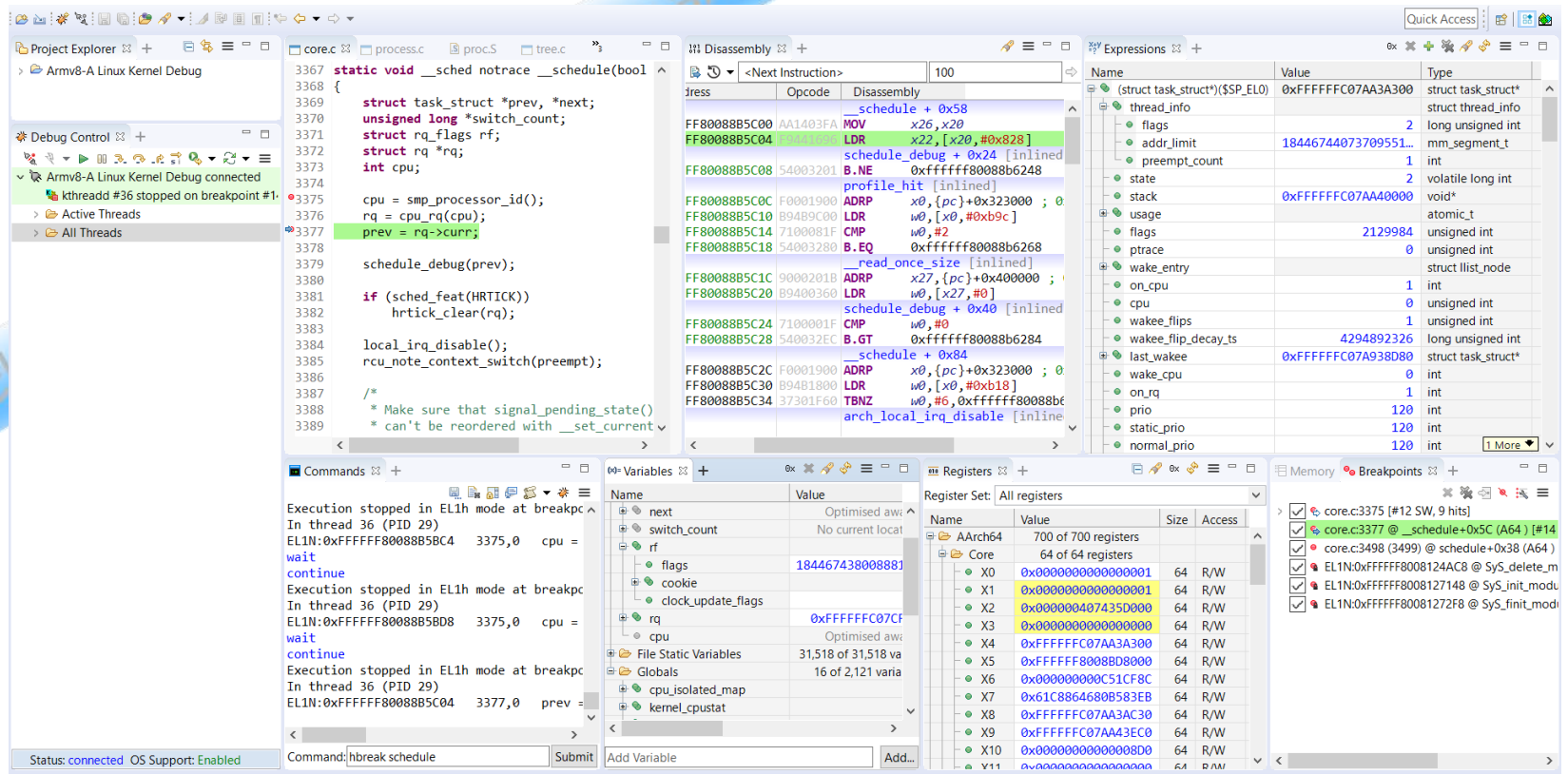
- Arm-Intel strategic partnership with unique OEM arrangement
- Complete multi-core debug and Arm CoreSight compliant trace
- Includes Arm compiler and Intel GCC compiler
- Industry-only FPGA-adaptive debug support
- Low cost, included in Intel SoC development kits

# Arm Development Studio for Intel® SoC FPGA Edition

## Arm's debug environment made for Arm processors

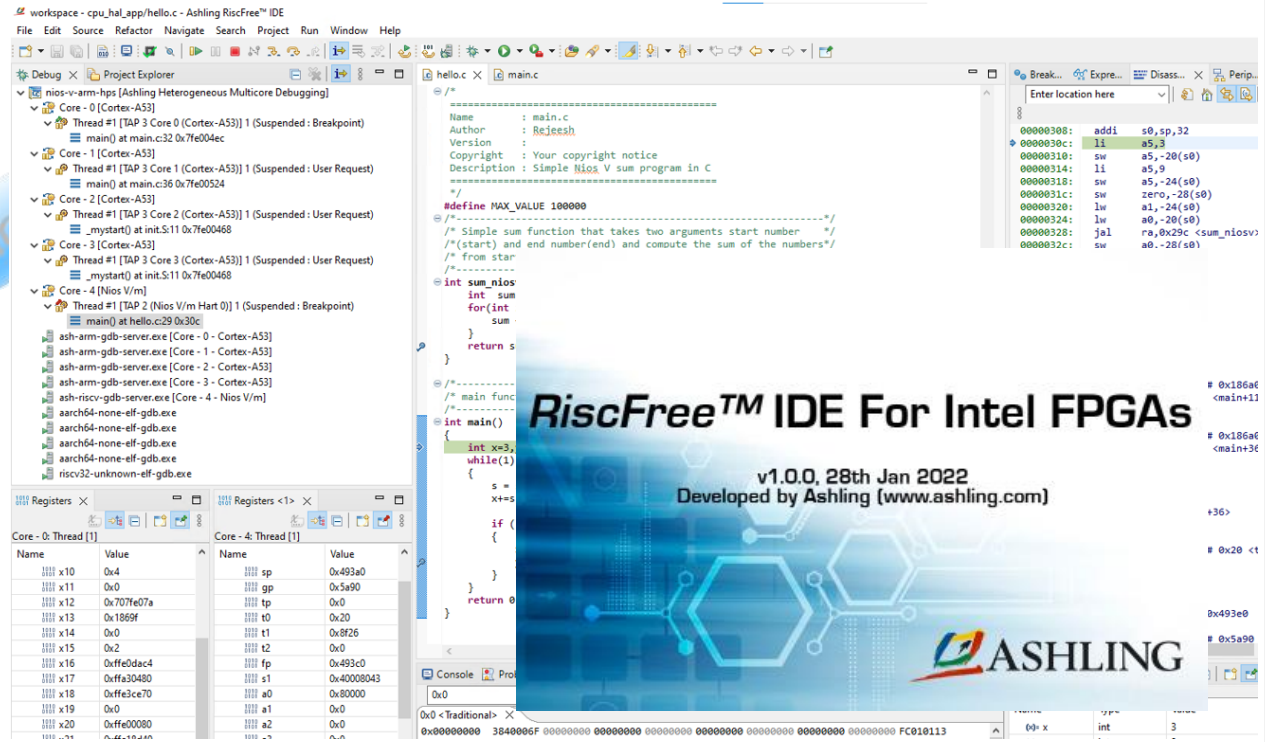
- Eclipse-based IDE
- Set hardware and software breakpoints
- Run scripts
- View disassembly
- Performance profiling



# RiscFree* IDE for Intel® FPGAs

## Out-of-box experience with Ashling's* RiscFree* IDE for Intel® FPGAs

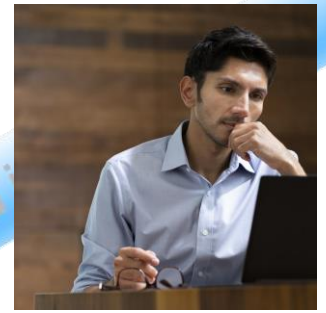
- Included with the Quartus Prime Pro Software version 22.2 onwards or available as a standalone installer for embedded software developers
- Full tool-chain including Ashling's* RiscFree* for Intel FPGAs IDE, Compiler, Debugger and Trace
- Provides software development and debug support for Nios® V and arm* processors
- Supports Intel Agilex™, Stratix® 10, Arria® 10, Cyclone® and Max 10 devices



# FPGA-Adaptive Debug

How do I develop embedded software that interfaces with the FPGA?

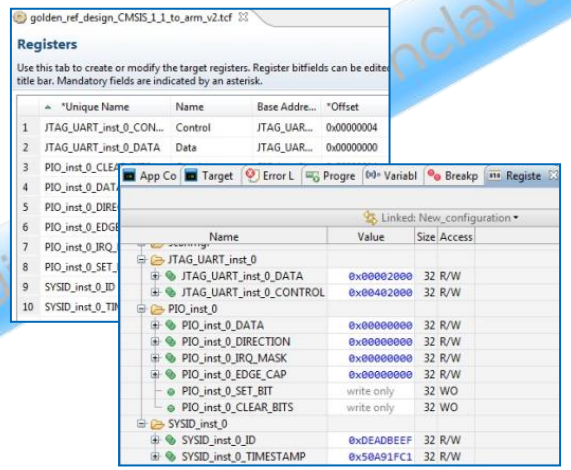
Drivers?



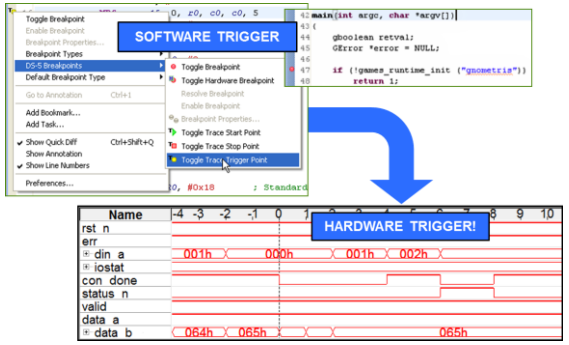
Optimize?

Debug?

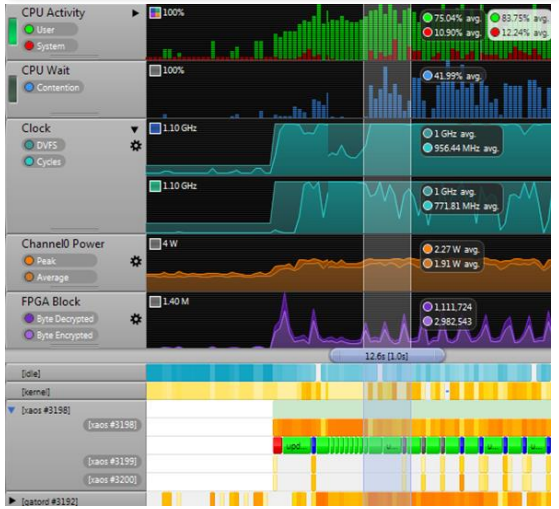
Register views of FPGA peripherals




Cross triggering and global time stamping

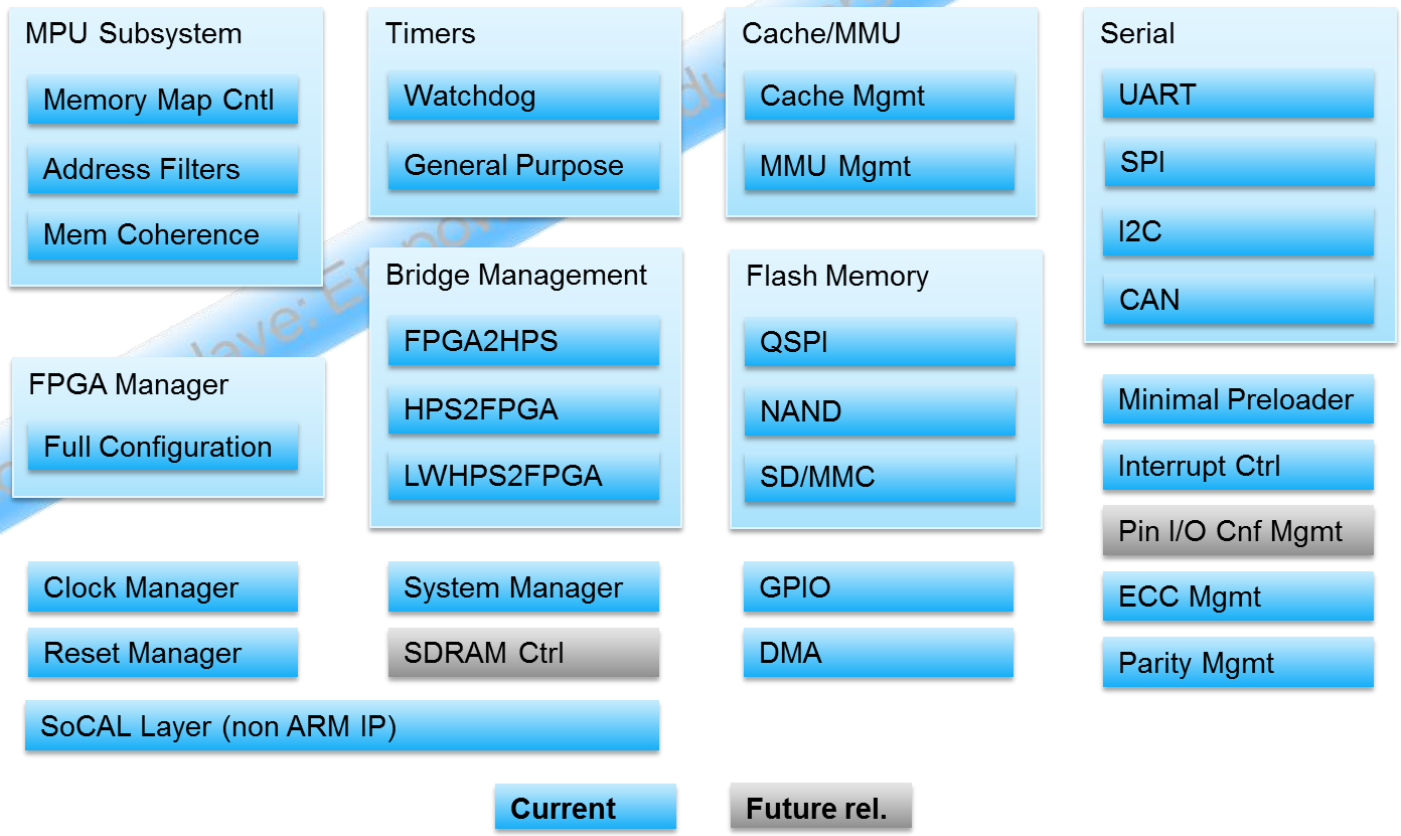



Arm* Development Studio for Intel® SoC FPGA Performance Analysis



# SoC Hardware Libraries - HWLIBs

Intel developed libraries for operating system enablement or bare-metal development



# Intel Embedded Software Leadership

## Ecosystem

A number of Operating Systems, development tools, IP cores, and professional services provided by SoC FPGAs partners.

Our ecosystem provides timely enablement and widely available support.

## Open Source

Intel provides comprehensive Linux OS enablement for SoC FPGAs.
**Visit Rocketboards.org**

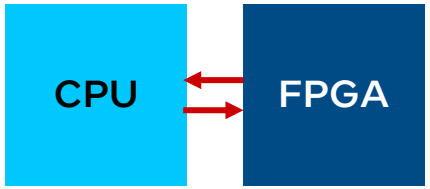
Intel embraces industry standards and leads the open source software community.
**Visit 01.org**

## Standard Software Development Flow


The SoC EDS includes user-friendly tools for software developers:

- ARM DS IDE with Intel enhancements
- Compiler, debugger, and profiler
- Hardware Libraries for bare-metal

## CPU+FPGA Value




Intel unlocks FPGA benefits through advanced embedded software development tools:

- Adaptive debug with cross-triggering
- Heterogeneous development
- High Level Design tools
- Embedded acceleration frameworks

## System Benefits of CPU+FPGA Integration thru Intel SoC FPGAs

- Increased System Performance
- Reduced Board Size
- Reduced Power Consumption
- Reduced System Cost

* Quartus 20.3, all SoC EDS components migrated to GitHub and can download from https://github.com/altera-opensource

# Industry Best-Practice Linux Enablement

- Up-to-date kernel and driver support
- Easy to create Linux distribution with Angstrom and Yocto
- Rocketboards.org portal; git repository; community support
- Partnerships for commercial Linux

LONG TERM SUPPORT INITIATIVE

Ångström

yocto PROJECT

git

# Embedded Operating System Availability





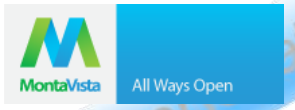
| Vendor | OS/RTOS | Development Tools | Available From |
|---|---|---|---|
| Open Source | Linux (current and 5.10 LTSI) | Linaro compiler | rocketboards.org |
| Wind River Systems | VxWorks 6.9.3 and 7.0 | Wind River Workbench | Wind River |
| Micriμm | μC/OS-II, μC/OS-III | GNU compiler | Micriμm |
| Enea | OSE 5.5.3 | Optima 2.6 | ENEA |
| Express Logic | ThreadX G5.5.5.0 | GNU compiler | Express Logic |
| Wind River Systems | Wind River Linux 5 and 7 | Workbench/GNU | Wind River |
| QNX | QNX/Neutrino 6.5.3 and 6.6 | Momentics | QNX |
| Fujisoft | Android | GNU compiler | Fujisoft |
| Green Hills | INTEGRITY | Multi/Green Hills | Green Hills |
| DDC-I | Deos | DDC-I | DDC-I |
| Code Time | Multicore Abassi | ArmCC/GCC | Code Time |
| Mentor | Nucleus | GCC | Mentor |
| eCosCentric | ECOSPRO (eCos) | GCC | eCosCentric |





# Embedded Operating System Availability (page 2)






| Vendor | OS/RTOS | Development Tools | Available From |
|---|---|---|---|
| MRA Digital | Android | GCC | MRA Digital |
| FreeRTOS | RTE | Arm* Development Studio for Intel® SoC FPGA and GCC | Freertos.org |
| Monta Vista | CGE7 Linux | Monta Vista/GCC | Monta Vista |
| AUTOSAR | AUTOSAR 4.0.3 MCAL | Elektrobit Tresos Studio | Intel |
| Microsoft | Windows Embedded 7 | Microsoft/Studio | Adeneo Embedded |
| Quadros | RTXC | GCC | Coming |
| rtems.org | RTEMS | GCC | rtems.org |




# Broad JTAG Debugging Tools Support

| Company | Debugger |
|---|---|
| Intel | Intel® FPGA Download Cable II |
| Lauterbach | Trace32 |
| Arm | DSTREAM |
| Wind River | ICE II, Probe |
| Green Hills | Probe |
| Yokogawa Digital Computer | AdviceLUNA |
| Kyoto Microcomputer | Partner-Jet |
| Computex | PALMiCE3 |
| Segger | J-Link |
| iSystem | Coming Soon |
| Ronetix | PEEDI |

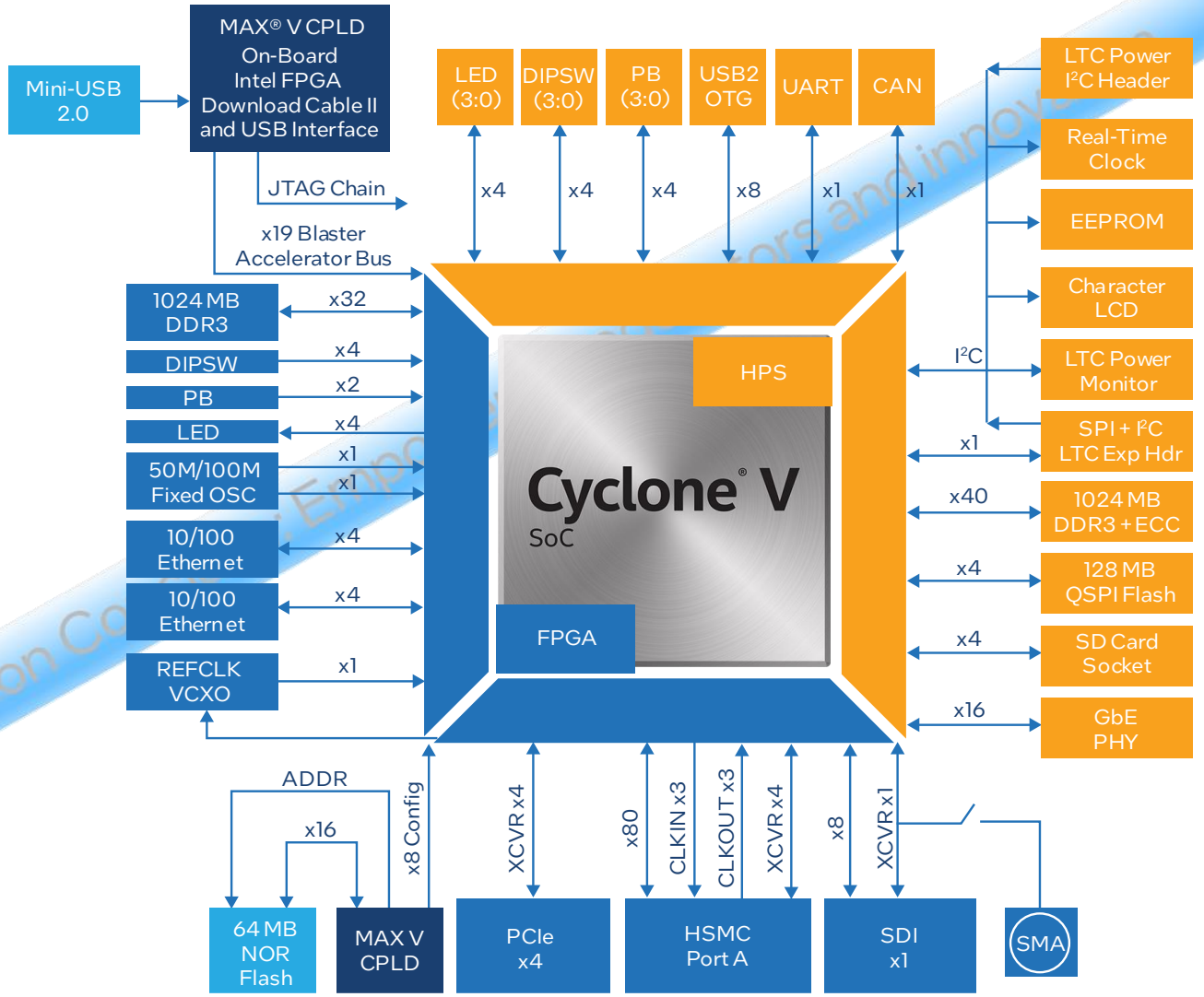
# Development Kits & Solutions

# Cyclone® V SoC Development Kit

- Everything you need to begin development
  - Board, power supply, cables, reference design
  - One user license for Arm Development Studio for Intel SoC FPGA
  - Uses Intel® Quartus® development software
- Features:
  - Ethernet, USB, CAN, UART
  - DDR3 (HPS and FPGA), SDCard, QSPI Flash
  - PCIe (rootport & endpoint)
  - HSMC header, Mictor (debug)
  - On-board Intel FPGA Download Cable debug/download probe
  - Much more . . .

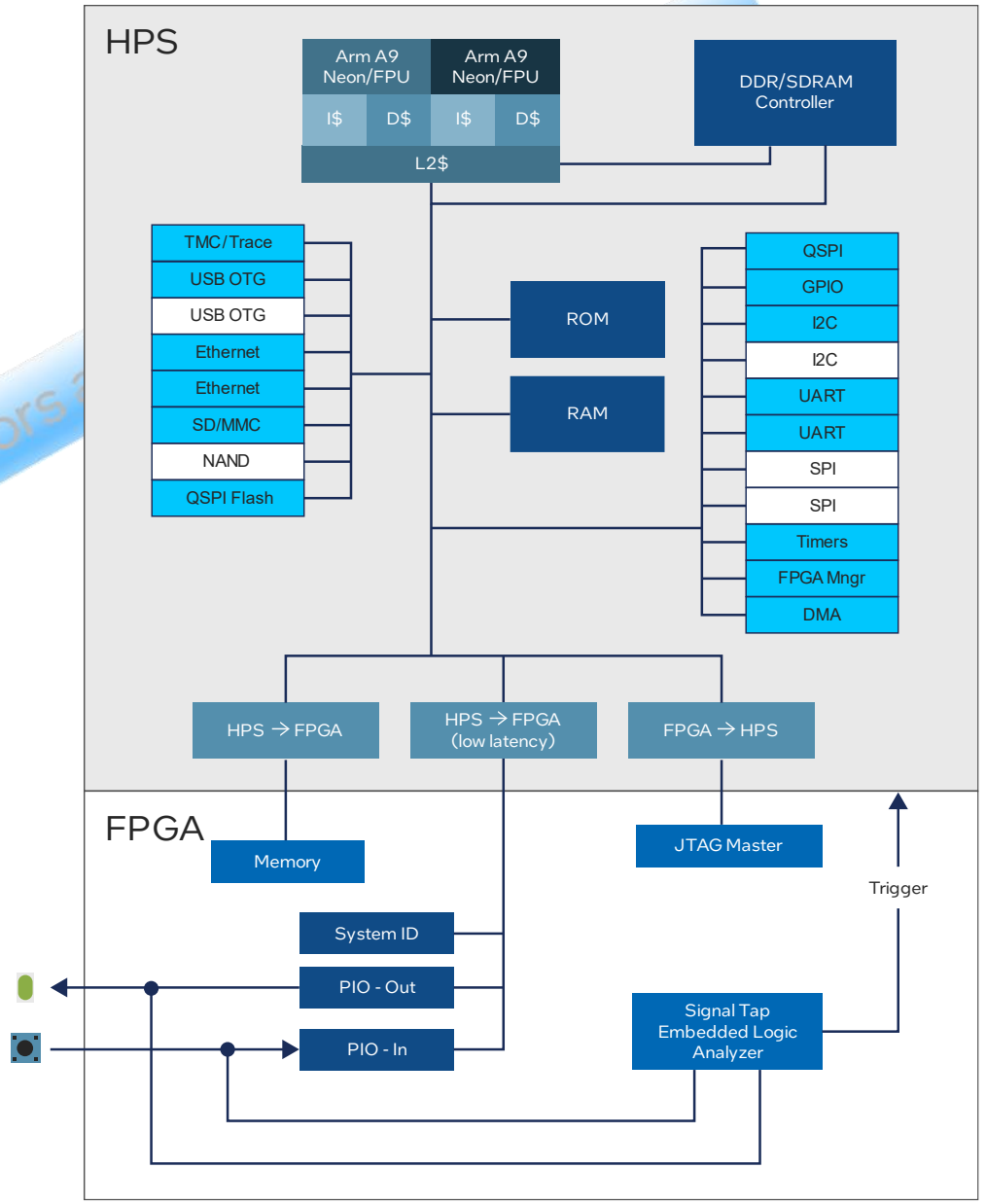
    https://www.intel.com/content/www/us/en/products/details/fpga/development-kits/cyclone/v-sx.html
- Available now
  - Part number: DK-DEV-5CSXC6N
  - List price: $1,795

# Cyclone® V SoC Kit Block Diagram



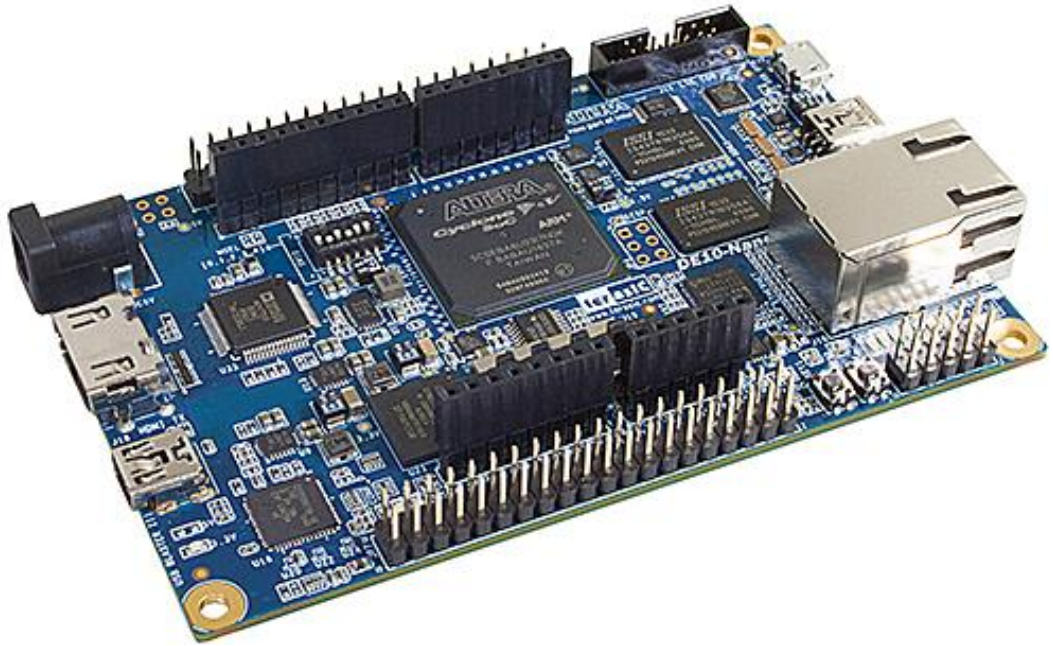
# Golden Reference Design

- HPS configuration
  - DRAM, QSPI, SD/Card
  - All peripheral functions exposed at least once
- FPGA configuration
  - Simple Platform Designer “sandbox” system
  - Getting started guide to walk them through the process on integrating IP
    - Hardware simulation
    - Verification via system console
    - Verification via CPU
    - Hardware or software hand-off
    - eSW development and debug



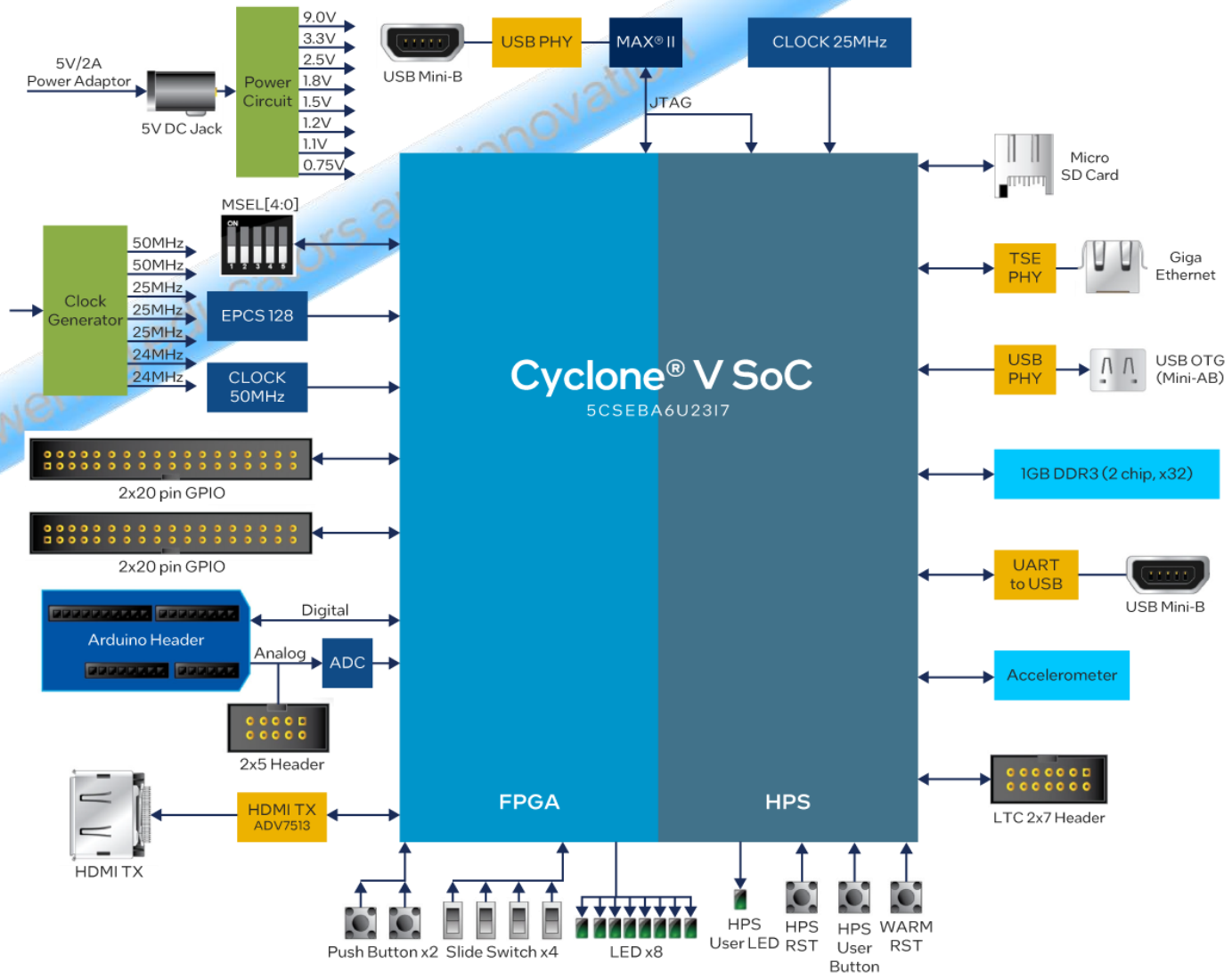
# Terasic DE10-Nano Low-Cost Development Platform

- Boots Linux, runs web server, and VNC server (remote access)
  - Native Arm software tools built-in (no download required)
  - Cross compiler tools available for free download
- Hardware acceleration example design in FPGA
- Example designs on Intel IoT Developer Zone



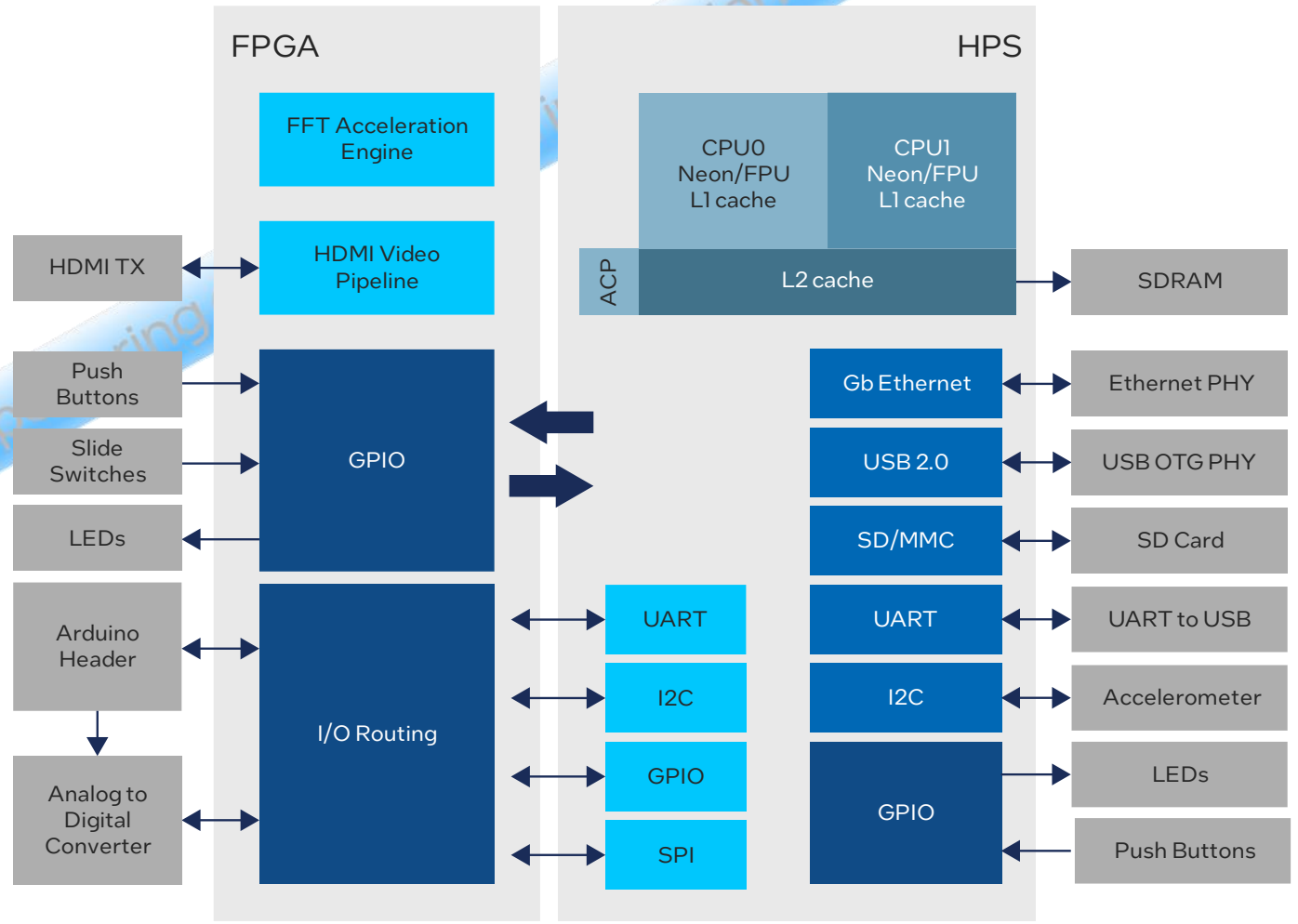
# Board Bock Diagram

- Cyclone® V SoC
  - Dual-core Arm Cortex-A9
  - 800 MHz
  - 110K LE
- Features
  - Ethernet, USB 2.0, UART
  - Micro-SD Card, EPCS flash
  - Accelerometer, analog-to-digital converter (ADC), HDMI
  - Intel® FPGA Download Cable
  - Arduino header
  - Two 2x20 pin headers
  - LEDs, push buttons, switches



# System Reference Design

- FPGA Configuration
  - 32-bit FFT engine
  - x2 DMA
  - 4K SRAM buffer
  - GPIO for LEDs, push buttons, and slide switches
- Embedded Software
  - OS: Linux
    - Kernel v4.1.33 LTSI
    - Angstrom v2016.12
  - Demo Applications:
    - GPIO
    - Accelerometer
    - Fast Fourier transform (FFT) acceleration
  - Other:
    - Web server
    - VNC server



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# DISCOVER THE TERASIC DE10-NANO KIT

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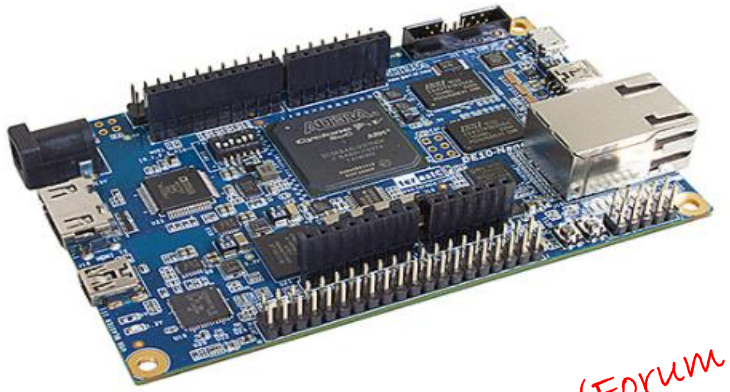

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- Write an Image to the microSD* Card

**Technical Details**

- Board Schematic
- Board Mechanical Layout

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## Inside the Kit

This kit includes a variety of reference designs, tools, and documentation designed for different types of developers.

- For embedded software developers, the system-on-chip (SoC)

# Edge-Centric SOM

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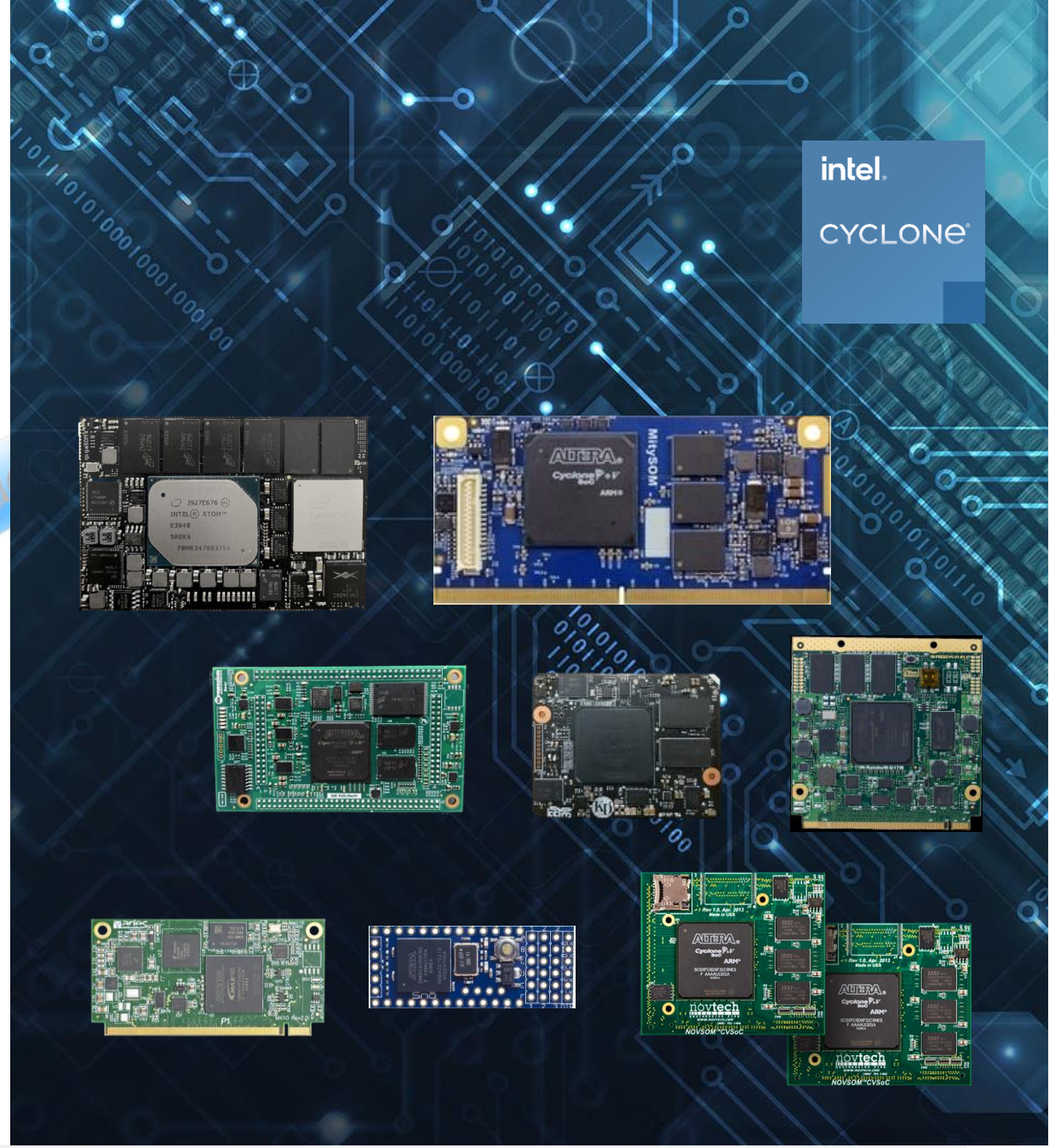
# Edge-Centric FPGA SoM

## Save your development time with reduced risk

Intel partners' edge-centric programmable system on module (SoM) portfolio offers versatility of application use cases in a production-ready hardware for time-to-market advantage and lower risk of complex board design

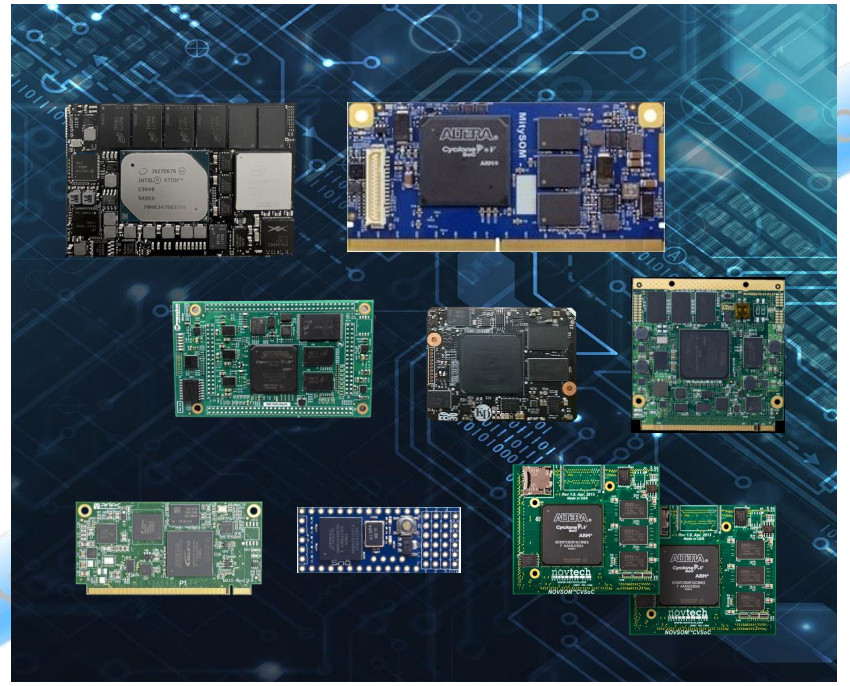
[Intel Partner SoM Web Page]



# Intel Partner SoM Ecosystem

## Features

- Small, highly integrated single-board computers includes DRAM, flash memory, power management, common interface controllers, and board support package (BSP) software
- Dozens of partner products available ranging from Intel® MAX®, Intel® Cyclone®, Intel® Arria®, Intel® Stratix® to Intel® Agilex™ FPGAs and SoCs



## Target Applications

- General embedded applications
- Industrial PC, factory automation, and control application
- Machine vision, surveillance camera, and retail
- Networking and security application
- Test and measurement equipment

## Customer Benefits

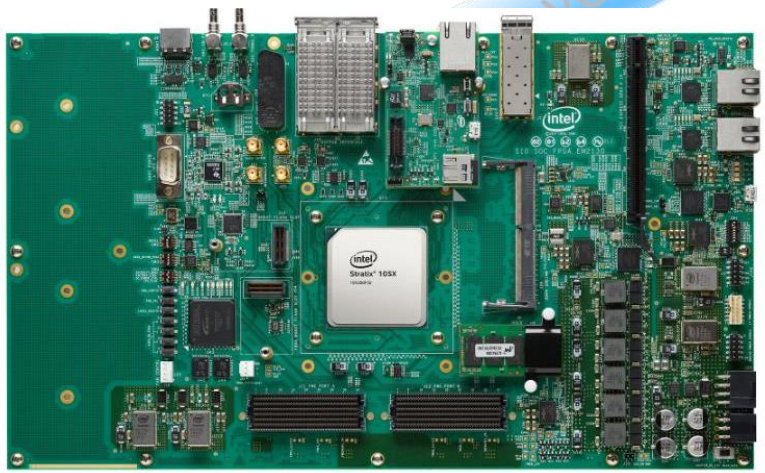
- Faster time to market by off-loading complex board design
- Production-ready hardware for immediate deployment
- Versatile product design and application fit from various partners
- Minimize component supplier management

# Cyclone® V SoC SoM Partner Ecosystem

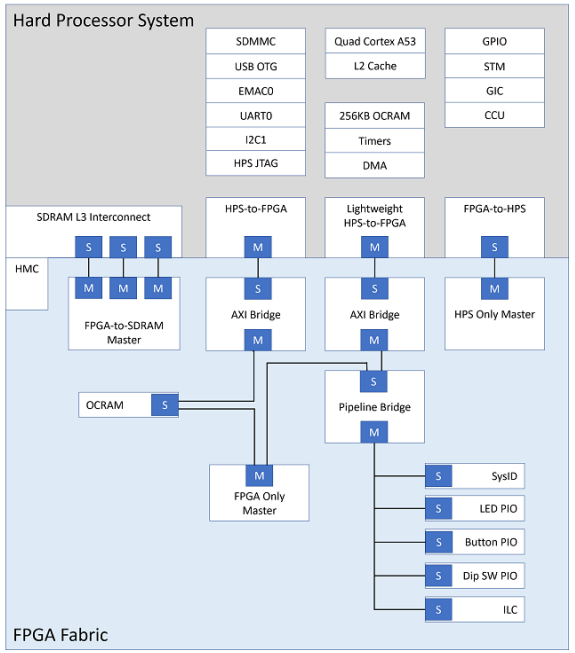
| Partner | Partner Tier | SoM Product Name | Intel Device | FPGA Logic Elements | Target Application | Size (mm) |
|---|---|---|---|---|---|---|
| Exor International | Titanium | microSOM us02 | Cyclone® V SoC (SE) | 25K/110KLEs | Industrial | 48x35 |
| Critical Link | Gold | MitySOM-5CSX | Cyclone® V SoC (SX) | Up to 110KLEs | General Purpose | 82x39 |
| Enclustra | Gold | Mercury SA1 | Cyclone® V SoC (SX) | 110KLEs | Industrial | 56x54 |
| | | Mercury+ SA2 | Cyclone® V SoC (ST) | 110KLEs | Industrial | 74x54 |
| iWave System Technologies | Gold | iW-RainboW-G17M | Cyclone® V SoC (SX) | Up to 110KLEs | General Purpose | 70x70 |
| Kondo Electronics | Gold | KEIm-CVSoC | Cyclone® V SoC (SX) | 85KLEs | Video & Vision, Industrial | 70x35 |
| MRA Digital | Gold | C5SOC-SOM-PROCESSOR | Cyclone® V SoC (SX) | 110KLEs | Video interface, Image processing | 66x56 |
| NDR | Gold | N-EMB-100/110 | Cyclone® V SoC (SX) | 110KLEs | Industrial Networking | TBD |
| Novtech | Gold | NOVSOM CVLite | Cyclone® V SoC (SE) | Up to 110KLEs | General purpose | 68x35 |
| | | NOVSOM CV | Cyclone® V SoC (SE, SX, ST) | Up to 110KLEs | General purpose | 73x64 |
| Aries | Member | MCV | Cyclone® V SoC (SE, SX) | Up to 110KLEs | General purpose | 74x42 |
| Macnica | Distributor | Borax SOM | Cyclone® V SoC (SE) | Up to 110KLEs | General purpose | 95x55 |

# How to Best Get Started on Your Design

- Development Kit
  - Schematics and board files supplied
  - Intel® Stratix® 10 SoC FPGA https://www.intel.com/content/www/us/en/programmable/products/boards_and_kits/dev-kits/altera/stratix-10-soc-development-kit.html
  - Intel® Agilex™ SoC FPGA https://www.intel.com/content/www/us/en/programmable/products/boards_and_kits/dev-kits/altera/kit-agf-si.html



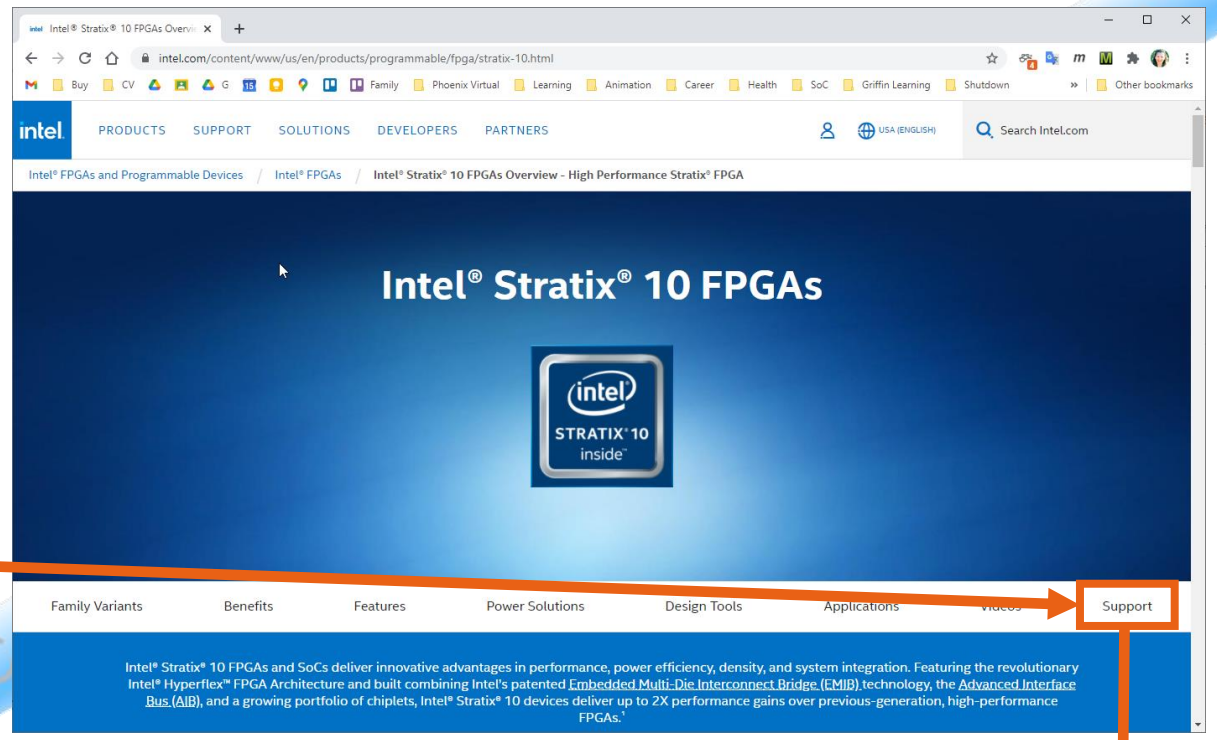
- Golden System Reference Design (GSRD)



# How To Access Documentation Resources

Search for the device family in your favorite search engine

Click on the first result, taking you to the device family landing page

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Direct Links:

https://www.intel.com/content/www/us/en/programmable/products/stratix-series/s10/support/documentation.html

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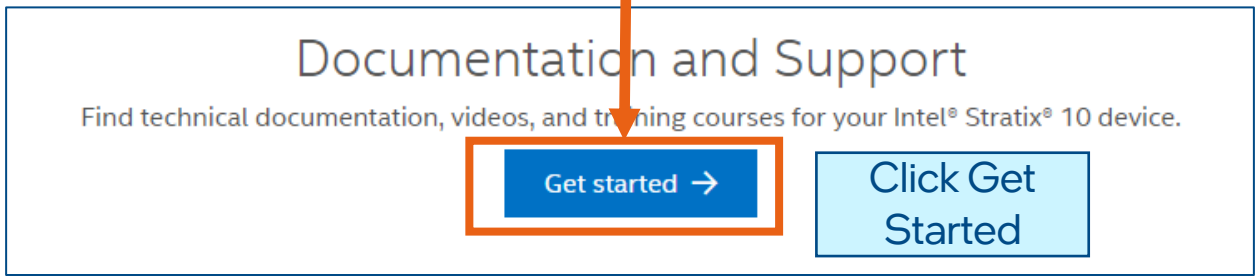


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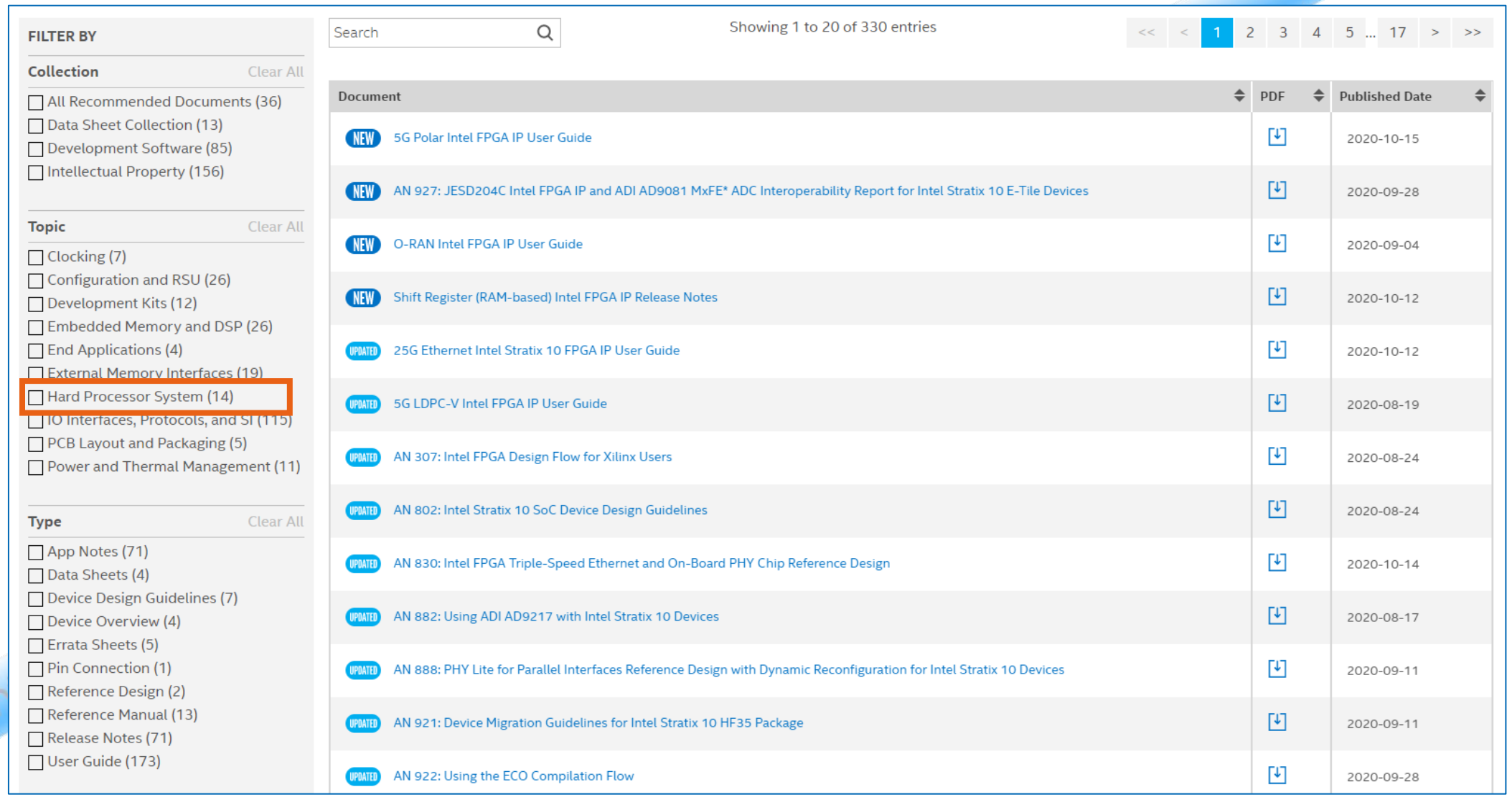

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| NEW O-RAN Intel FPGA IP User Guide | | 2020-09-04 |
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| UPDATED AN 882: Using ADI AD9217 with Intel Stratix 10 Devices | | 2020-08-17 |
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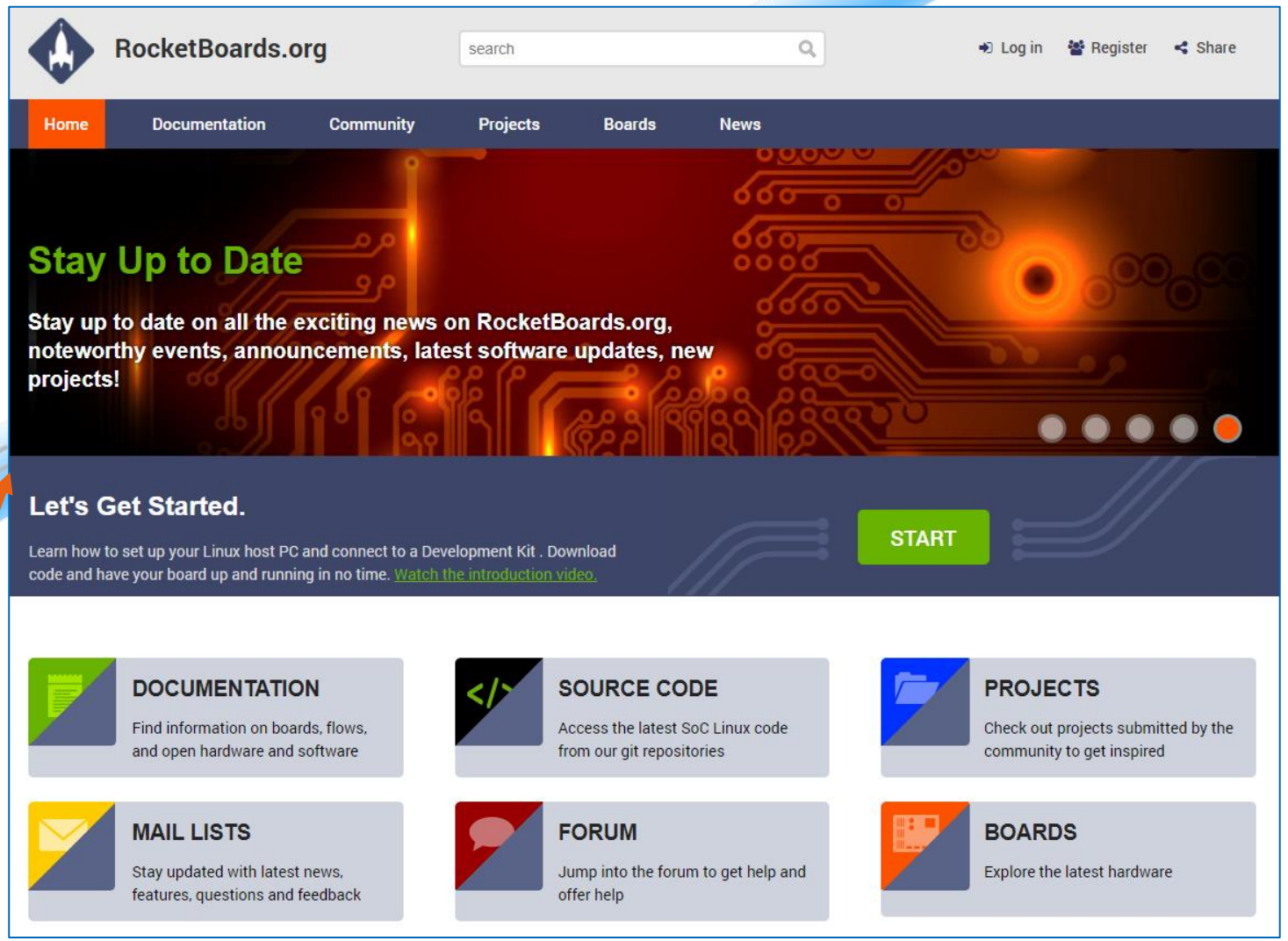
| UPDATED AN 921: Device Migration Guidelines for Intel Stratix 10 HF35 Package | | 2020-09-11 |
| UPDATED AN 922: Using the ECO Compilation Flow | | 2020-09-28 |

# How To Access Software Resources

For the U-Boot & Linux* OS based flow used by most customers, RocketBoards.org is your first and best resource.

You'll learn more about throughout the class.

https://rocketboards.org



# Guide to SoC Information Resources

## Planning Your Board Design

- Board Developer Center
  - https://www.intel.com/content/www/us/en/programmable/support/support-resources/design-guidance/board-developer.html
- Pin Connection Guidelines
  - Intel® Stratix® 10 FPGAs:
    - https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/dp/stratix-10/pcg-01020.pdf
  - Intel Agilex™ FPGAs:
    - https://www.intel.com/content/dam/altera-www/global/en_US/pdfs/literature/dp/agilex/pcg-01023.pdf

## General Design Planning

- Device Design Guidelines
  - Intel Stratix 10 SoC FPGAs
    - https://www.intel.com/content/dam/altera-www/global/en_US/pdfs/literature/an/an802-s10-soc-device-design-guidelines.pdf
  - Intel Agilex SoC FPGAs
    - https://www.intel.com/content/dam/altera-www/global/en_US/pdfs/literature/an/an886-agilex-device-design-guidelines.pdf
- Device Datasheets
  - Intel Stratix 10 FPGAs
    - https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/hb/stratix-10/s10_datasheet.pdf
  - Intel Agilex FPGAs
    - https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/hb/agilex/ag_datasheet.pdf

# Guide to SoC Information Resources

## Booting and Configuration

- Boot User Guide
  - Intel® Stratix® 10 SoC FPGAs
    - https://www.intel.com/content/dam/altera-www/global/en_US/pdfs/literature/ug/ug-s10-soc-boot.pdf
- Configuration User Guide
  - Intel Stratix 10 FPGAs
    - https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/hb/stratix-10/s10_datasheet.pdf
  - Intel Agilex™ FPGAs
    - https://www.intel.com/content/dam/altera-www/global/en_US/pdfs/literature/hb/agilex/ug-ag-config.pdf

## HPS

- HPS Technical Reference Manual
  - Intel Stratix 10 SoC FPGAs
    - https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/hb/stratix-10/s10_5v4.pdf
  - Intel Agilex SoC FPGAs
    - https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/hb/agilex/mnl-1100.pdf
- HPS Component Reference Manual
  - Intel Stratix 10 SoC FPGAs
    - https://www.intel.com/content/dam/altera-www/global/en_US/pdfs/literature/hb/stratix-10/s10-hpscomponent.pdf
  - Intel Agilex SoC FPGAs
    - https://www.intel.com/content/dam/altera-www/global/en_US/pdfs/literature/manual/mnl-1103.pdf

# Guide to SoC Information Resources

## Software

- GSRD User Manual
  - Intel® Stratix® 10 FPGAs
    - https://rocketboards.org/foswiki/Documentation/Stratix10SoCGSRD
  - Intel Agilex™ FPGAs
    - https://rocketboards.org/foswiki/Documentation/AgilexSoCGSRD
- Programmer's Reference Manual
  - Intel Stratix 10 SoC FPGAs
    - https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/manual/mnl-1091.pdf

## Other

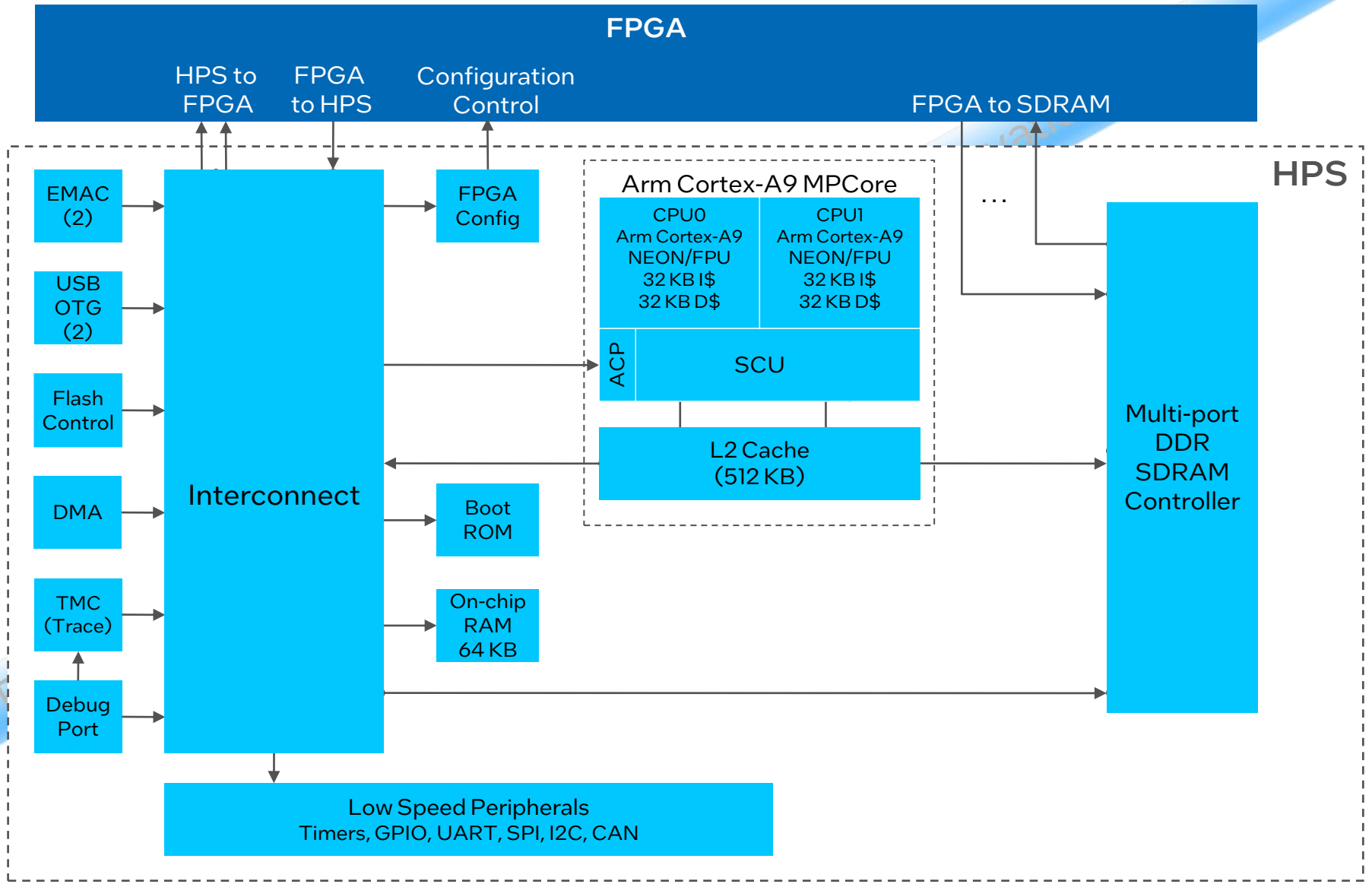
- Development Kit User Guide
  - Intel Stratix 10 SoC FPGAs
    - https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/ug/ug-intel-s10-soc-devl-kit.pdf
  - Intel Agilex SoC FPGAs
    - https://www.intel.com/content/dam/altera-www/global/en_US/pdfs/literature/ug/ug-agilex-soc-devl-kit.pdf
- Product Catalog
  - https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/sg/product-catalog.pdf


intel

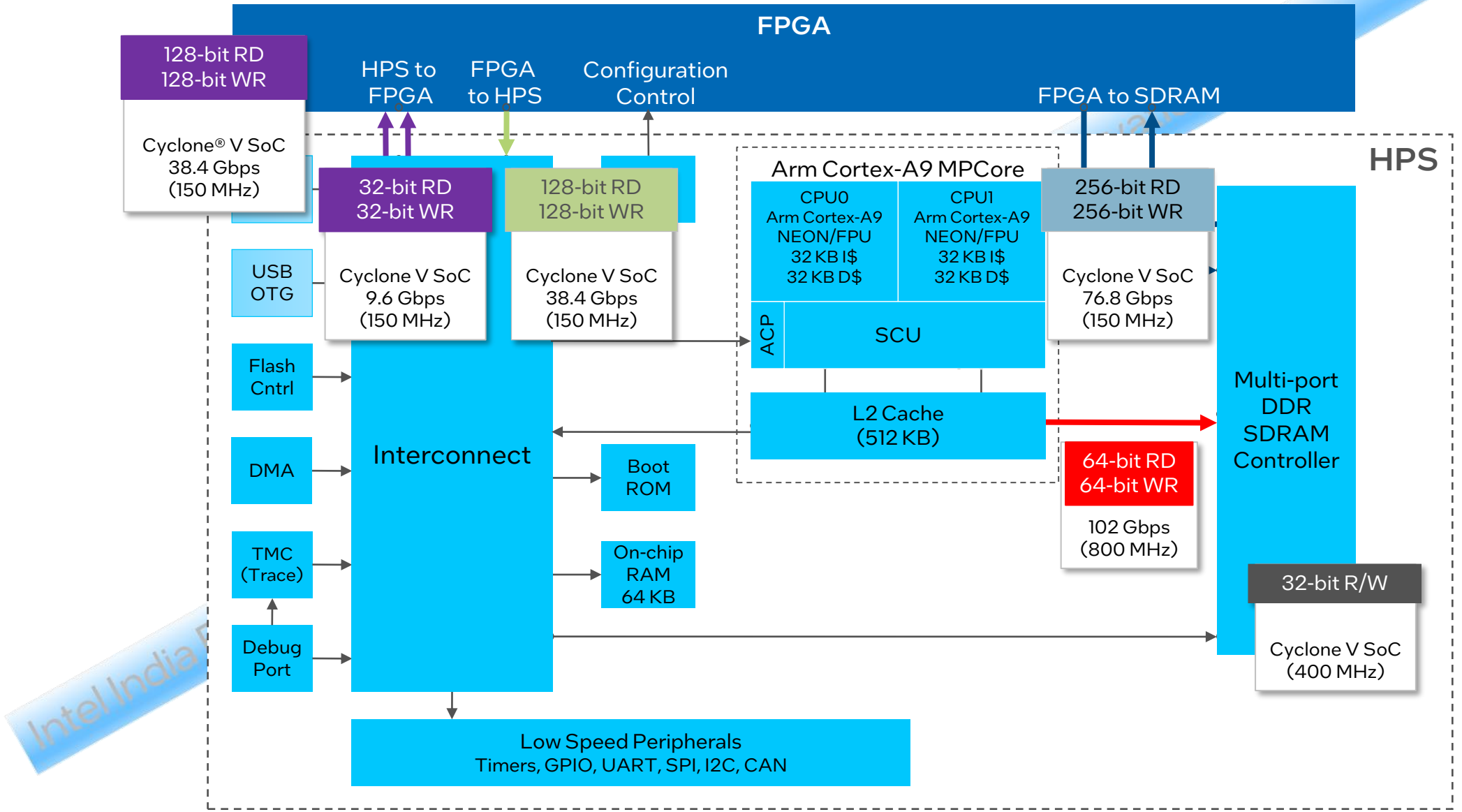
# HPS Architecture Deep Dive

Cyclone V SoC FPGA

# High-Level Block Diagram

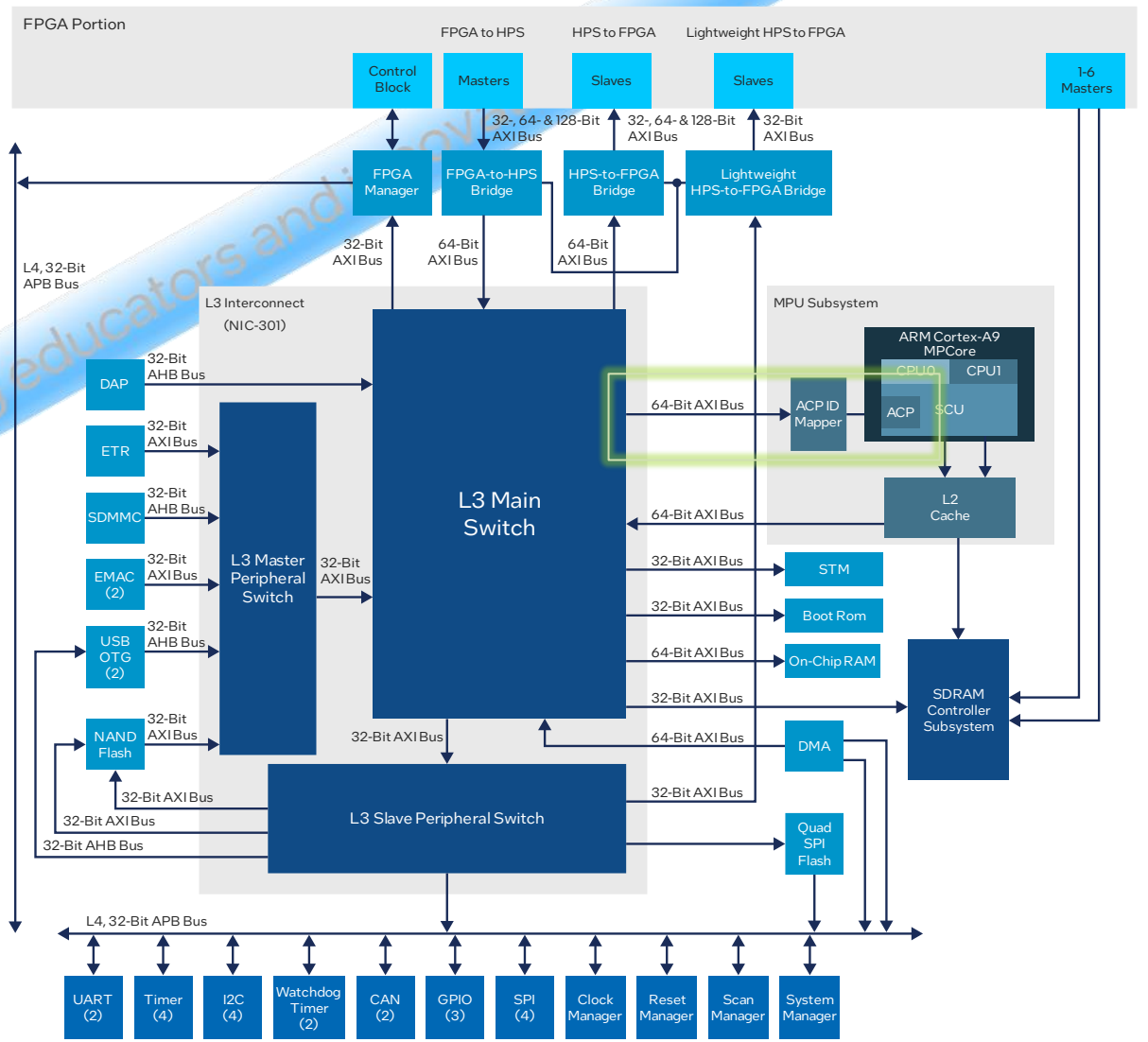


# System Throughput



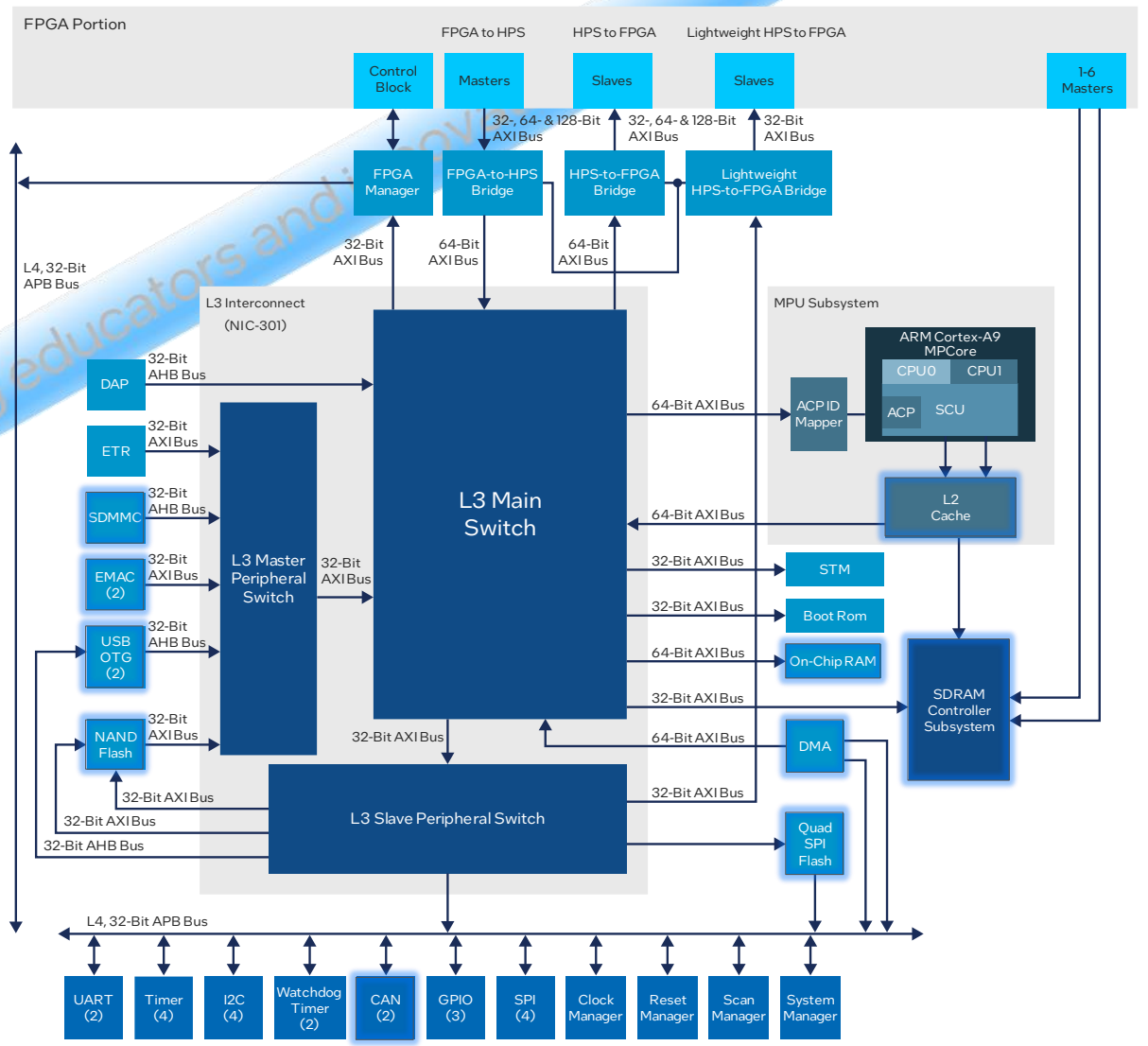
# Coherent Memory Sharing

- Coherent memory support for *all* masters
  - FPGA and HPS
- ACP Mapper removes 8-master limit
  - Up to 8 transactions in flight
  - Unlimited transactions pending
- High bandwidth
  - 64-bit port running at ½ CPU clock



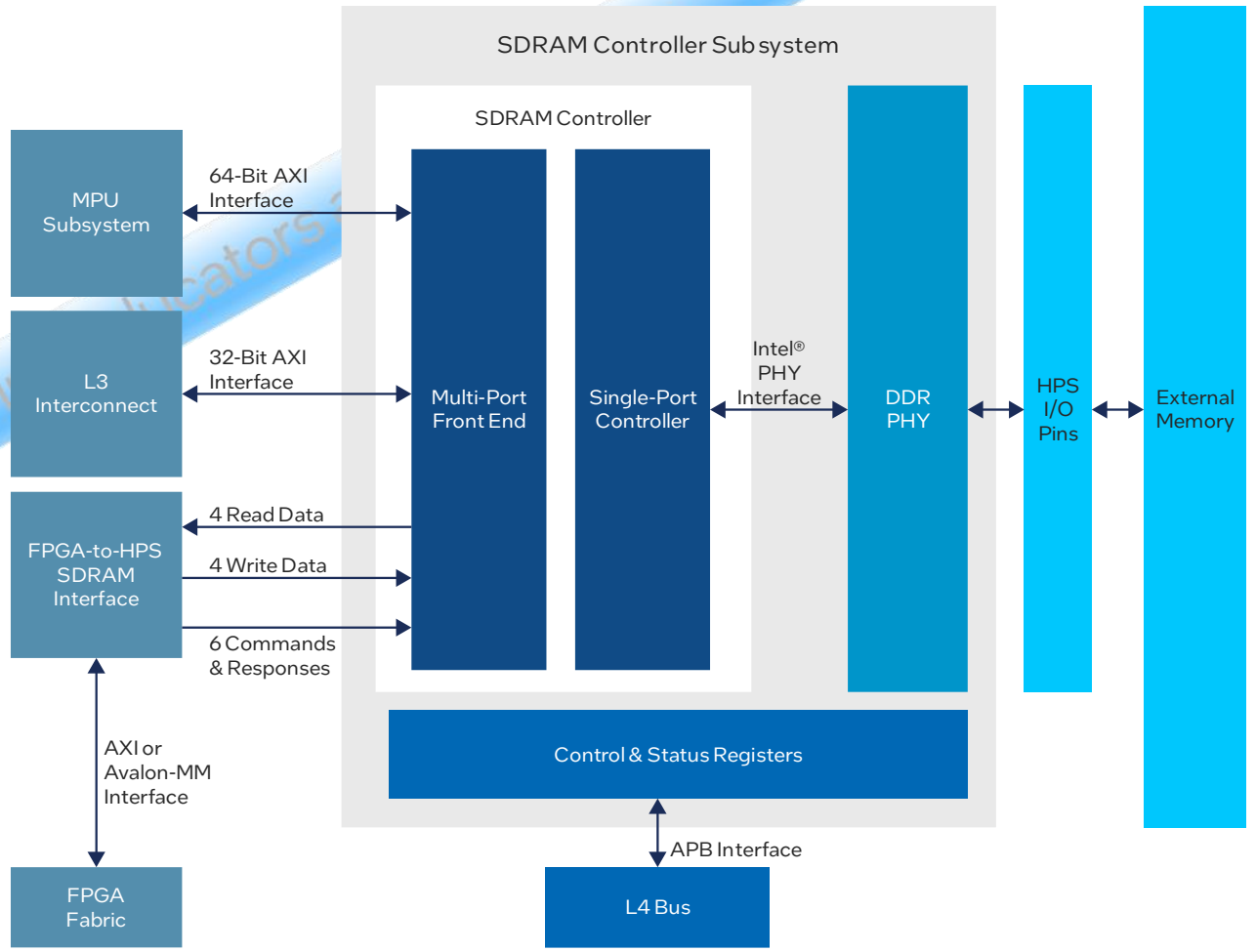
# Memory Protection: ECC Support

- DDR controller (16-bit, 32-bit)
- L2 cache
- On-chip RAM
- QSPI, SD/MMC, NAND
- Direct memory access (DMA)
- USB, EMAC, CAN



# HPS DDR Memory Controller

- One 64-bit AXI port for CPU
- One 32-bit AXI port for L3
- Up to six ports shared with FPGA
  - Six CMD ports
  - Four 64-bit RD ports
  - Four 64-bit WR ports
- Direct connection (no switch)
- Variable DRAM port width
  - 8-bit
  - 16-bit, 16-bit + ECC
  - 32-bit, 32-bit + ECC
- Up to 4 GB of address map for DDR
- TrustZone regions: 1MB boundaries



# FPGA to HPS SDRAM Port Utilization

- Port Configuration
  - Up to 4 Read Ports
  - Up to 4 Write Ports
  - Up to 6 Command Ports
- Example:

| Protocol | Command | Read | Write |
|---|---|---|---|
| 64-bit AXI | 2 | 1 | 1 |
| 128-bit AXI | 2 | 2 | 2 |
| 32-bit Avalon® memory mapped interface | 1 | 1 | 1 |
| Total | 5 | 4 | 4 |

| Bus Protocol | Command | Read Data | Write Data |
|---|---|---|---|
| 8-, 16-, 32-, and 64-bit AXI | 2 (1) | 1 | 1 |
| 128-bit AXI | 2 (1) | 2 (2) | 2 (2) |
| 256-bit AXI | 2 (1) | 4 (2) | 4 (2) |
| 32- and 64-bit Avalon-MM | 1 | 1 | 1 |
| 128-bit Avalon-MM | 1 | 2 | 2 |
| 256-bit Avalon-MM | 1 | 4 | 4 |
| 32- and 64-bit Avalon-MM write-only | 1 | 0 | 1 |
| 128-bit Avalon-MM write-only | 1 | 0 | 2 |
| 256-bit Avalon-MM write-only | 1 | 0 | 4 |
| 32- and 64-bit Avalon-MM read-only | 1 | 1 | 0 |
| 128-bit Avalon-MM read-only | 1 | 2 | 0 |
| 256-bit Avalon-MM read-only | 1 | 4 | 0 |

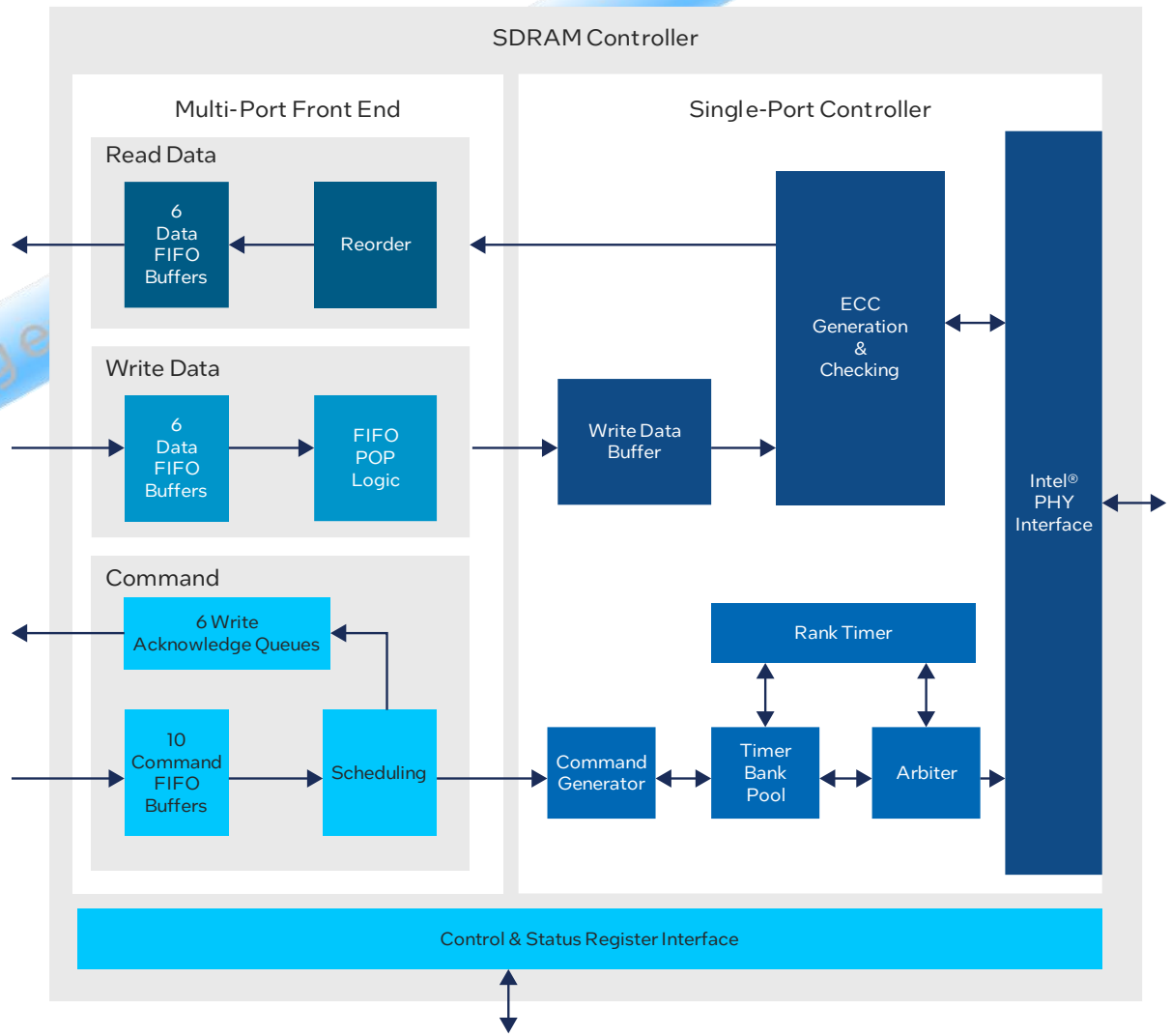
**Note to Table 8–2:**

(1) Because the AXI protocol allows simultaneous read and write commands to be issued, two SDRAM control ports are required to form an AXI interface.

(2) Because the native size of the data ports is 64 bits, extra read and write ports are required to form an AXI interface.

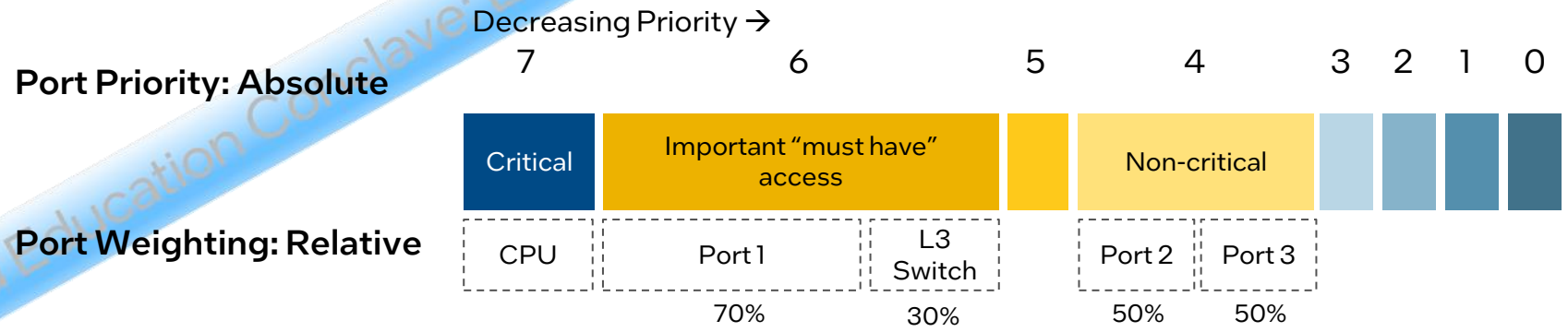
# DDR Memory Controller Features

- Relative port priority (deficit-weighted round robin)
- Absolute priority (multi-level)
- Priority by-pass
- ECC (16-bit, 32-bit)
- Bank management (+ hint)
- Command reordering
- Power management
- TrustZone security
- Exclusive memory sharing
- Memory protection



# Multiport Scheduling: Fine Granularity

- Absolute priority
  - Ports are assigned an absolute priority level (0 – 7)
  - The highest priority port transactions are always served first
  - Absolute port priority can be changed dynamically
  - Absolute priority can be assigned to any FPGA *transaction* dynamically
- Relative priority for ports with the same absolute priority
  - Deficit-weighted round robin - allocates bandwidth per port, avoids bandwidth starvation

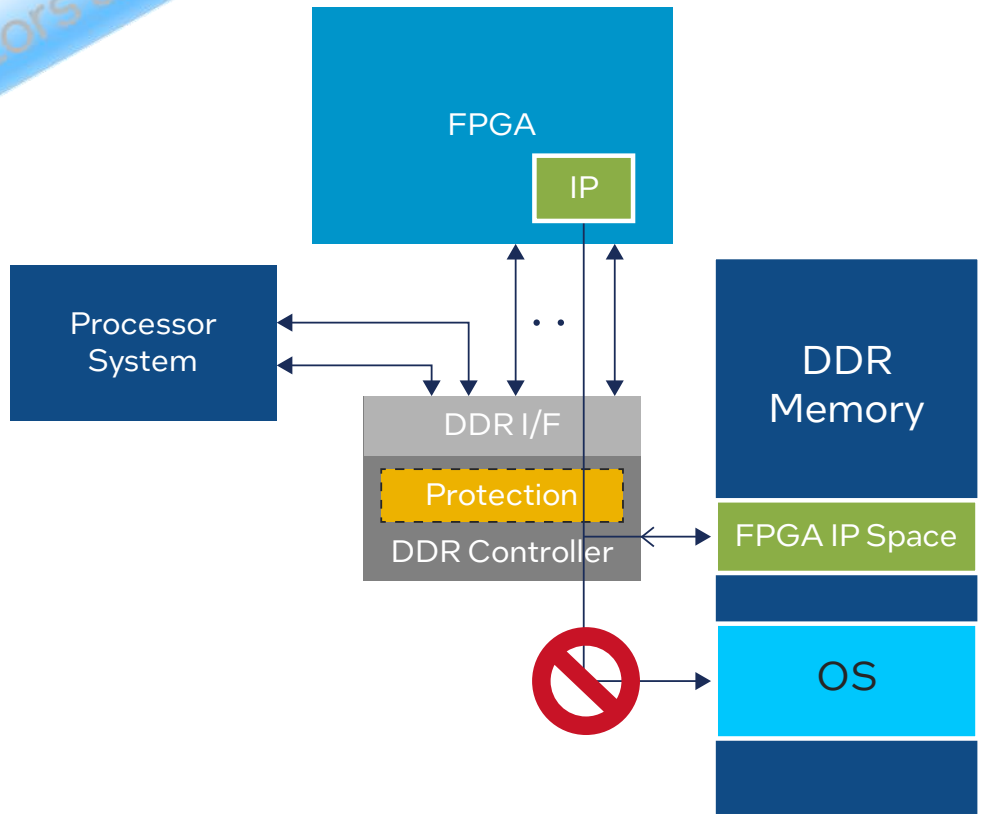



Typical Use Case:

- One port assigned to the highest priority (e.g. CPU)
- Multiple ports can share the same absolute priority
- Port weighting determines bandwidth % for ports sharing the same priority

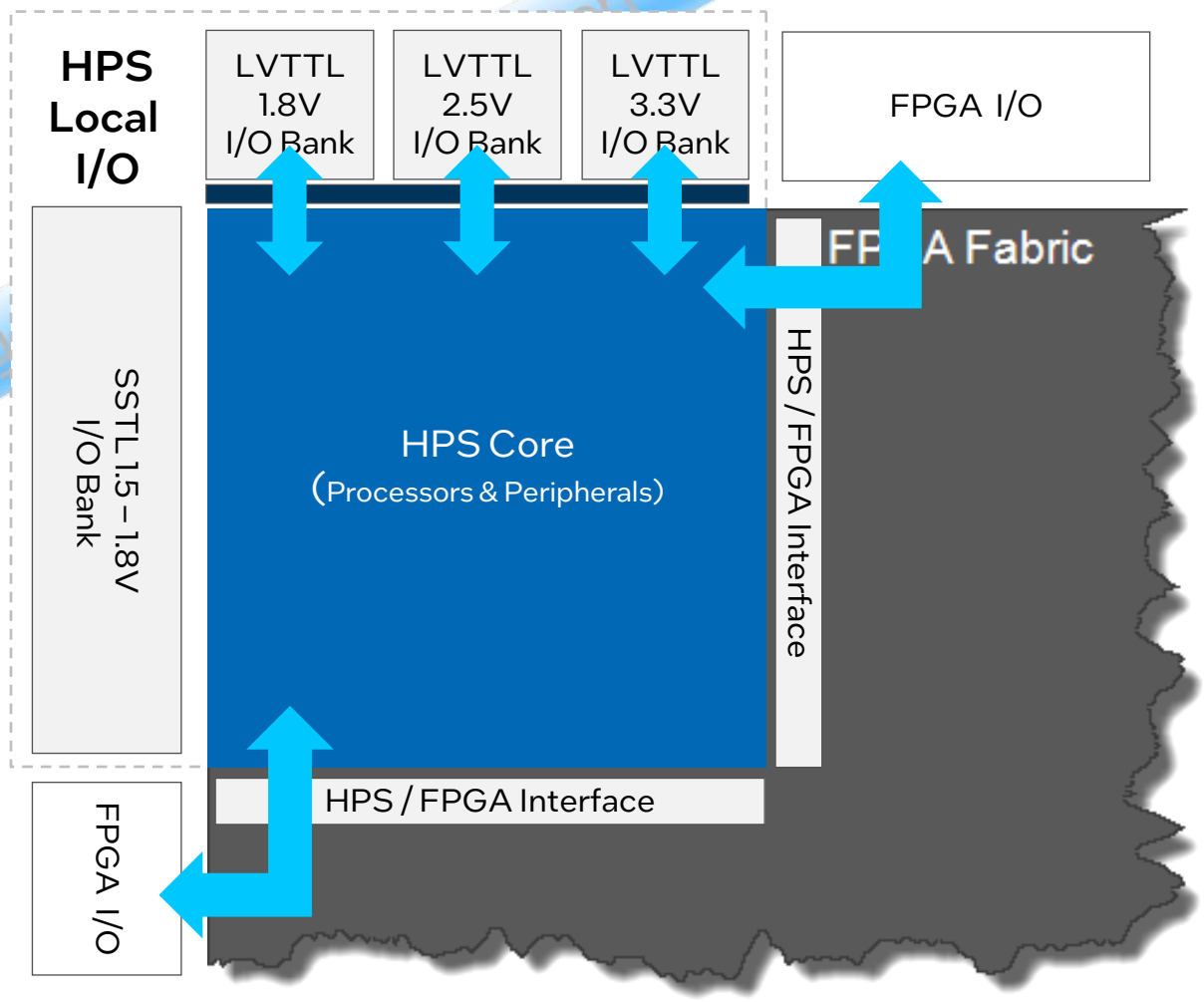
# Memory Protection for Shared DRAM

- Protects DDR memory regions by port and master ID
  - Keeps masters from accessing memory regions they shouldn't
  - Like a MPU for the DDR controller
- 20 protection rules supported
  - Setting for each rule
    - Protection enable (on / off)
    - Address range (high / low)
    - Master ID range (high / low)
    - Port range (mask)
    - TrustZone secure transaction (on / off)
    - Protection type (exclusive / inclusive)



# CPU and FPGA I/O

- A portion of device I/O are allocated to the HPS
  - Some are dedicated to DDR
  - Others can be assigned to HPS peripherals
- HPS peripheral signals can be routed into the FPGA to share FPGA I/O, such as:
  - UART, SPI, I2C
  - Ethernet
- Low speed signals from FPGA logic can use HPS I/O



# User-Specified Peripheral Use

- Non-DDR I/O pins in the HPS can be assigned to one of several functions
  - For example, HPS_BANK_2_2 can be:
    - NAND
    - Ethernet
    - USB
    - GPIO
    - "Loaned" to FPGA
- Some HPS peripherals can be routed into the FPGA
  - Ethernet, I2C, UART, SPI, CAN
  - Trace

| HPS I/O Bank | Opt 1 | Opt 2 | Opt 3 | GPIO | From FPGA |
|---|---|---|---|---|---|
| HPS_BANK0_0 | EMAC0 | | | GPIO0 | LOANIO0 |
| HPS_BANK0_1 | | USB1 Data 0-3 | | GPIO1 | LOANIO1 |
| HPS_BANK0_2 | | | | GPIO2 | LOANIO2 |
| HPS_BANK0_3 | | | | GPIO3 | LOANIO3 |
| HPS_BANK0_4 | | | | GPIO4 | LOANIO4 |
| HPS_BANK0_5 | | USB1 Data 4-7 | | GPIO5 | LOANIO5 |
| HPS_BANK0_6 | | | I2C_2 | GPIO6 | LOANIO6 |
| HPS_BANK0_7 | | | | GPIO7 | LOANIO7 |
| HPS_BANK0_8 | | | | GPIO8 | LOANIO8 |
| HPS_BANK0_9 | | | | GPIO9 | LOANIO9 |
| HPS_BANK0_10 | | USB1 Control | | GPIO10 | LOANIO10 |
| HPS_BANK0_11 | | | | GPIO11 | LOANIO11 |
| HPS_BANK0_12 | | | | GPIO12 | LOANIO12 |
| HPS_BANK0_13 | | | | GPIO13 | LOANIO13 |
| HPS_BANK2_0 | | EMAC1 | QSPI SS3 | GPIO14 | LOANIO14 |
| HPS_BANK2_1 | | | | GPIO15 | LOANIO15 |
| HPS_BANK2_2 | | | USB1 Data 0-3 | GPIO16 | LOANIO16 |
| HPS_BANK2_3 | | | | GPIO17 | LOANIO17 |
| HPS_BANK2_4 | | | | GPIO18 | LOANIO18 |
| HPS_BANK2_5 | | | | GPIO19 | LOANIO19 |
| HPS_BANK2_6 | | | I2C_3 | GPIO20 | LOANIO20 |
| HPS_BANK2_7 | NAND | | | GPIO21 | LOANIO21 |
| HPS_BANK2_8 | | | | GPIO22 | LOANIO22 |
| HPS_BANK2_9 | | | USB1 Data 4-7 | GPIO23 | LOANIO23 |
| HPS_BANK2_10 | | | | GPIO24 | LOANIO24 |
| HPS_BANK2_11 | | | | GPIO25 | LOANIO25 |
| HPS_BANK2_12 | | | | GPIO26 | LOANIO26 |
| HPS_BANK2_13 | | | QSPI SS2 | GPIO27 | LOANIO27 |
| HPS_BANK2_14 | | | QSPI SS1 | GPIO28 | LOANIO28 |
| HPS_BANK2_15 | QSPI Control & SS0 | | USB1 Control | GPIO29 | LOANIO29 |
| HPS_BANK2_16 | | | | GPIO30 | LOANIO30 |
| HPS_BANK2_17 | | | | GPIO31 | LOANIO31 |
| HPS_BANK2_18 | | | | GPIO32 | LOANIO32 |
| HPS_BANK2_19 | | | | GPIO33 | LOANIO33 |
| HPS_BANK2_20 | | | | GPIO34 | LOANIO34 |
| HPS_BANK2_21 | QSPI SS1 | | | GPIO35 | LOANIO35 |

| HPS I/O Bank | Opt 1 | Opt 2 | Opt 3 | GPIO | From FPGA |
|---|---|---|---|---|---|
| HPS_BANK3_0 | SDMMC | USB0 Data 0-3 | | GPIO36 | LOANIO36 |
| HPS_BANK3_1 | | | | GPIO37 | LOANIO37 |
| HPS_BANK3_2 | | | | GPIO38 | LOANIO38 |
| HPS_BANK3_3 | | | | GPIO39 | LOANIO39 |
| HPS_BANK3_4 | SDMMC Data 4-7 | USB0 Data 4-7 | | GPIO40 | LOANIO40 |
| HPS_BANK3_5 | | | | GPIO41 | LOANIO41 |
| HPS_BANK3_6 | | | | GPIO42 | LOANIO42 |
| HPS_BANK3_7 | | | | GPIO43 | LOANIO43 |
| HPS_BANK3_8 | SDMMC | USB0 Control | | GPIO44 | LOANIO44 |
| HPS_BANK3_9 | | | | GPIO45 | LOANIO45 |
| HPS_BANK3_10 | | | | GPIO46 | LOANIO46 |
| HPS_BANK3_11 | | | | GPIO47 | LOANIO47 |
| HPS_BANK4_0 | TRACE Clk & Data 0-3 | | | GPIO51 | LOANIO48 |
| HPS_BANK4_1 | | SPIS0 | UART0 | GPIO52 | LOANIO49 |
| HPS_BANK4_2 | | | | GPIO53 | LOANIO50 |
| HPS_BANK4_3 | | | I2C_1 | GPIO54 | LOANIO51 |
| HPS_BANK4_4 | | | | GPIO55 | LOANIO52 |
| HPS_BANK4_5 | TRACE Data 4-7 | SPIS1 | CAN1 | GPIO56 | LOANIO53 |
| HPS_BANK4_6 | | | | GPIO57 | LOANIO54 |
| HPS_BANK4_7 | | | I2C0 | GPIO58 | LOANIO55 |
| HPS_BANK4_8 | | | | GPIO59 | LOANIO56 |
| HPS_BANK4_9 | SPIM0 | UART0 CTS/RTS | I2C_1 | GPIO60 | LOANIO57 |
| HPS_BANK4_10 | | | | GPIO61 | LOANIO58 |
| HPS_BANK4_11 | | UART1 CTS/RTS | CAN1 | GPIO62 | LOANIO59 |
| HPS_BANK4_12 | | | | GPIO63 | LOANIO60 |
| HPS_BANK4_13 | SPIM0 SS1 | UART0 | CAN0 | GPIO64 | LOANIO61 |
| HPS_BANK4_14 | SPIM1 SS1 | | | GPIO65 | LOANIO62 |
| HPS_BANK4_15 | SPIM1 | UART1 | I2C0 | GPIO66 | LOANIO63 |
| HPS_BANK4_16 | | | | GPIO67 | LOANIO64 |
| HPS_BANK4_17 | | UART0 | CAN0 | GPIO68 | LOANIO65 |
| HPS_BANK4_18 | | | | GPIO69 | LOANIO66 |

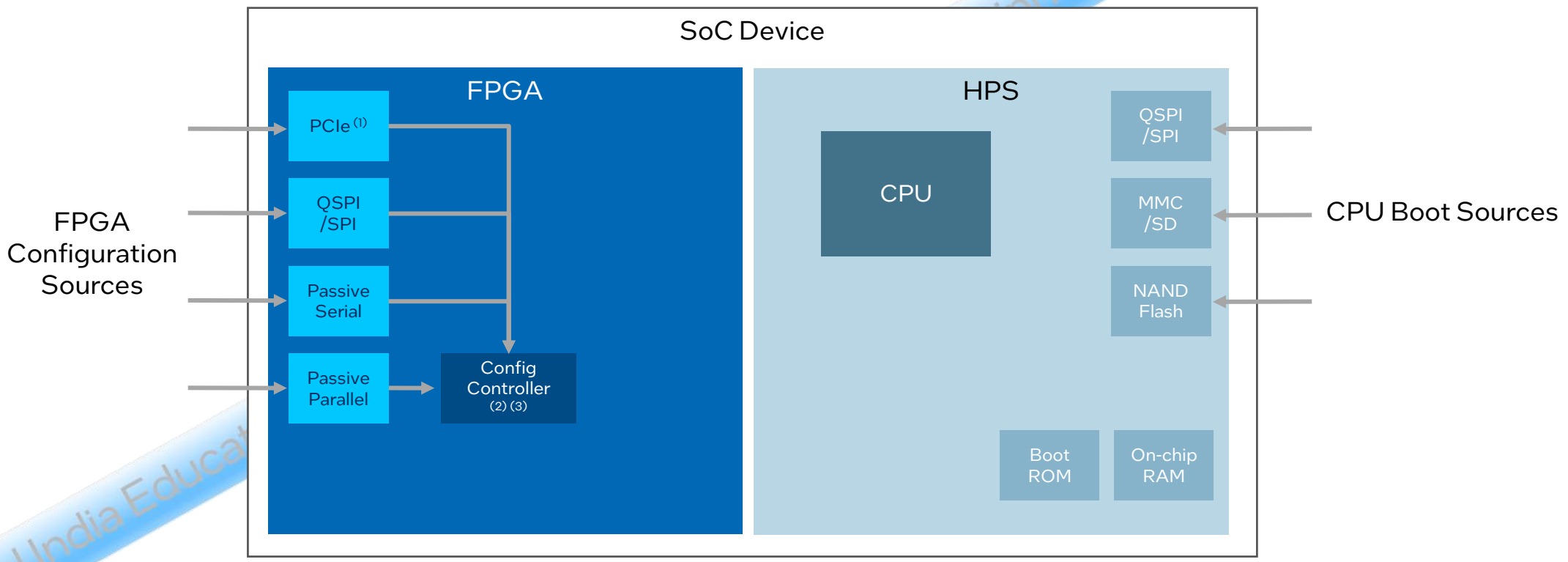
**Can be routed "To FPGA"**

# HPS Configuration

## in Intel SoC FPGAs

# Ultimate Configuration Flexibility

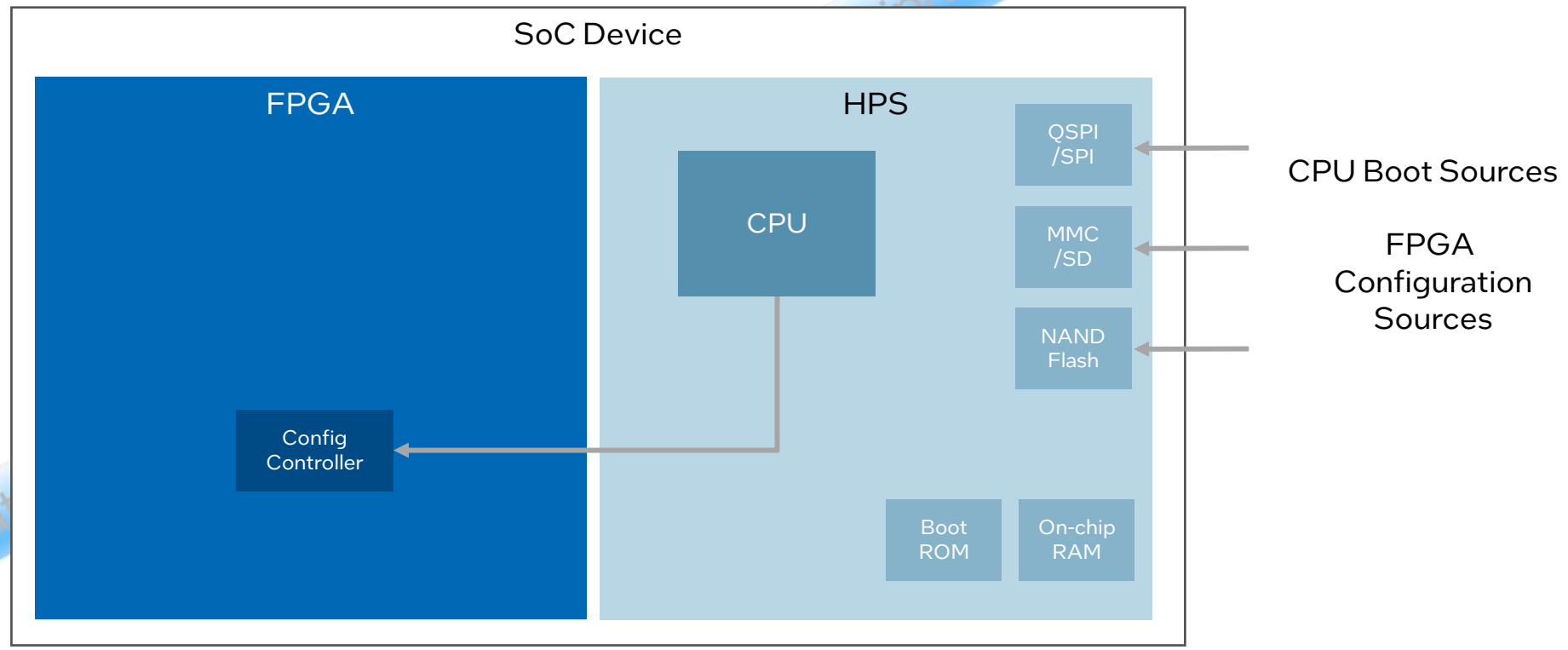
## Independent FPGA configuration and processor boot




(1) Meets the PCIe 100 ms power-up-active time requirement
(2) Supports AES encryption for design security
(3) Supports partial re-configuration

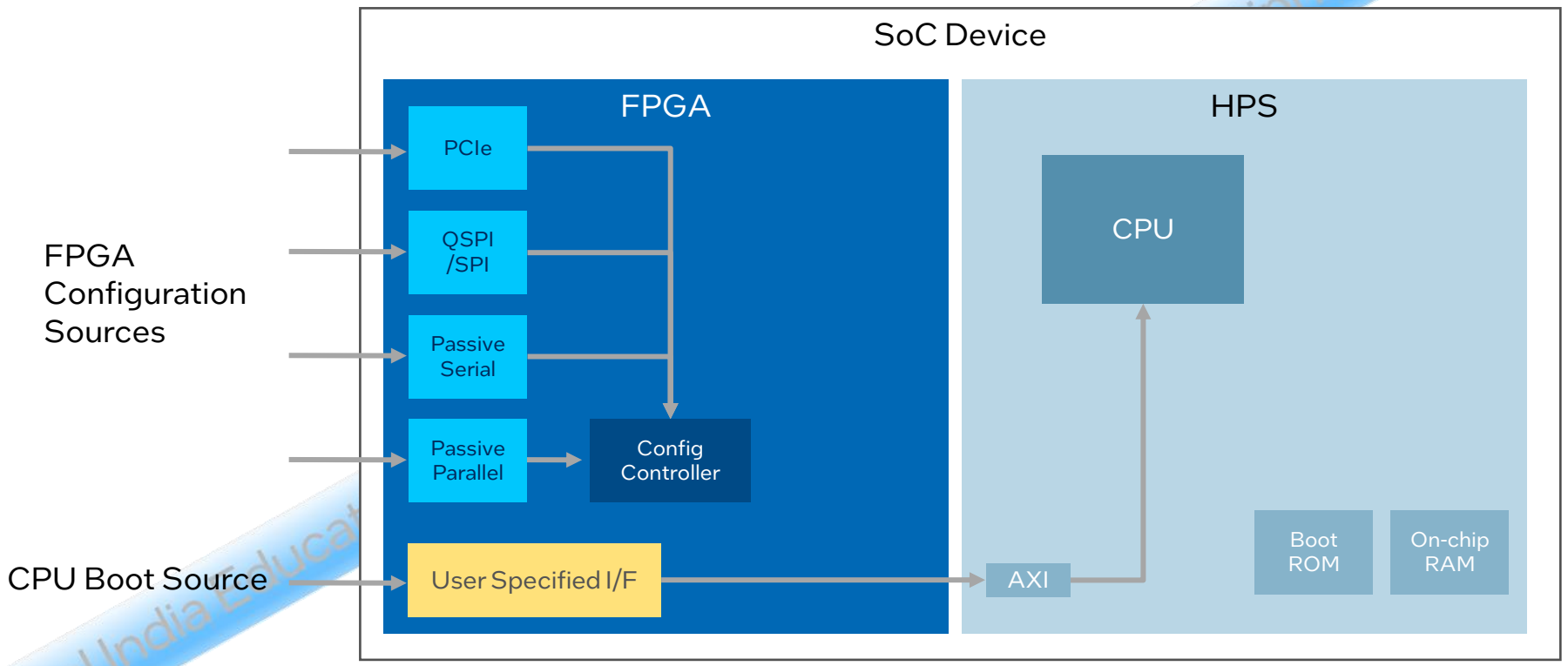
# Ultimate Configuration Flexibility

Processor boots first, then configures the FPGA



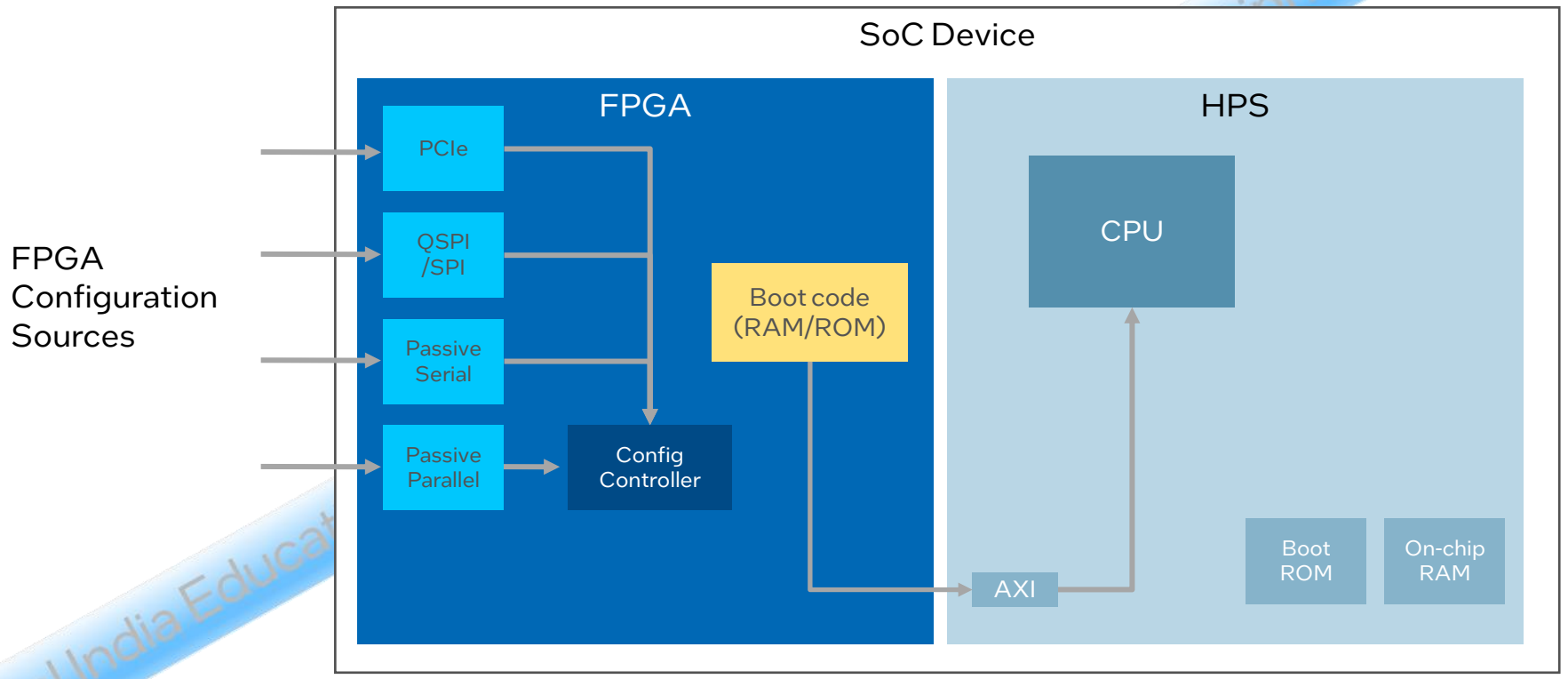
# Ultimate Configuration Flexibility

FPGA configures first, CPU boots through FPGA logic
(e.g. custom backplane I/F)



# Ultimate Configuration Flexibility

FPGA configures first, CPU boots through FPGA logic
(e.g. boot from FPGA memory)



# HPS Booting

## in Intel SoC FPGAs

# Boot Sources

- Specified by physical Boot Select (BSEL) pins
  - Flash Boot
    - NAND, SD/MMC, or QSPI
    - Corresponding CSEL pins determines clock speed of the flash device
  - FPGA Boot (requires the FPGA to be configured first)

| bsel Field Value | Flash Device |
|---|---|
| 0x0 | Reserved |
| 0x1 | FPGA (HPS-to-FPGA bridge) |
| 0x2 | 1.8 V NAND flash memory |
| 0x3 | 3.0 V NAND flash memory |
| 0x4 | 1.8 V SD/MMC flash memory with external transceiver |
| 0x5 | 3.0 V SD/MMC flash memory with internal transceiver |
| 0x6 | 1.8 V SPI or quad SPI flash memory |
| 0x7 | 3.0 V SPI or quad SPI flash memory |







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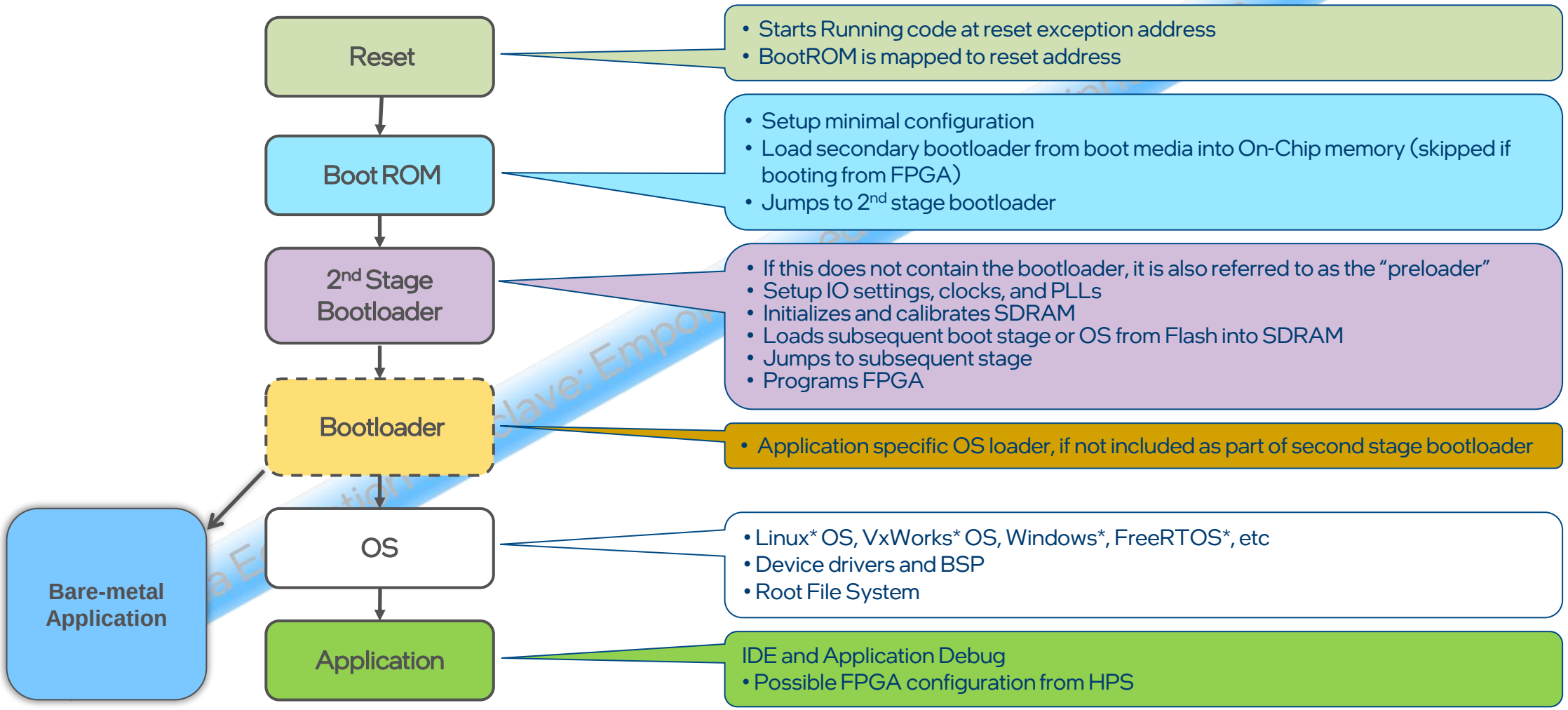
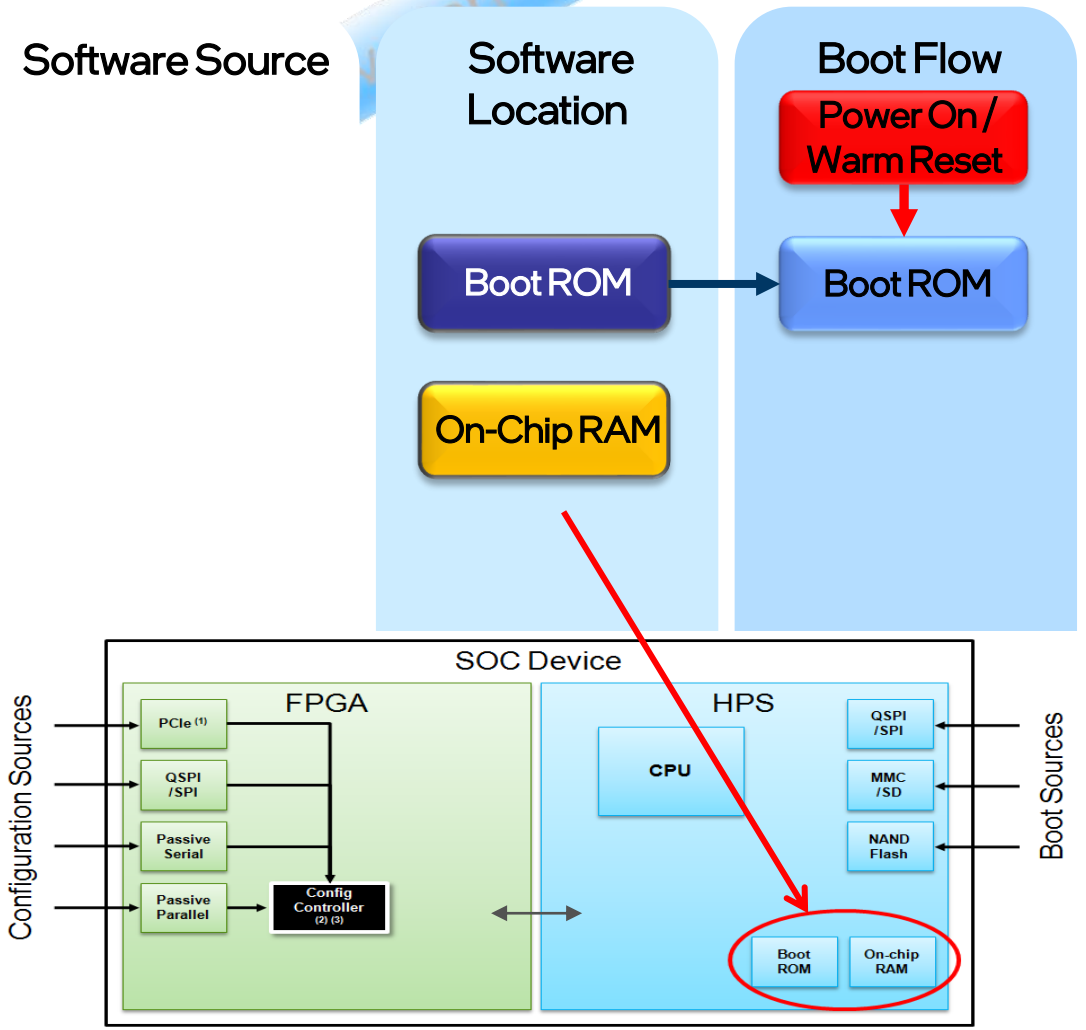
# HPS Typical Boot Stages



# HPS Power On / Reset

- After reset/power up system runs Boot ROM code on CPU0
- CPU1 is held in reset
- Boot ROM code hard programmed as primary bootloader
- Boot ROM code uses On-chip RAM space for data storage







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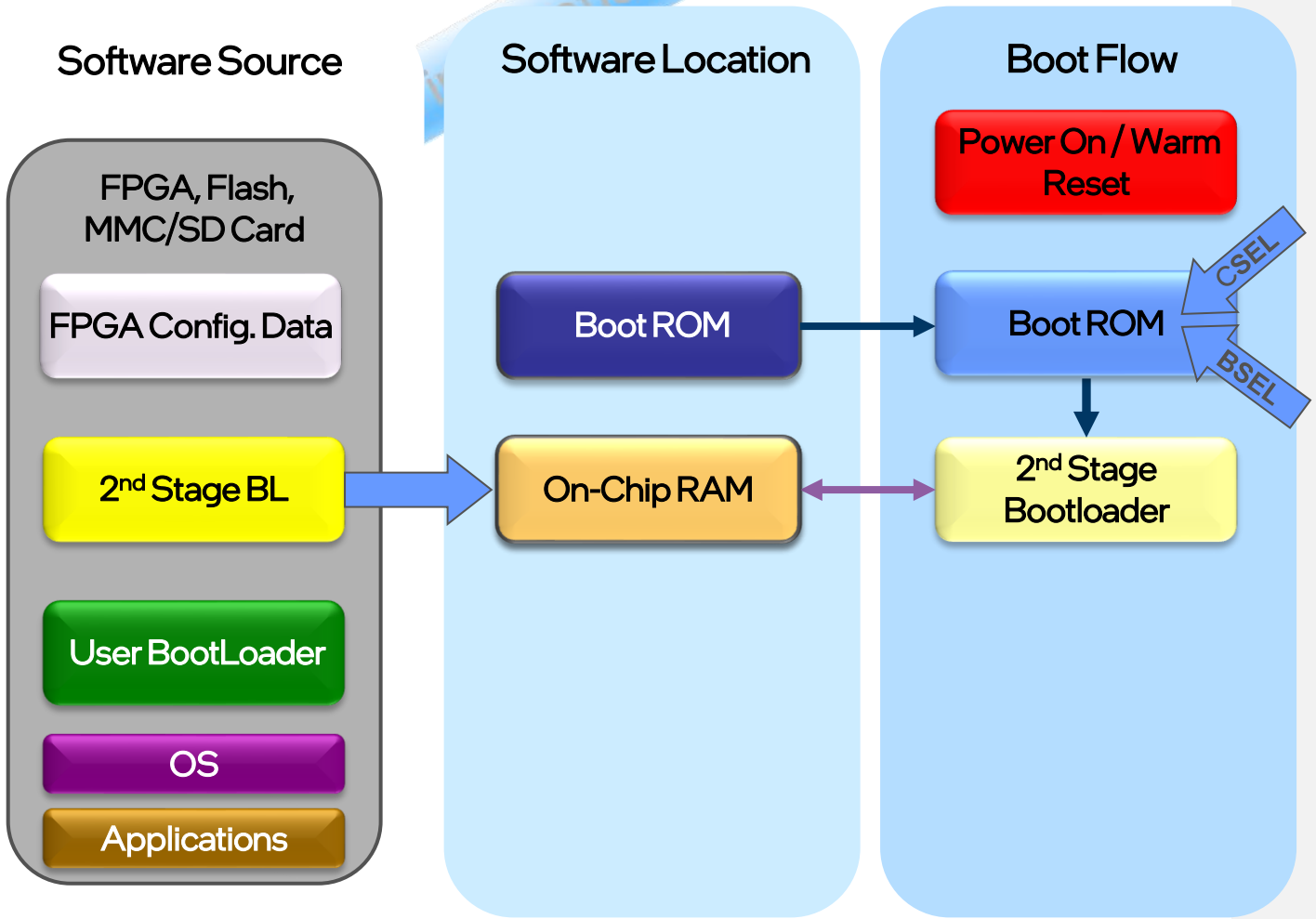
# HPS Boot ROM

- Boot ROM code scans boot-select and clock-select pins to determine flash clock setup and boot source
- Configures minimal set of HPS I/O pins to read boot source using I/O config. data stored in Boot ROM
- Performs CRC check & loads 2nd stage bootloader (Preloader) software from boot source into On-Chip RAM
- Boot ROM hands off program control to the 2nd stage bootloader







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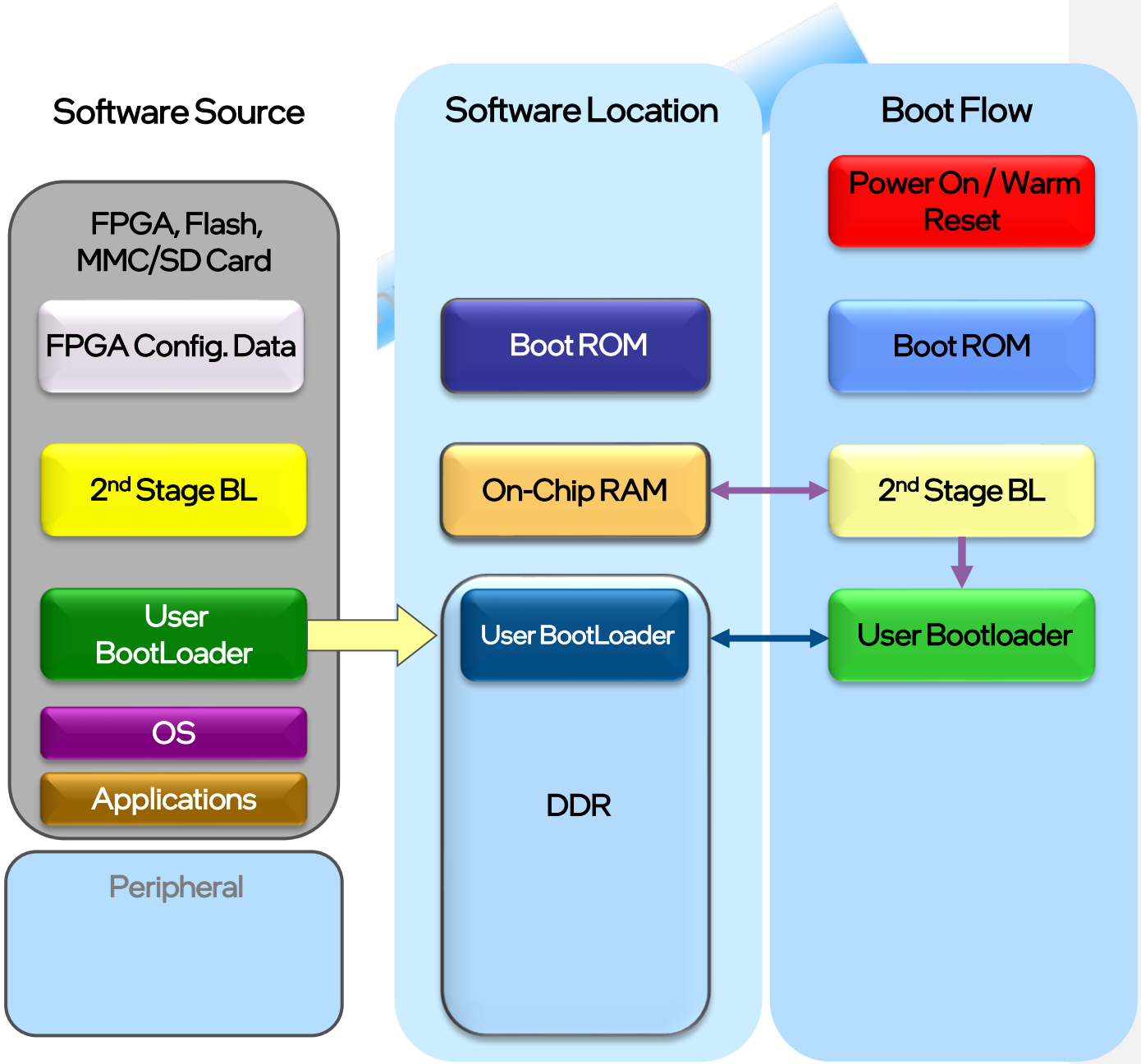
# Second Stage Bootloader

- Referred to as the "Preloader" for Cyclone® V and Arria® V devices
- Built from Qsys handoff files
- Limited by size of On-Chip memory
- HPS I/O and SDRAM configuration data compiled into 2nd Stage Bootloader
- Sets HPS pin configuration
- Initializes, calibrates and verifies SDRAM setup
- Copies next stage software (e.g. U-Boot or OS) into SDRAM from boot source and hands off control to it







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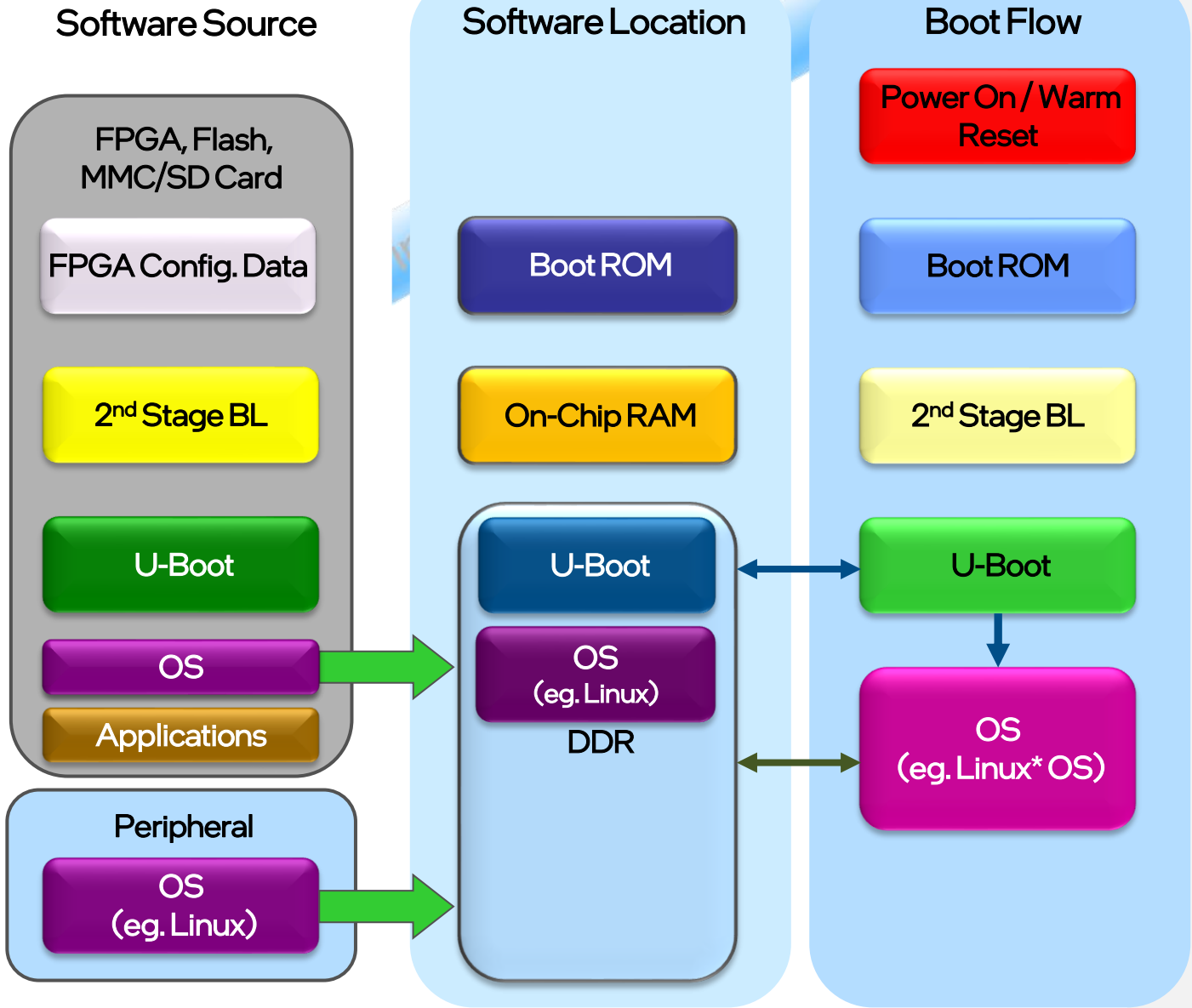
# HPS User Bootloader

- Application/OS specific
- Bootloader Copies Operating System from non-volatile RAM (or Peripheral) to SDRAM
  - Linux* OS, VxWorks* OS, etc
- Runs any other processes specified
- Hands off control to OS
- For Intel® Arria® 10 devices, the functionality of the User Bootloader is built into the 2nd Stage Bootloader









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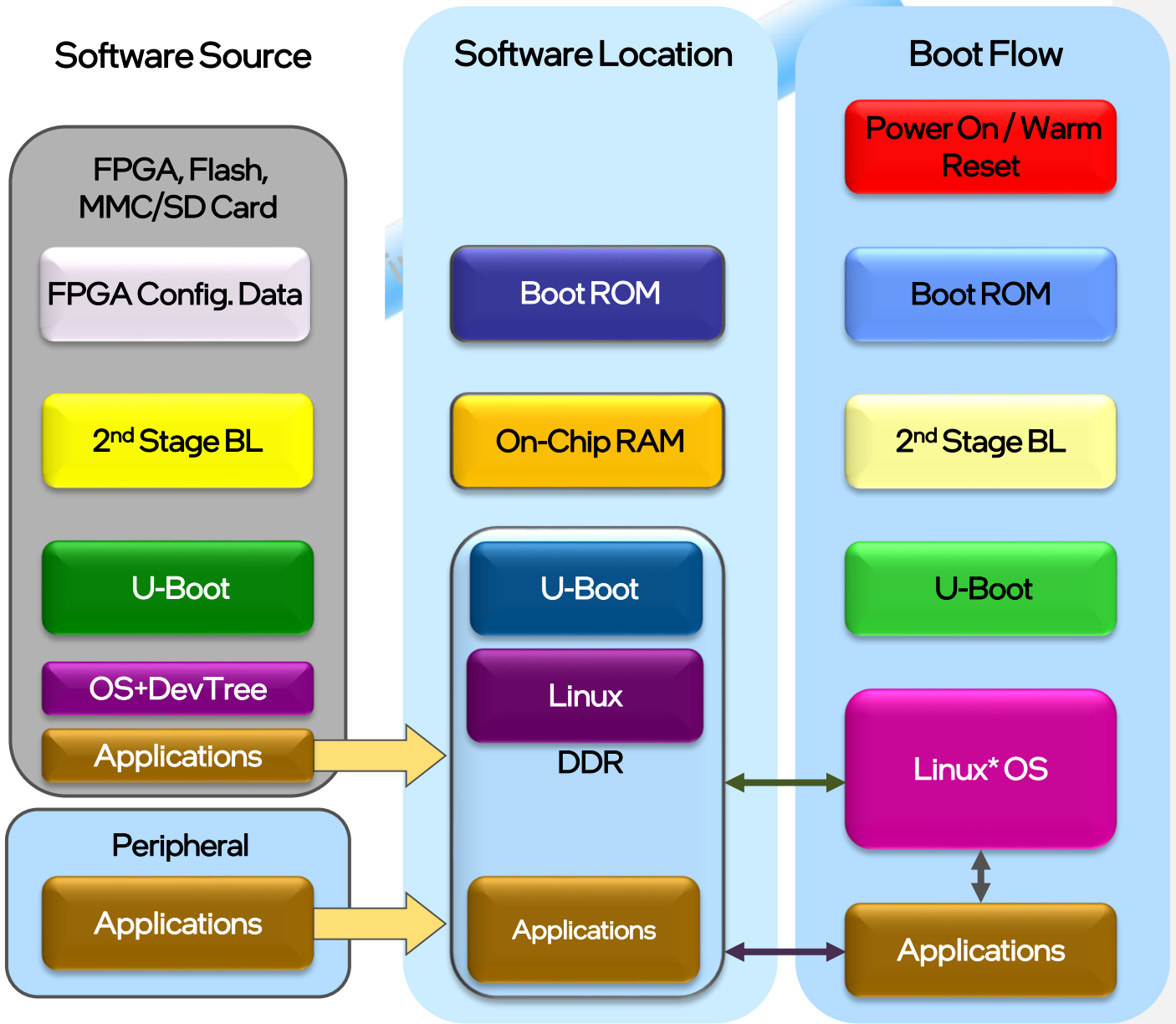
# HPS Linux Start Up

- OS launches
- Runs BSP/device driver initialization routines
  - Processor setup (memory, interrupts etc.)
  - CPU 1 initializes and runs
  - Peripheral hardware setup (detect, verify and initialize)
- Creates OS specific resources
  - e.g. Root File System
- Same OS runs on both processors
- Loads and runs Applications









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# Summary

- SoC FPGAs powered by Intel & ARM
- 54+ variants with Cortex A9, A53, A55, A76 with HPS architectures
- Industry standard Hardware and Software Development Tools and flow
- Ready to start Development kits & solutions
- Several Documents & Community Forum with Rocketboards.org


intel