System on Chip (SoC) Overview

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Moore’s Law ?

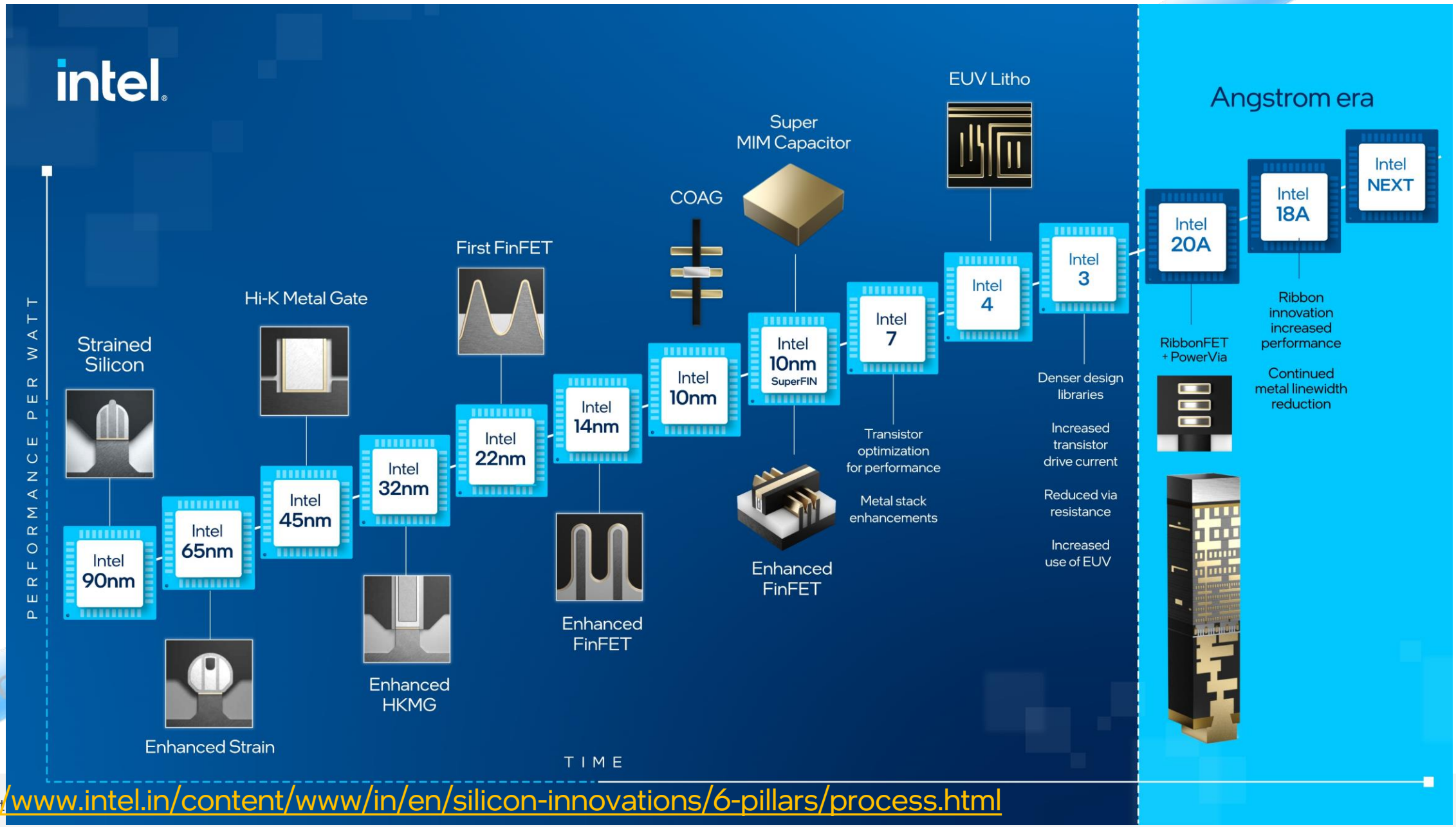
Moore's Law

PPAC value for node scaling every 2-3 years :

- (P)erformance: >10% more operating frequency at scaled supply voltage
- (P)ower: >20% less energy per switching at a given performance
- (A)rea: >30% less chip area footprint
- (C)ost : ~15% less die cost for scaled die

✓ Approx every 18 Months the transistor count double on a chip

Technology Node Roadmap

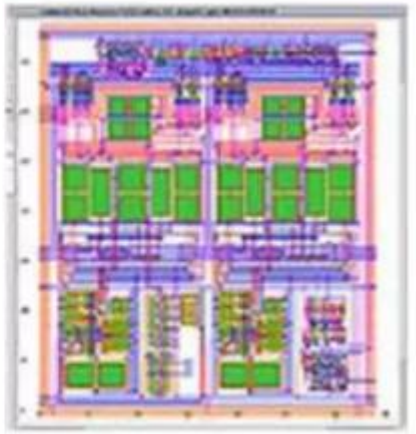


https://www.intel.in/content/www/in/en/silicon-innovations/6-pillars/process.html

Tech leading to SoC

- Technology enables to pack more features on a chip
- Components from the PCB can be integrated on Single Silicon
- Better form factor for different product designs

From PCB to SoC



SoC is everywhere

System on Chip (SoC)

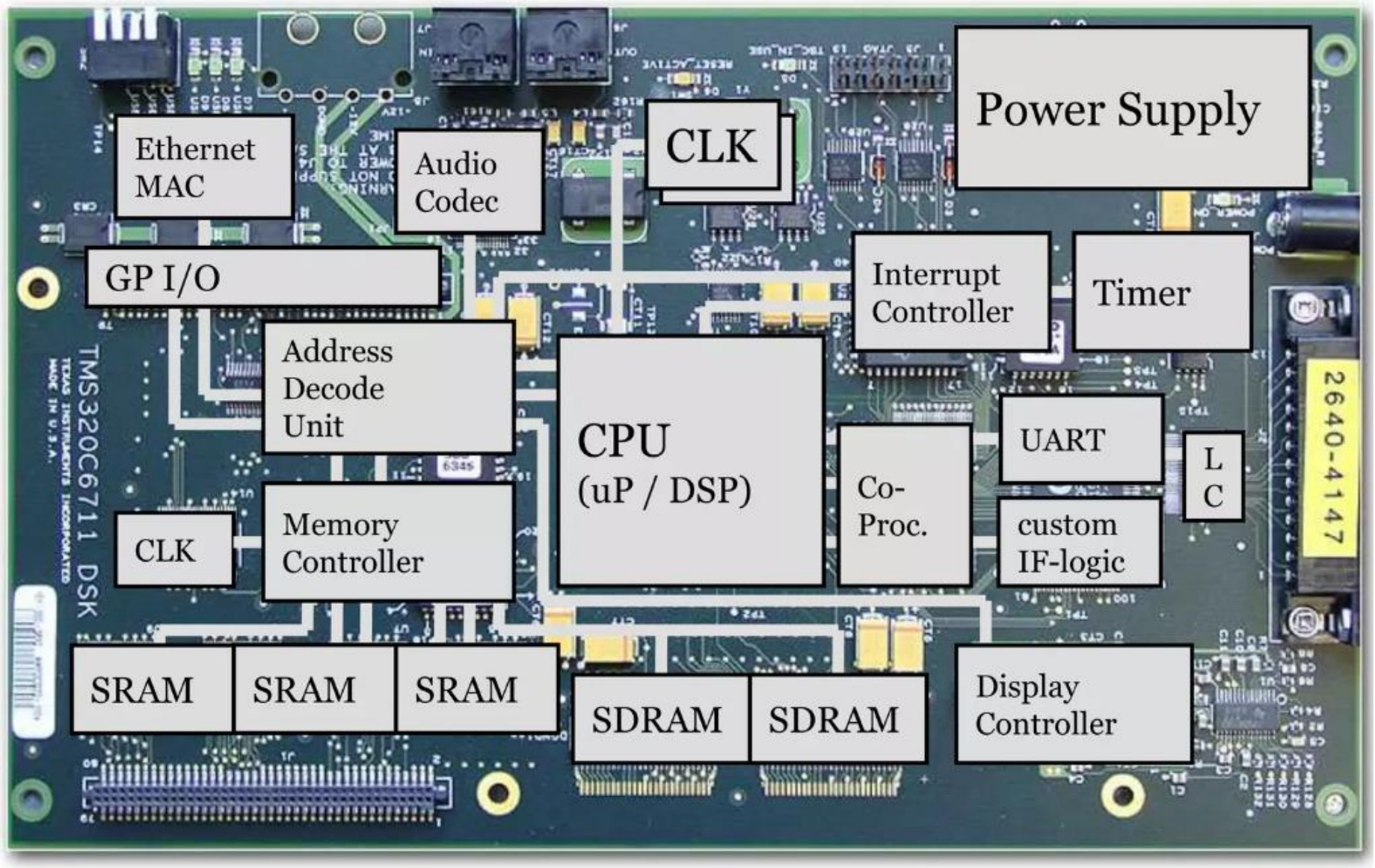
- System on chip

  Definition : (nearly) complete embedded system on a single chip

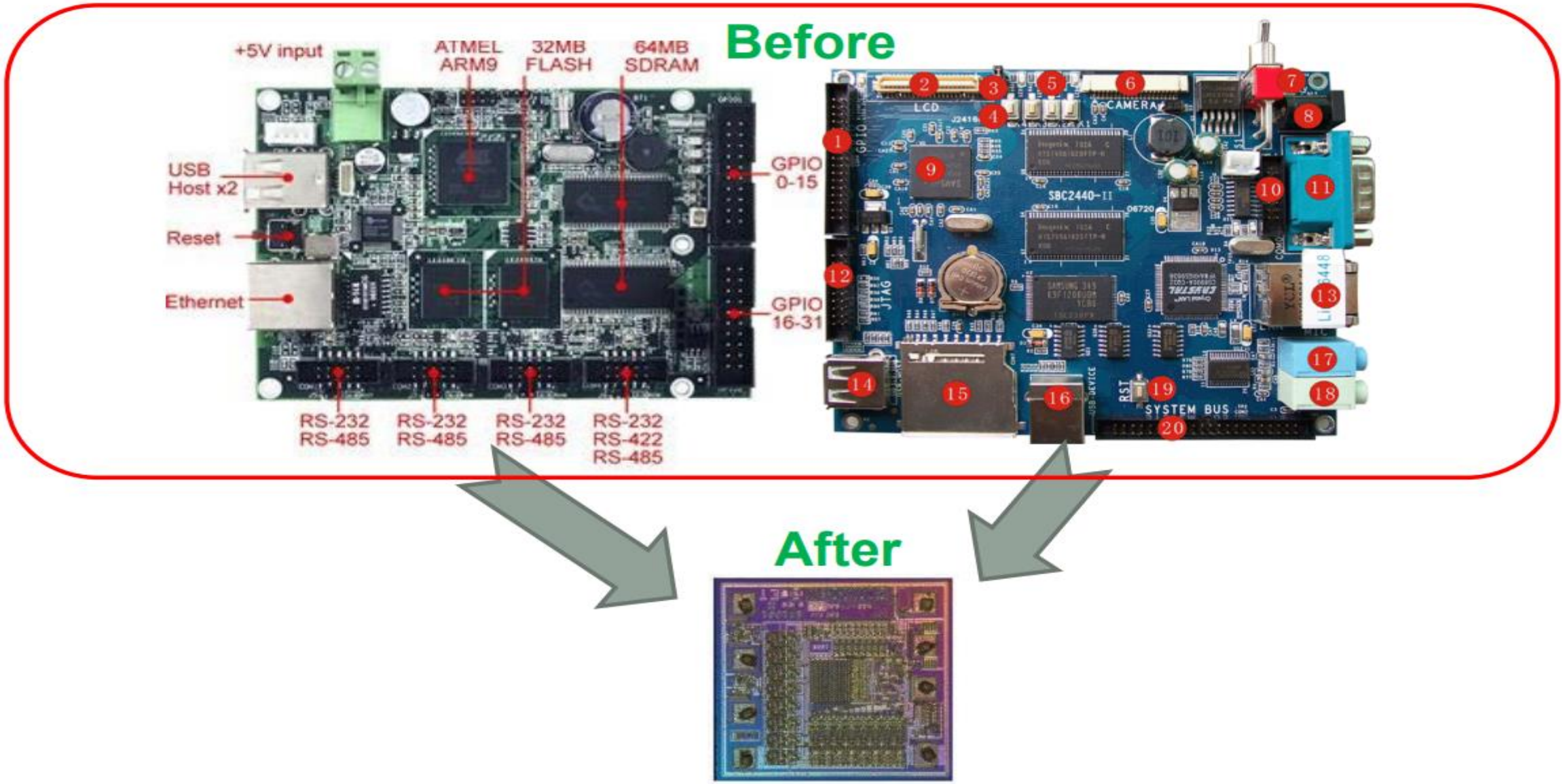
- Usually includes
  - Programmable processor(s)
  - Memory
  - Accelerating function units
  - On-chip interconnection (busses, network, etc.)
  - Input/output interfaces
  - Software
  - Re-usable intellectual property blocks (HW + SW)

✓It's more of a System not a Chip

Traditional Embedded System

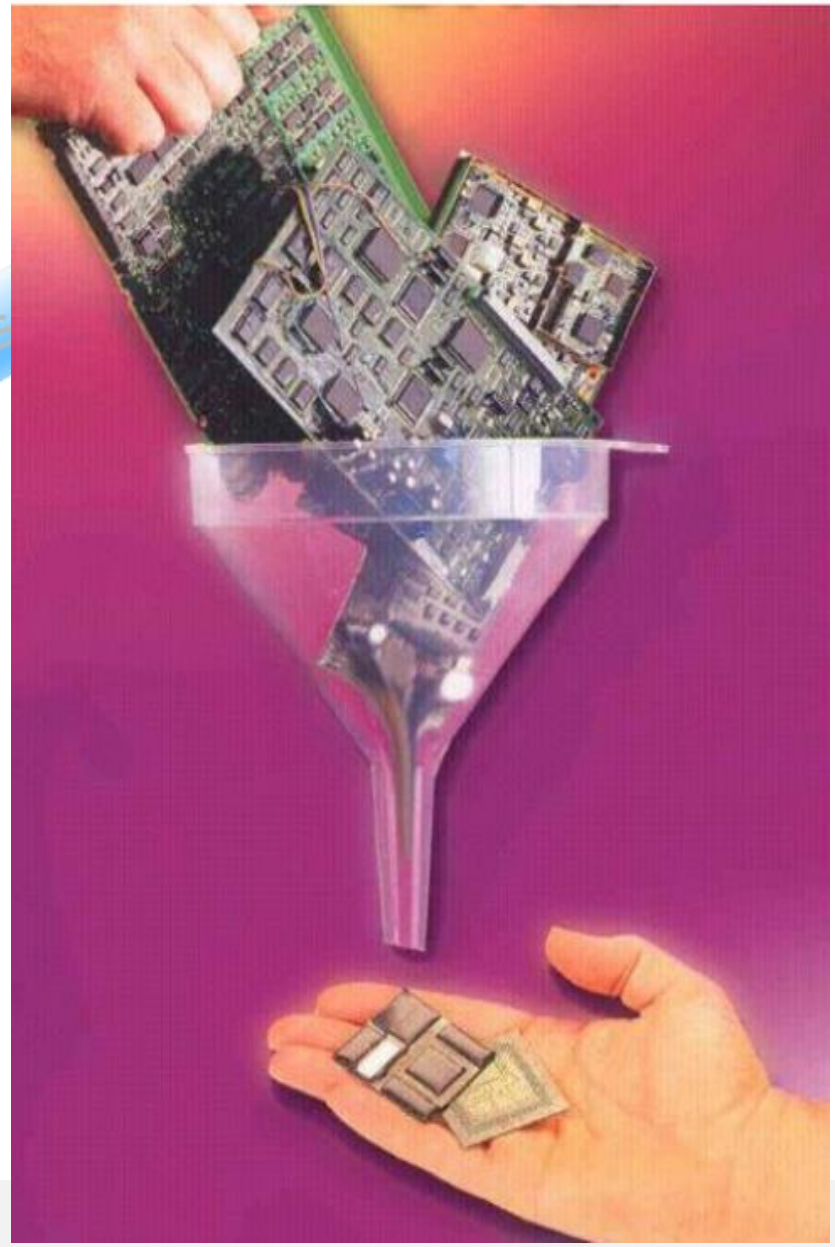


SoC Design Goal



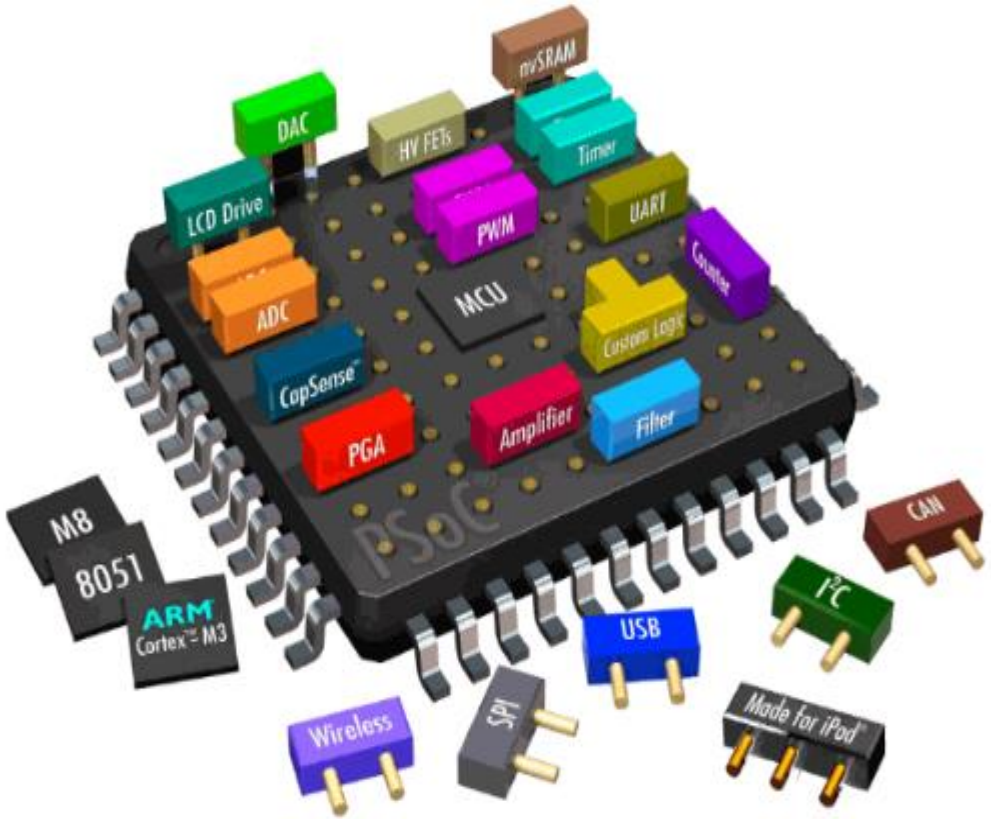
Evolution: Board (PCB) to SoC

- Evolution
  - IP based design
- Challenges/Future
  - HW/SW Co-design
  - IP integration
  - Mixed Design
  - Greater complexity
  - Higher density



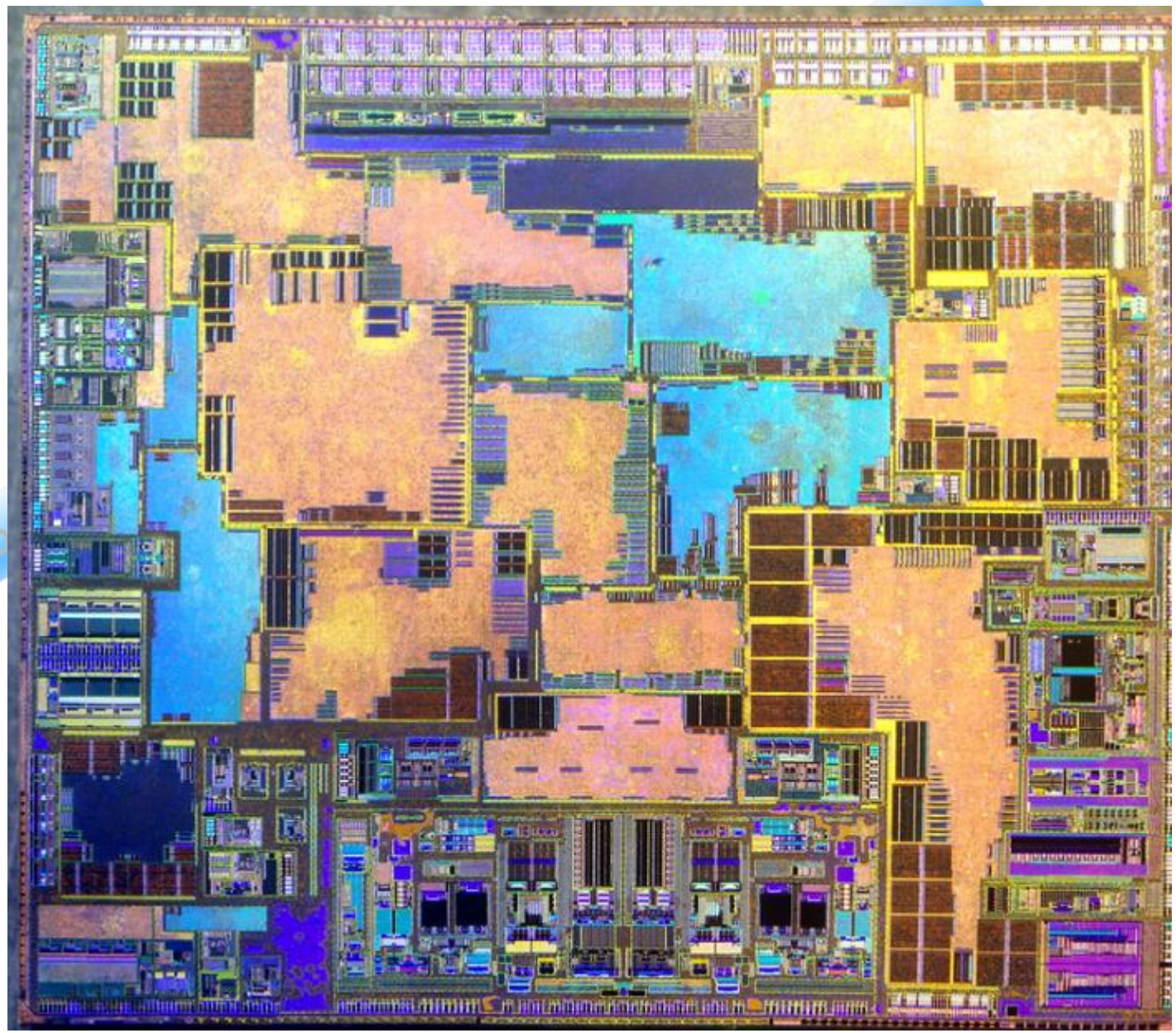
Different types of SoC

- ASIC
  - Application specific IC
  - Very well integrated
  - Yet expensive
- FPGA
  - Cheaper to implement
  - Field programmable
- General Purpose System
  - Off the shelf device
  - Quick to program
  - Low Cost



ASIC SoC

- BCM7019 STB SoC
- Low Power
- Specific use case

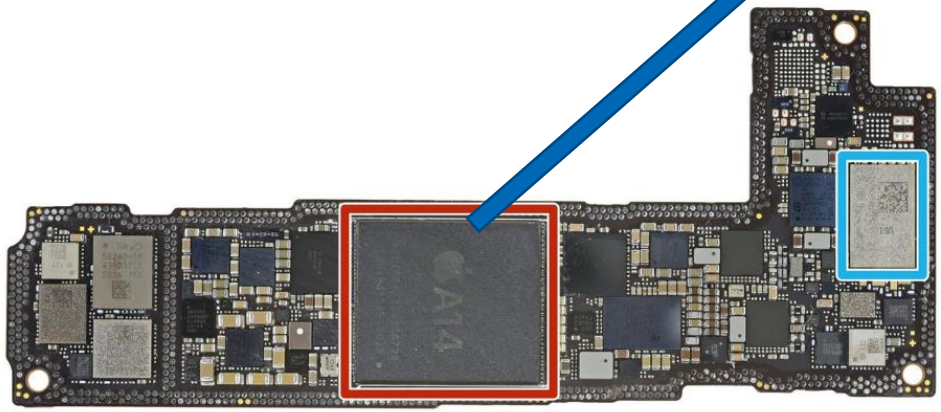


Picture credit : Martijn Boer

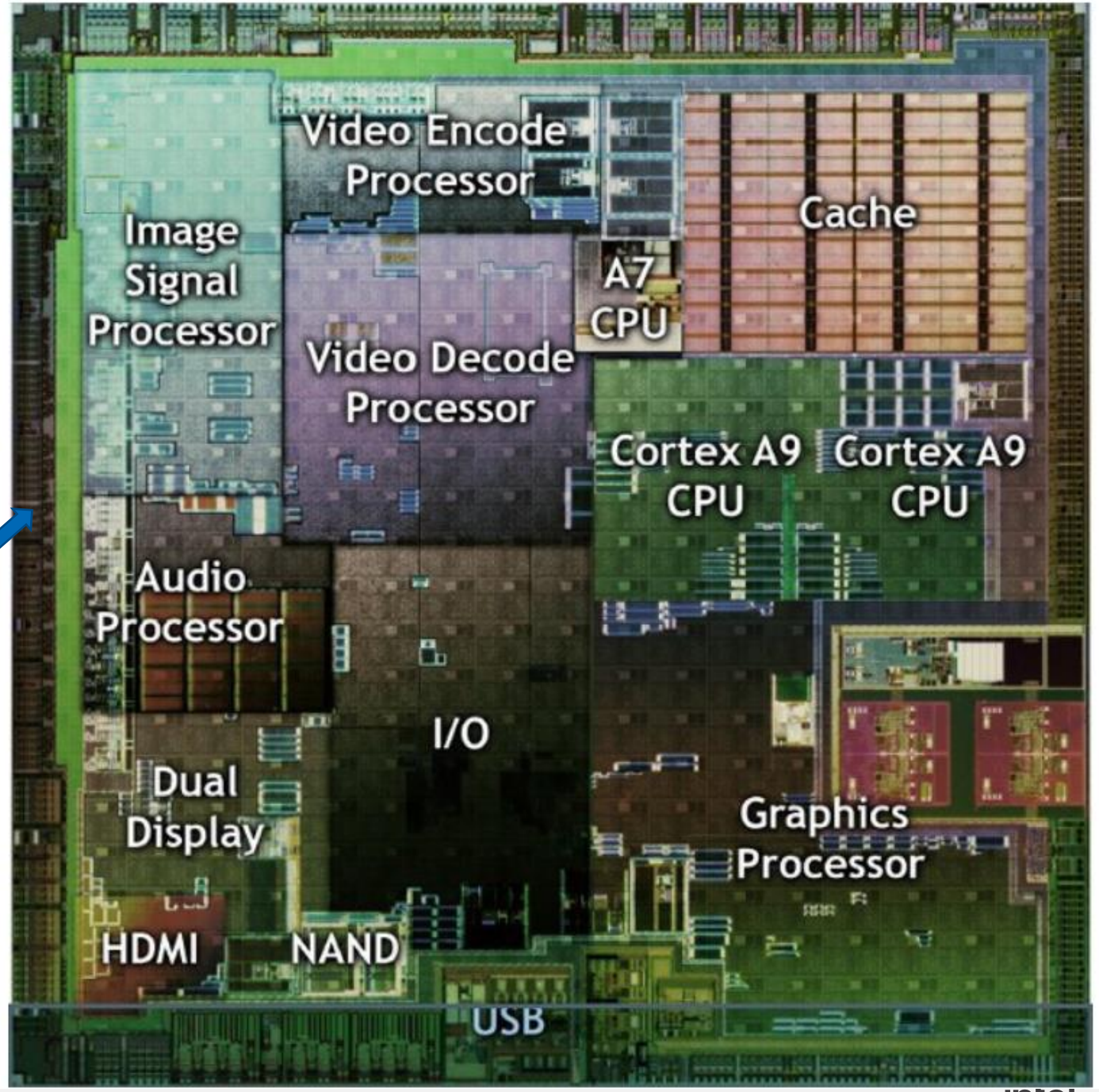
Smart Phone SoC

Different functional units integrated in an SoC

Low Power

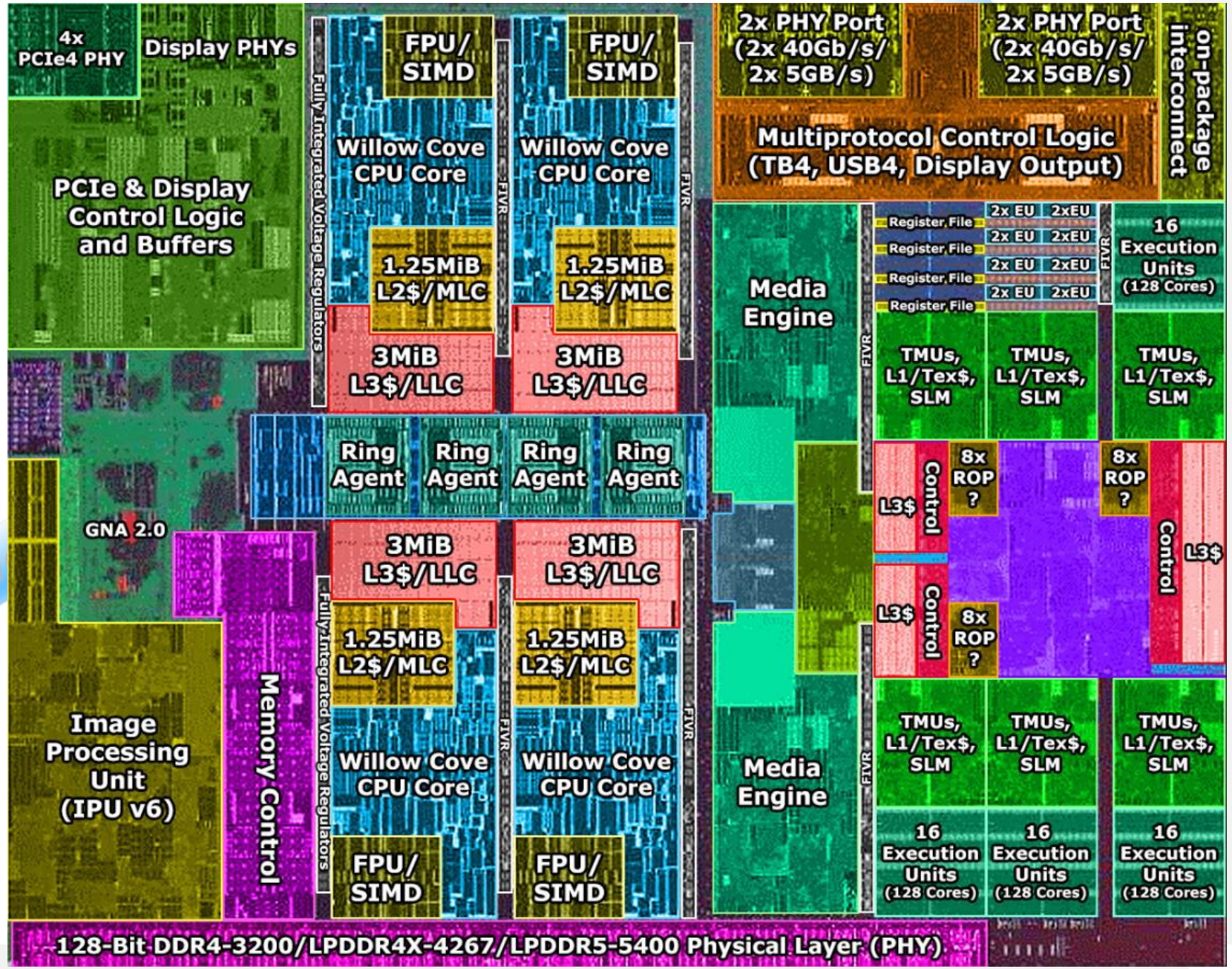


iphone 12 Motherboard (Source : ifixit)



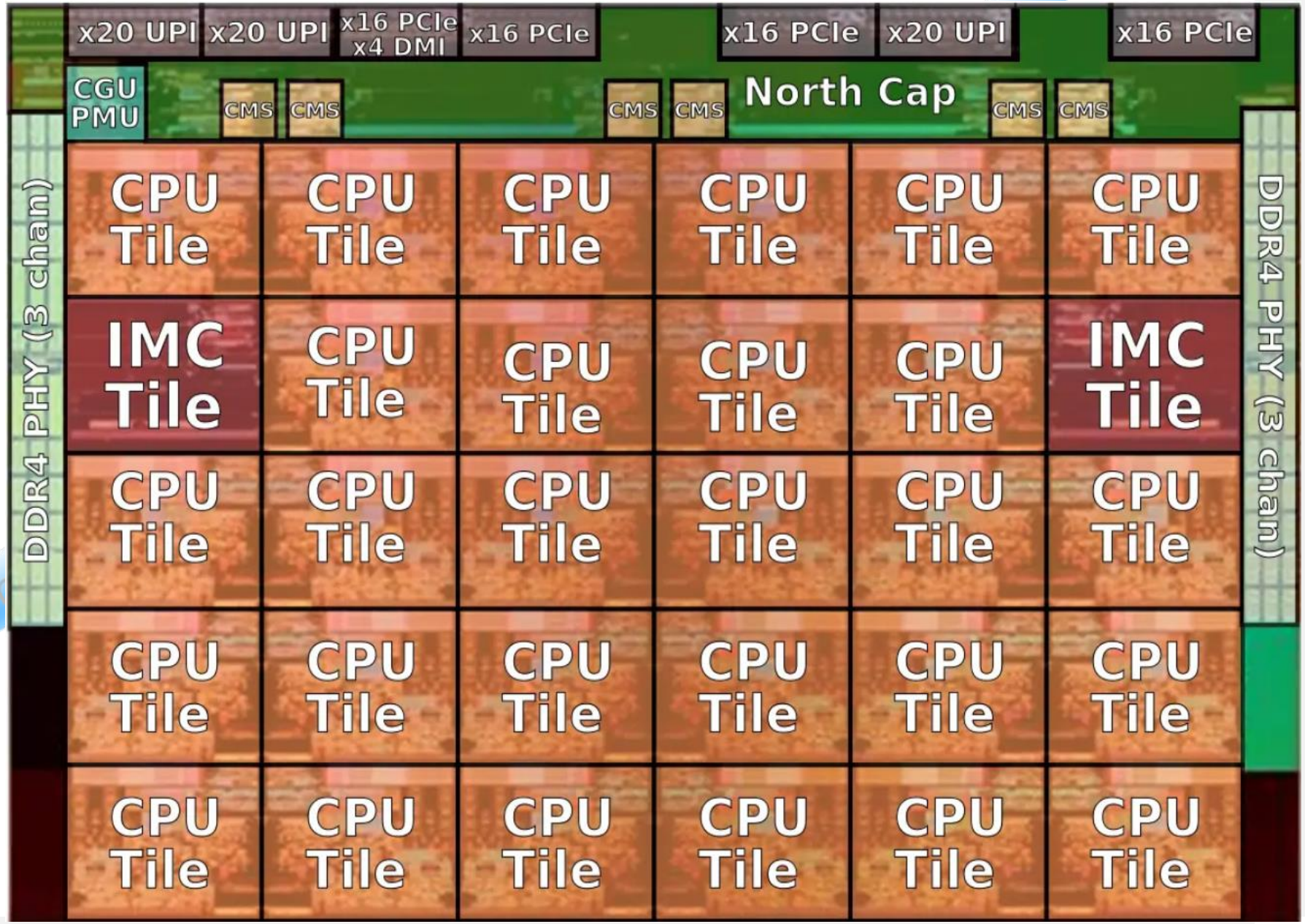
PC SoC

- General Purpose SoC
- Medium power



HPC SoC

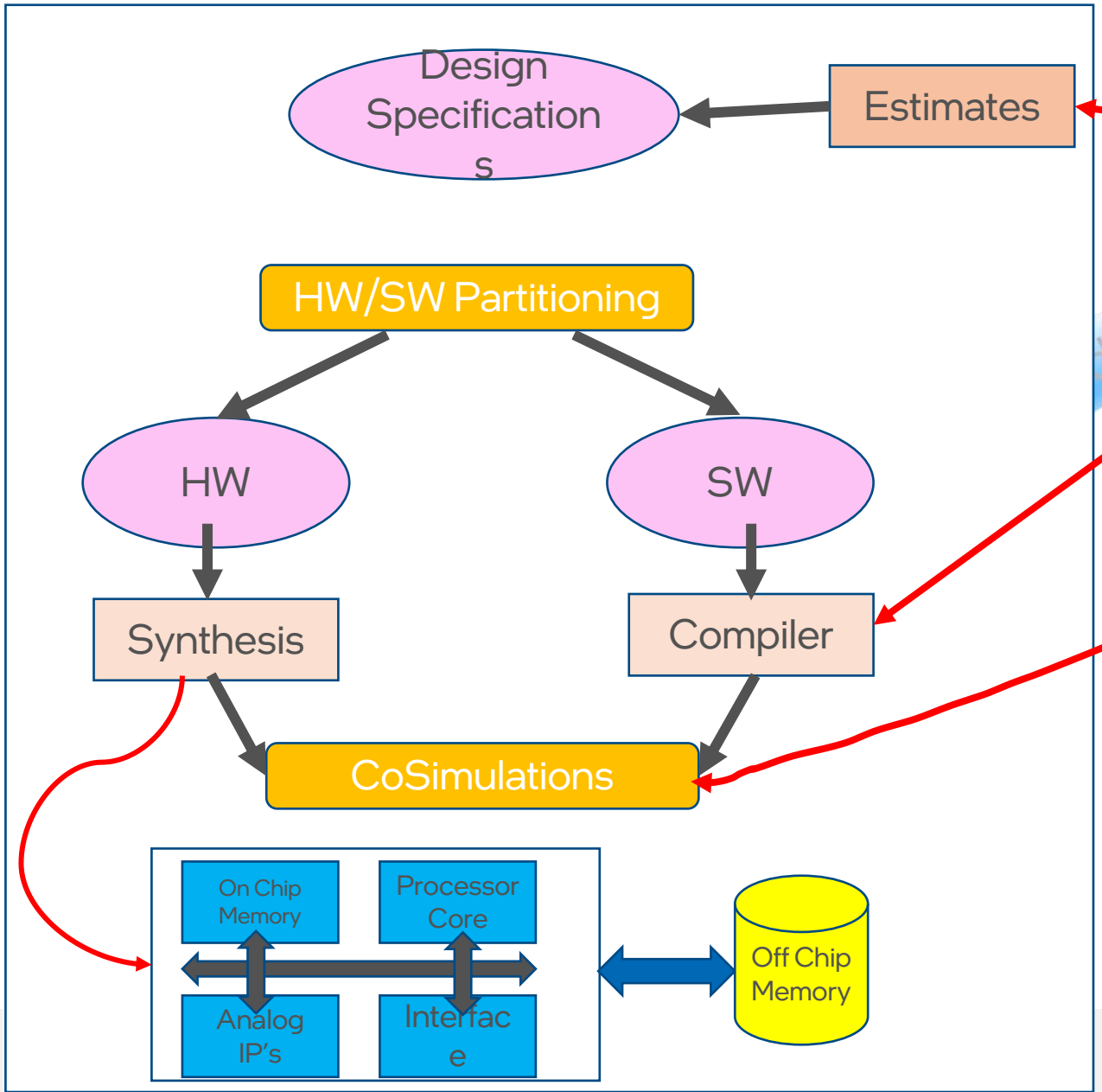
- Performance device
- Very High Power
- Big Die's

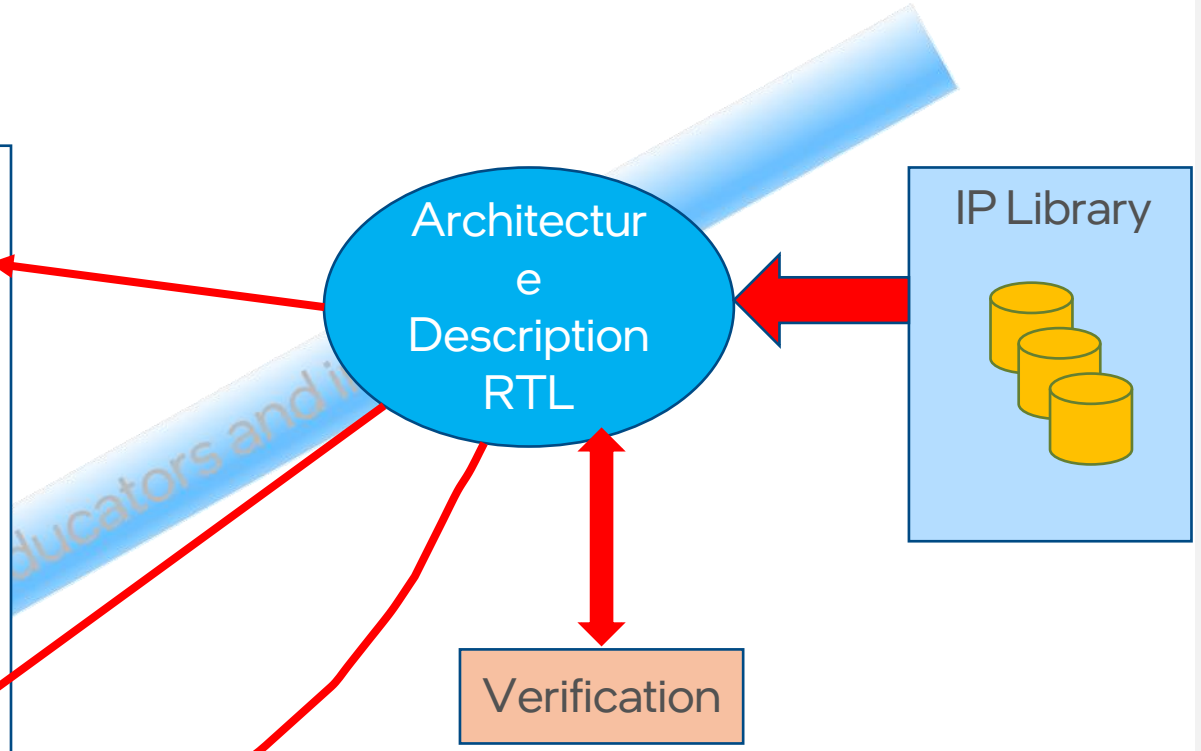


Benefits of SoC

- Overall reduced System Cost
- Increased Performance
- Low Power Consumption
- Reduce System Size

SoC Design Flow



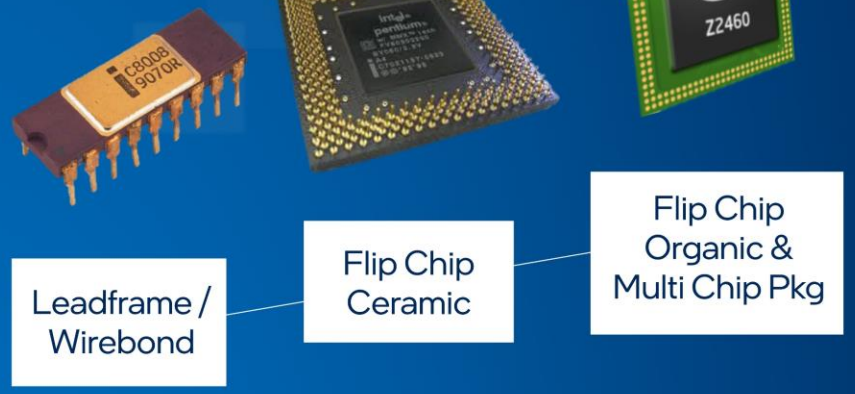


- Quick Design Exploration
- TFM re-use
- IP/Design re-use

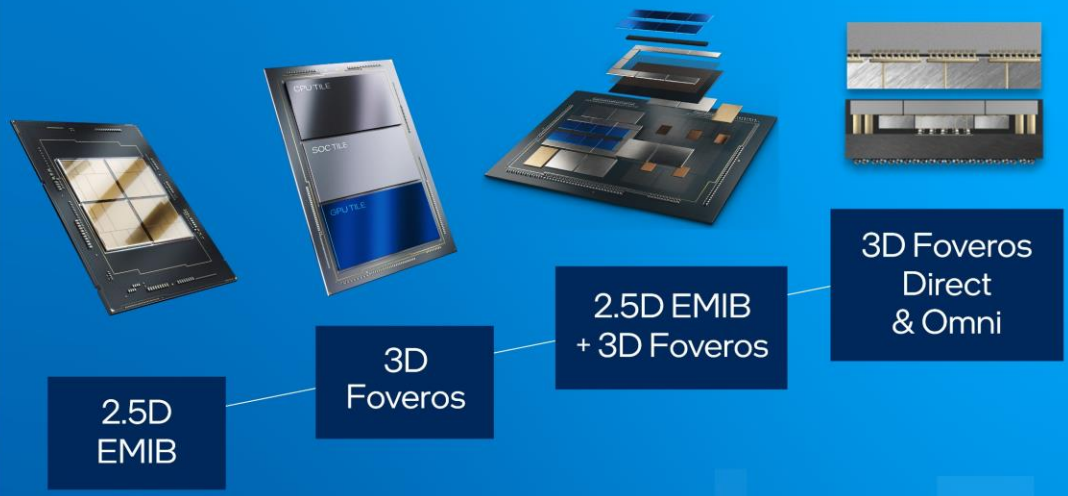
System In Package: SiP

Chip Dis-aggregation

Advance Packaging



Package main function:
provide power and signaling from motherboard to die



Added Package value:
high density interconnects that enable larger die complexes from multiple process nodes

PVC : Disaggregated SoP

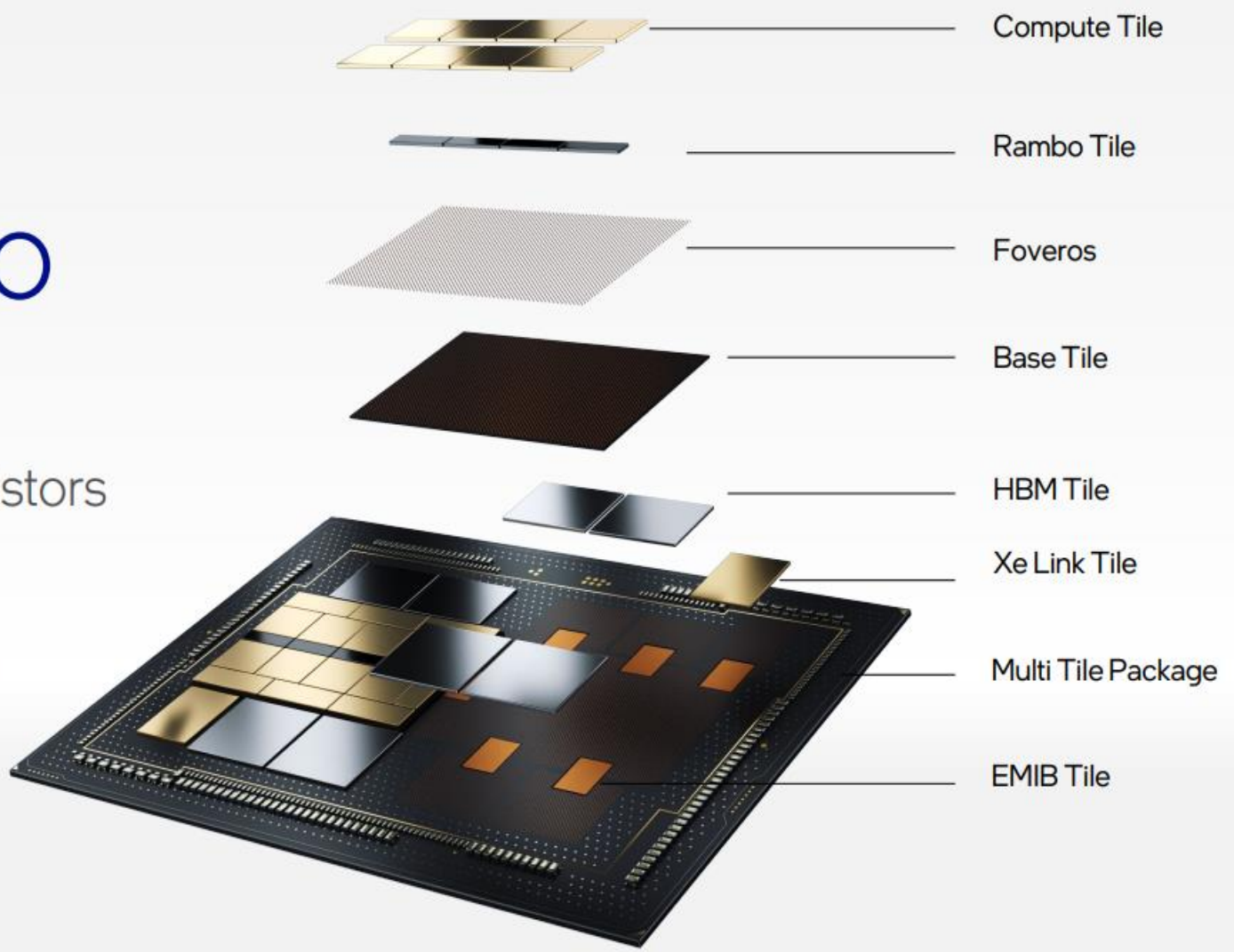
Ponte Vecchio

SOC

>100 Billion Transistors

47 Active Tiles

5 Process Nodes



Q&A

Thank You

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