AN 482: High Definition (HD) Video Monitoring Reference Design (M2)

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Introduction

The Altera® High Definition (HD) Video Monitoring Reference Designs demonstrate the application of Altera tools and devices to broadcast and video surveillance applications.

The reference designs provide a working template that can be used to rapidly build further broadcast applications using a flexible, re-usable and parameterizable video framework. All hardware functions in the reference designs use standard, open interfaces and protocols to facilitate function re-use and system design.

Specifically, the designs use the Altera Video and Image Processing Suite MegaCore® functions library, the SDI MegaCore® function, the DDR2 High Performance Memory Controller MegaCore® function, and supporting development tools.

For information about these MegaCore functions, refer to the *Video and Image Processing Suite User Guide*, *SDI MegaCore function User Guide*, and *DDR and DDR2 SDRAM High-Performance Controller User Guide*.

The Milestone 2 (M2) release of the reference design demonstrates how to deal with input resolution change of an interlaced high definition (HD) or standard definition (SD) video frame through a downscaling data path.

The downscaled video frame is mixed with the original unscaled video from a 1,920×1,080 HD source in interlaced format (1080i60), or a 720×480 SD source in interlaced format (NTSC) that is deinterlaced using the new motion adaptive deinterlacer.

You can switch between a multiple view, where both the downscaled frames and the original video, at its original size, are shown and a single view where just the original video is shown.

All user interaction is performed using button 0 of the push-buttons (S6) on the Stratix® II GX development board. The frames are input over a single triple-rate SDI interface and the output is via a 1080p60 DVI interface.

Video Design Flow

The M2 reference design provides a simple, yet highly parameterizable, design flow.

Each parameterizable IP block is implemented using standard interfaces:

- Avalon® Streaming (Avalon-ST) interfaces for point-to-point data connections using the Avalon-ST Video protocol
- Avalon® Memory-Mapped (Avalon-MM) for address based read and write transactions

For information about the Avalon-MM and Avalon-ST interfaces, refer to the *Avalon Interface Specifications*. For information about the Avalon-ST Video protocol, refer to the *Interfaces* chapter in the *Video and Image Processing Suite User Guide*.

These interfaces allow you to rapidly, and cleanly, develop and/or integrate:

a. video processing data paths

b. control logic

c. external memory controllers

The designs are implemented using the Quartus II software, SOPC Builder and the Nios Embedded Development Suite. The SOPC Builder system takes advantage of standard interfaces by presenting an abstracted view of the design, and generating an application specific switch fabric to construct the system. The control logic used is provided as a software project for the Nios II softcore processor.

For information on the Quartus II software and SOPC Builder, refer to the Quartus II online help.

Hardware Requirements

The video monitoring reference design requires the following hardware components:

- Audio Video Development Kit Stratix II GX Edition including:
  - Stratix II GX video development board
  - Digital video interface (DVI), serial digital interface (SDI), and asynchronous serial interface (ASI) inputs and outputs
  - DDR2 DIMM external memory
- A monitor or display with a DVI interface supporting 1,920×1,080 resolution
- One DVI cable to connect the `DVI_TX` output to the monitor
- A SDI source providing 1080i60or NTSC output connected to `SDI_IN0`

Software Requirements

The video monitoring reference design is supported on Windows XP only. You must have the following software installed on your PC:

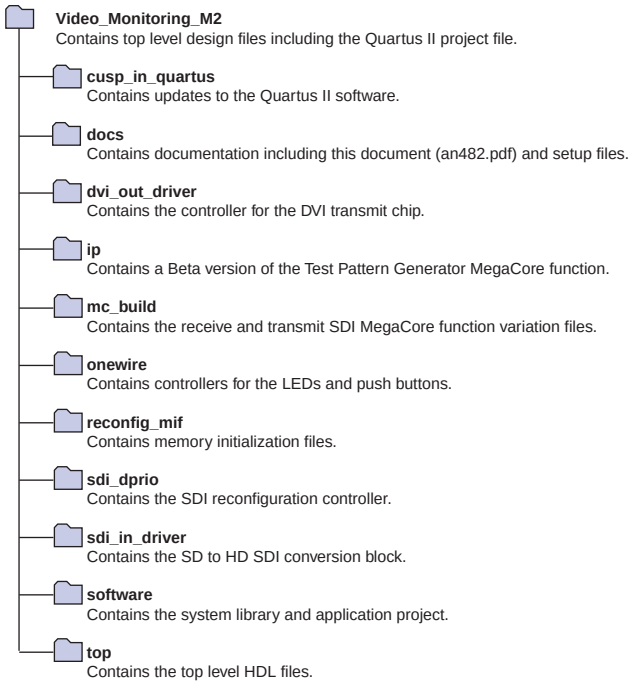
- Quartus II software, v8.0 SP1
- SOPC Builder, v8.0 SP1
- Nios II Embedded Development Suite, v8.0 SP1
- MegaCore IP Library, v8.0 SP1 (including the Video and Image Processing Suite, SDI and DDR2 MegaCore functions)
- Update to the IP and IP generation engine. See "Review the Example Design" on page 13 for instructions on updating the 8.0 SP1 installation.

Installing the Reference Design

The reference design is available as a zip file from the Altera Multimedia System Solutions Group.

Figure 1 shows the directory structure for the reference design files when they have been extracted from the zip file.

Figure 1. Reference Design Directory Structure



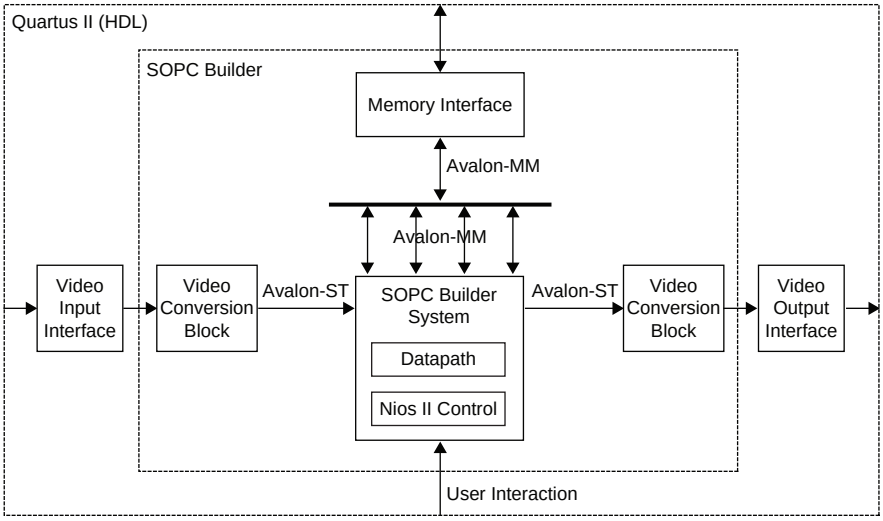
Tool Flow

The SOPC Builder system has four main external connections as shown in Figure 2 on page 4:

- Video input from an external video interface. The connection to the external video interface is made using a parameterizable video conversion IP function. The IP function provides a bridge between a clocked video interface (such as a SDI MegaCore function) and the Avalon-ST flow controlled domain.
- Video output to an external video interface. The connection to the external video interface is done using a parameterizable video conversion IP function. The IP function provides a bridge between the Avalon-ST flow controlled domain and a clocked video interface (such as DVI).
- Connection to an external memory interface. This connection uses a DDR2 SDRAM Controller MegaCore function. SOPC Builder generates the application specific switch fabric to arbitrate between multiple masters trying to access the controller.

- Connection to a control block. This block handles the run-time configuration of the Video and Image Processing MegaCore functions as a response to an input resolution or frame rate change, or user interaction via the push buttons on the development board. All of the control block functionality is implemented in software running on a Nios® II processor.

Figure 2. Tool Flow Block Diagram



SOPC Builder

SOPC Builder provides an abstracted design environment that simplifies the process of system design, including the datapath, control logic and external memory integration.

All the connections in the SOPC Builder system use Avalon-ST and Avalon-MM interfaces. SOPC Builder provides arbitration for multiple Avalon-MM masters accessing a single memory interface.

The parameterizable video conversion MegaCore functions interface to the `Datapath` block with the standard Avalon-ST interface, using the same video protocol used by the Video and Image Processing Suite MegaCore functions.

Refer to the *Interfaces* chapter in the Video and Image Processing Suite User Guide for a full description of this protocol.

The `Datapath` block in Figure 2 contains multiple Video and Image Processing Suite MegaCore functions that are used to perform common video processing functions, including scaling, mixing, deinterlacing, chroma resampling, and color space conversion. The `Datapath` block also contains a parameterizable Frame Buffer MegaCore function that provides a convenient function for double or triple buffering data in external memory and supporting system rate changes.The MegaCore function GUIs are used to configure these functions in SOPC Builder.

The `SOPC Builder System` includes a Nios II processor subsystem which includes standard peripherals such as timers, and I/O interfaces.

Quartus II

The SOPC Builder system is connected to the external video interfaces (implemented by a SDI MegaCore Function and DVI Controller) using HDL. Pin assignments and I/O constraints are set in the Quartus II software. The Quartus II project file is **test_system.qpf**.

Features

The Video Monitoring Reference Design is provided as a Quartus II project supporting:

- One background layer in format R'G'B, 4:4:4, consisting of a color bar.
- One HD 1080i60 (1,920×1,080, interlaced), or SD NTSC (720×480, interlaced) SDI input as source.
- Chroma upsampling from 4:2:2 to 4:4:4 for stream 1.
- Color Space conversion from Y'CbCr to R'G'B'.
- Deinterlacing of source stream using the motion adaptive deinterlacer.
- Downscaling of source stream (1,920×1,080 or 720×480) to 480×270 or 180×120 using frame buffers to support data throughput changes and synchronization.
- Reconfiguration of the source stream data processing path at run-time as a result of resolution or frame rate change at source.
- One 1080p60 (1,920×1,080) DVI output.

Design Description

Figure 3 on page 6 shows a block diagram of the Video Monitoring Reference Design system.

Block Descriptions

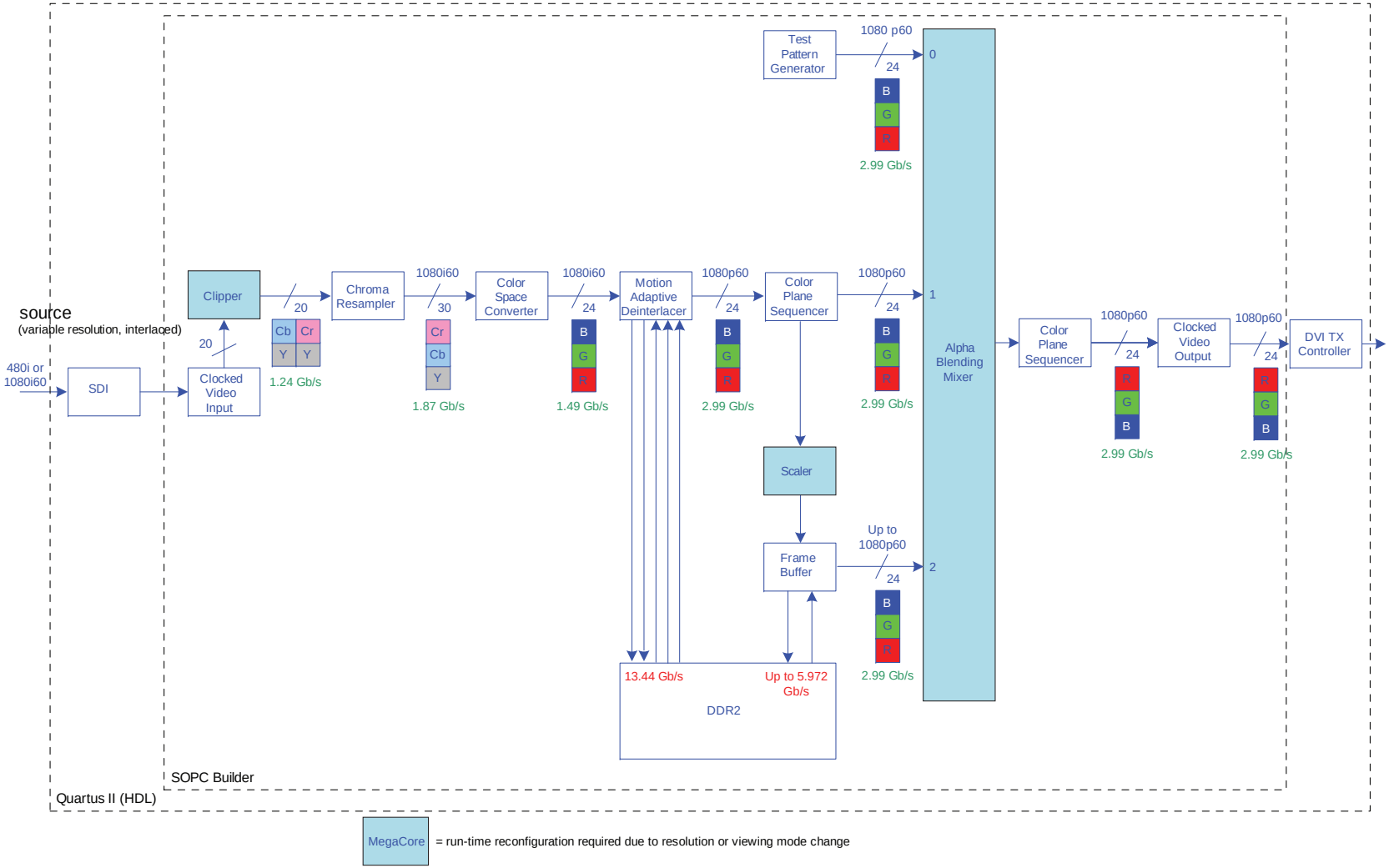
The following blocks are used in the Video Monitoring reference design:

SDI MegaCore Function

The SDI MegaCore function is configured as a triple -rate receiver serial digital interface. The SDI input clock frequency is 148.5 MHz for 3Gb/s HD or 74.25 MHz for 1.5Gb/s HD video inputs, and 27.0 MHz for SD video inputs. In this design, a clock frequency of 148.5 MHz is used.

☞ For more information about the SDI MegaCore function, refer to the *SDI MegaCore Function User Guide*.

Figure 3. System Block Diagram



Notes to Figure 3:

(1) 360p60 means 640×360 progressive @ 60 Hz.

(2) The shaded blocks in the data path from source 2 require run-time configuration due to possible resolution change at the input.

Clocked Video Input MegaCore Function

The Clocked Video Input MegaCore function converts a clocked video input to the Avalon-ST Video protocol used by the Video and Image Processing Suite MegaCore functions (removing blanking information). This block provides clock domain crossing that allows the image stream to run at a different frequency to the video input.

It has the following features:

- Support for sequential and parallel color planes (different data widths and formats)
- Support for different data streams:
  - BT656 (Composite or SD, HD & 3G SDI)
  - RGB (DVI)
- Configurable FIFO size
- Support for clock domain crossing
- Feedback about FIFO over/underflow

The Clocked Video Input block are is configured for:

- 20-bit HD SDI (BT656) input
- FIFO depth of two 1080p lines. Each line contains 1,920 samples giving a FIFO depth of one 1080p line and a width of 20 bits (9.4Kbit)
- Run-time control enabled

For more information about the Clocked Video Input MegaCore function, refer to the *Video and Image Processing Suite User Guide*.

Clipper MegaCore Function

The Clipper MegaCore function is used when the SDI input is in NTSC format. In this mode, it clips the top three lines of both fields and the bottom line of Field 0.

If the SDI input is any other format the clipper leaves it untouched.

For more information about the Clipper MegaCore function, refer to the *Video and Image Processing Suite User Guide*.

Color Plane Sequencer MegaCore Function

The Color Plane Sequencer MegaCore function in the output stream is configured to swap the red (R') and blue (B') components.

For more information about the Color Plane Sequencer MegaCore function, refer to the *Video and Image Processing Suite User Guide*.

Chroma Resampler MegaCore Function

The Chroma Resampler MegaCore Function is configured for:

- Input of two 10-bit color planes in parallel (Y' and alternating Cb or Cr), 4:2:2
- Output of three10-bit color planes in parallel, 4:4:4

- Luma adaptive algorithm for horizontal resampling

Resolution changes are handled by control packets in the Avalon-ST Video protocol.

For more information about the Chroma Resampler MegaCore function, refer to the *Video and Image Processing Suite User Guide*.

Color Space Converter MegaCore Function

The Color Space Converter MegaCore function is configured for:

- Input of three 10-bit color planes in parallel (Y'CbCr)
- Output of three 8-bit color planes in parallel (R'G'B')
- Y'CbCr: HDTV to Computer R'G'B' coefficients
- The maximum resolution is set to 1,920×1,080

For more information about the Color Space Converter MegaCore function, refer to the *Video and Image Processing Suite User Guide*.

Deinterlacer MegaCore Function

The Deinterlacer MegaCore function is configured for:

- Maximum resolution of 1,920×1,080
- Input of three 8-bit color planes in parallel (R'G'B') at 1080i60
- Output of three 8-bit color planes in parallel (R'G'B') at 1080p60
- Motion-adaptive deinterlacing method
- Double-buffering with Avalon-MM port width set to 256 bits
- Output frame rate set as input field rate

For more information about the Deinterlacer MegaCore function, refer to the *Video and Image Processing Suite User Guide*.

Scaler MegaCore Function

The Scaler MegaCore function is configured for:

- Input and output of three 8-bit color planes in parallel (R'G'B')
- Run-time control used to change output resolution depending on the viewing mode
- Polyphase mode with 16×16 taps and Lanczos-2 coefficients
- Run-time control turned on
- Maximum output resolution set to 1,920×1,080

For more information about the Scaler MegaCore function, refer to the *Video and Image Processing Suite User Guide*.

Frame Buffer MegaCore Function

The Frame Buffer MegaCore function takes image stream frames and buffers them into memory using an Avalon-MM connection (in this case DDR2 memory). The Frame Buffer can also drop or repeat frames where necessary to smooth out the data flow. This block has the following features:

- Parameterizable GUI
- Support for different frame width/heights
- Support for different sequential/parallel color planes and different data widths
- Support for different memory data widths
- Support for run-time control

The Frame Buffer MegaCore function is configured for:

- 24-bit wide Avalon-ST source and sink
- Three 8-bit color planes in parallel
- 256-bit wide Avalon-MM read and write masters (for 64-bit DDR2)
- Resolution set by control packets with maximum resolution of 1,920×1,080
- Both frame dropping and frame repeating allowed

For more information about the Frame Buffer MegaCore function, refer to the *Video and Image Processing Suite User Guide*.

DDR2 SDRAM High Performance Controller MegaCore Function

This is the controller block for the external DDR2 SDRAM required as buffer for the Deinterlacer and the three Frame Buffers described above. It is configured for:

- Micron MT9HF6472AY-5EB38 (72-bit, 512MByte, 533MT/s, CL4, 266.7MHz)
- Data width set to use 64 bits (SOPC Builder cannot handle non power of 2 data widths)
- Memory set up in Half-Rate mode (266.7MHz internally, 133.35MHz externally)

For more information about the DDR2 SDRAM High Performance Controller MegaCore Function, refer to the *DDR and DDR2 SDRAM High Performance Controller User Guide*.

Test Pattern Generator (Beta) MegaCore Function

This block generates a color bar which is used as the background layer for the Alpha Blending Mixer. It is configured for:

- Resolution 1,920×1,080
- 8 bits per color plane in parallel
- R'G'B
- 4:4:4
- Progressive output

Alpha Blending Mixer MegaCore Function

This block mixes three input layers under software control at run-time. It is configured for:

- Three input layers:
  - Layer 0 (background) - 1,920×1,080 color bar
  - Layer 1 - 1,920×1,080 or 720×480 output from the Deinterlacer
  - Layer 2 - 480×270 or 180×120 output from run-time configurable Scaler

For more information about the Alpha Blending Mixer MegaCore function, refer to the *Video and Image Processing Suite User Guide*.

Control Block (Nios II Processor)

This block is based on a Nios II embedded processor connected to DDR2-SDRAM, together with the Video and Image Processing Suite MegaCore functions, through an Avalon-MM master. The Control block initializes the run-time reconfigurable blocks at startup, after mode change as caused by user interface interaction, or when a resolution change is detected.

Clocked Video Output MegaCore Function

The Clocked Video Output MegaCore function takes an Avalon-ST video stream and converts it to a clocked video stream (reconstructing blanking information). This block provides clock domain crossing that allows the Avalon-ST image stream to run at a different frequency to the clocked video output. It has the following features:

- Compile time parameterizable GUI
- Support for sequential and parallel color planes (different data widths and formats)
- Support for different data streams:
  - BT656 (Composite or SD, HD & 3G SDI)
  - RGB (DVI)
- Configurable FIFO size
- Supports clock domain crossing
- Feedback about FIFO over/underflow

The Clocked Video Output block is configured for:

- 24-bit DVI (RGB) output
- Video input and output use the same clock
- Run-time control enabled
- FIFO depth of 1 1080p line. This gives a FIFO depth of 1,920 and a width of 20 bits (9.4Kbit)

For more information about the Clocked Video Output MegaCore function, refer to the *Video and Image Processing Suite User Guide*.

DVI TX Controller

The DVI TX Controller controls the DVI transmitter block on the Stratix II GX Audio Video development board to output the video stream. This block provides:

- Compile time parameterizable HDL
- Support for different resolutions (720p30/60 and 1080p30/60)

The DVI TX Controller block is configured for:

- 24-bit (RGB), 1080p60 (1,920×1,080) output
- 148.5MHz output frequency

Clock Domains

The Nios II processor runs at 100MHz while the memory controller subsystem runs at 133.35MHz. The remainder of the SOPC Builder system, including the video datapath, run at 148.5MHz.

The DDR2 memory runs at its maximum rate of 266MHz. This requires the memory controller to run in half-rate mode.

The Clocked Video Input and Clocked Video Output blocks provide clock domain crossing which allows the DVI output and SDI input to run at the speed of the relevant standard being used.

Clock domain crossing is also used in the Deinterlacer and the Frame Buffers, as the Avalon-ST based data path runs at 148.5MHz, while the Avalon-MM based memory connections run at 133.35 MHz.

Reconfiguration Sequence

When the resolution changes at the input of the video source stream, the Nios II processor updates the scaler output resolution based on the new resolution that is read from the Clocked Video Input block.

All other resolution updates are handled by Avalon-ST Video control packets that are transmitted from block to block in addition to the video data.

Memory Bandwidth Calculations

Access to external memory is required (through the DDR2 SDRAM High Performance Memory Controller) for the Motion Adaptive Deinterlacer (five masters) and the Frame Buffer (two masters).

Motion Adaptive Deinterlacer

- Input format: 1080i60
  1,920 × 1,080 × 24bits × 60/2s = 1.493Gbit/s
- Output format: 1080p60
  1,920 × 1,080 × 24bits × 60 = 2.986Gbit/s

- Memory access:
  1 × write at input rate: 1.493Gbit/s
  1 × write at output rate: 2.986Gbit/s
  3 × read at output rate: 8.958Gbit/s
- Total: 13.437Gbit/s

Frame Buffer (After Scaling)

- Input format: 480×270 progressive at 60Hz
  480 × 270 × 24 bits × 60/s = 0.187Gbit/s
- Output format: 480×270 progressive at 60Hz
  480 × 270 × 24bits × 60/s = 0.187Gbit/s
- Memory access:
  1 × write at input rate: 0.187Gbit/s
  1 × write at output rate: 0.187Gbit/s
- Total (per frame buffer): 0.374Gbit/s

Total Bandwidth

- Deinterlacer: 14.437Gbit/s
- Frame Buffer 0.374Gbit/s
- Total: 14.811Gbit/s

The Stratix II GX development board when used with the Micron MT9HTF6472AY-53EB3 high-performance DDR2 SDRAM provides a maximum theoretical bandwidth of:

266.7 MHz × 64 bits × 2 (both clock edges used) = 34.133 Gbit/s

This results in a memory access efficiency requirement of up to 43%.

Memory bandwidth efficiency is determined by a number of factors, such as randomness of addresses, refresh rate, turnaround times between reads and writes, and burst lengths.

Altera's memory controllers can reach an efficiency of up to about 90% if the access conditions are right (long bursts of writes to the same column followed by long bursts of reads).

The use of a half-rate memory controller in order to satisfy the memory bandwidth requirements means that the local interface width between memory controller and internal FPGA logic is 256 bits (= 4 × 64 bits).

Both DDR2 memory and memory controller will run at 266MHz, while the internal FPGA blocks will run at half this rate, that is, 133MHz.

Replacing the SDI Input with DVI

An all DVI system is much simpler and can be produced by the following steps:

1. Replace the SDI MegaCore function with a DVI RX Controller.
2. Configure the Clocked Video Input MegaCore function for the DVI input.
3. Remove the Chroma Resampler and Color Space Converter MegaCore functions.
4. Regenerate the SOPC Builder system and recompile the Quartus II project.

Review the Example Design

This section describes how you can open the High Definition (HD) Video Monitoring Reference Design components in SOPC Builder.

To review the complete High Definition (HD) Video Monitoring Reference Design in SOPC Builder perform the following steps:

1. Run the Quartus II software to ensure the *QUARTUS_ROOTDIR* environment variable is correctly set.
2. Close the Quartus II software.
3. In Windows Explorer, browse to the install directory.
4. Double-click on **update_quartus.bat** to install updates to the Video and Image Processing toolkit blocks.
5. Double-click on **make_project.bat** to create the quartus project.
6. Re-open the Quartus II software.
7. Choose Open Project (File menu), browse to the <*install directory*> and select the Quartus II project file: **test_system.qpf**.
8. Choose **SOPC Builder** from the Tools menu in the Quartus II software.
9. Generate the SOPC Builder system by clicking on **Generate**. Progress messages are issued in the SOPC Builder **System Generation** window and should complete with a message:

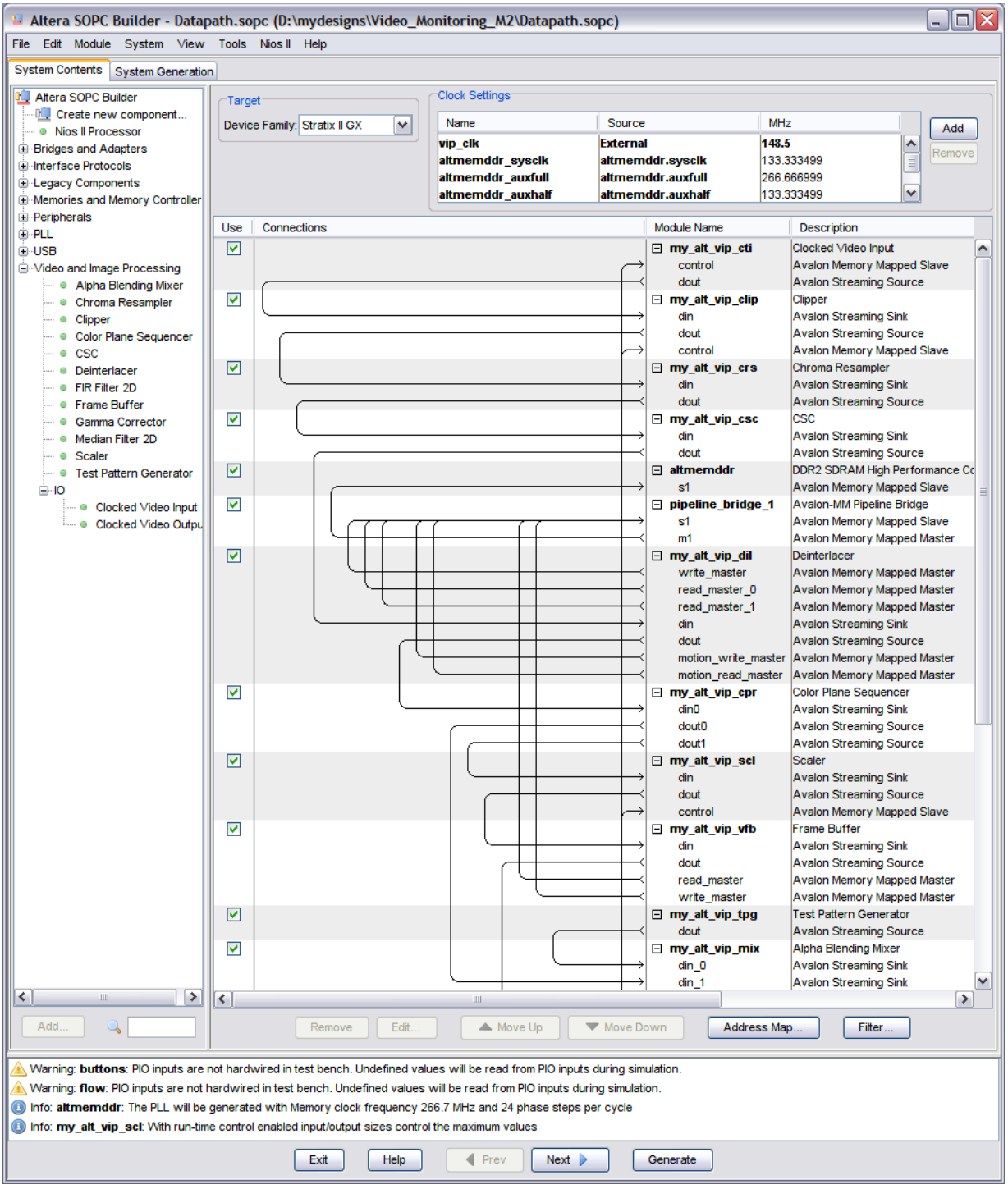
   ```
   Info: System generation was successful.
   ```

10. Close SOPC Builder and choose **Start Compilation** from the Processing menu to compile the Quartus II project.

☞ If any there are any blocks are missing from your SOPC Builder project, check that step 4 completed without errors. If necessary, you can add any missing directories to your IP Search Path by choosing **Options** from the Tools menu in SOPC Builder.

The complete SOPC Builder design is shown in Figure 4 on page 14.

Figure 4. Video Monitoring Reference Design in SOPC Builder (Part 1 of 3)

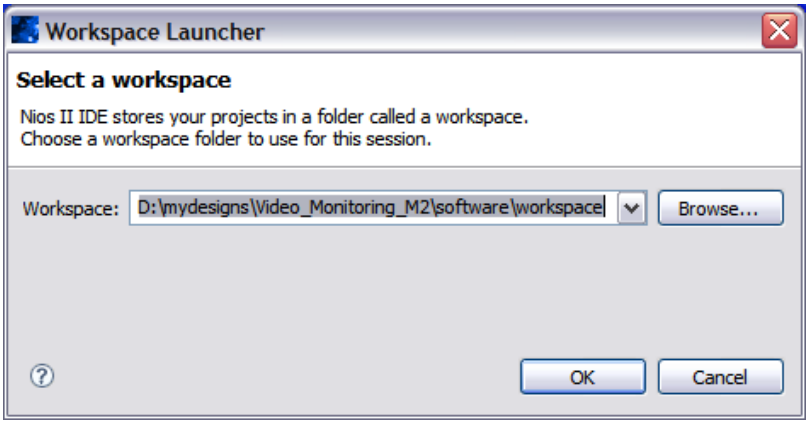


Building the Software in the Nios II IDE

Perform the following steps to build the software in the Nios II Integrated Development Environment (IDE):

1. Start the Nios II IDE, v8.0 SP1 software.
2. Choose **Switch Workspac**e from the File menu and browse to the **software** subdirectory of the M2 design install directory.

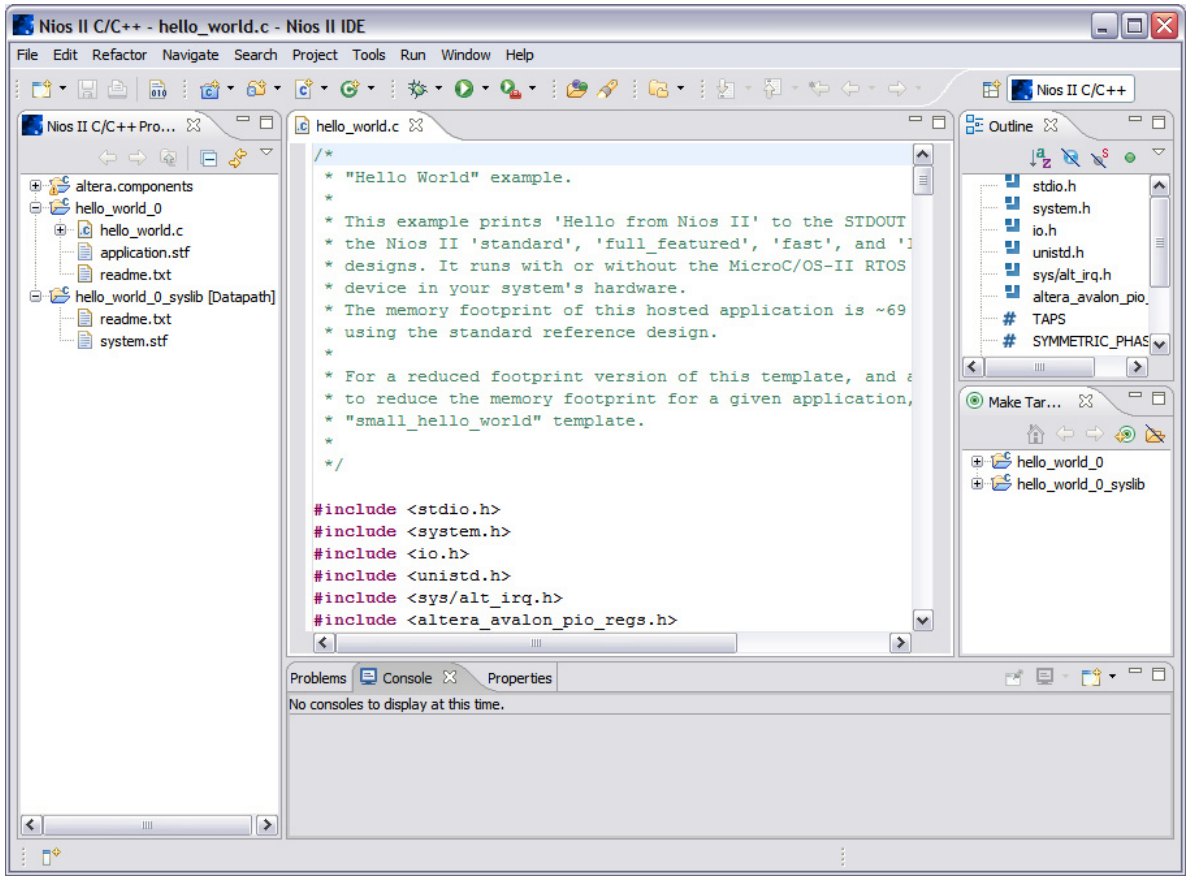
Figure 5. Nios II IDE Workspace Launcher



3. Add `workspace` to the end of the path name and click **OK** to create a new workspace.
4. Choose **Import** from the File menu and double- click on **Altera Nios II** in the Import dialog box. Choose **Existing Nios II IDE project into workspace** and click **Next**.
5. Browse to the application project (**hello_world_0**) and click **Finish**.
6. Repeat step 4 for the library project (**hello_world_0_syslib**).
7. Browse to the PTF file (**Datapath.ptf**) in the Quartus II project directory and confirm that `cpu` appears in the **CPU** field. Click **Finish** to import the project from the file system.
8. Check that the application project (**hello_world_0**) and system library project (**hello_world_0_syslib**) are shown in the workspace (Figure 6 on page 16).
9. Browse the application source code listed below **hello_world_0**.
10. Right click on **hello_world_0** and choose **System Library Properties** to browse the library properties.
11. Right click on **hello_world_0** and select **Build Project**. Confirm that the **debug** directory (containing the **hello_world_0.elf** file) appears after a few minutes.
12. After programming the development board with hardware, right click on **hello_world_0** and select **Run As->Nios II Hardware** to download the control software.

☞ The default software is already included in the .**sof** and .**pof** files.

Figure 6. Nios II Integrated Development Environment (IDE) Workspace



Conclusion

The High Definition (HD) Video Monitoring Reference Design demonstrate a re-usable and flexible video framework for rapid development of video and image processing designs.

The use of standard open interfaces and protocols throughout the system allows you to build further applications, by re-using parameterizable IP from the Altera IP library or by adding your own IP to the framework.

The video framework does not preclude use of HDL to connect the IP components. However, the HD Video Monitoring Reference Designs demonstrate that the SOPC Builder environment significantly accelerates system design by:

- Automatic generation of an application specific switch fabric and ability to insert a custom priority arbitration scheme.
- Providing an abstracted view of the video system.
- Detecting and displaying Altera and user IP in an immediately accessible form.

Revision History

Table 1 shows the revision history for the *AN-482: High Definition (HD) Video Monitoring Reference Design M2* application note.

Table 1. AN-482 Revision History

Version	Date	Summary
4.0	August 2008	Updated to use Nios II processor, added support for SD video input and video frame locking.
3.0	February 2008	Added design variants for 1080i60 and 1080p60.
2.0	December 2007	Added support for interlaced video, All blocks are now integrated directly within SOPC Builder.
1.0	September 2007	First release of this application note.

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