High Definition (HD) Video Monitoring Reference Design (Milestone 4)

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Introduction

The Altera® High Definition (HD) Video Monitoring Reference Designs demonstrate the application of Altera tools and devices to broadcast and video surveillance applications.

The reference designs provide a working template that can be used to rapidly build further broadcast applications using a flexible, re-usable and parameterizable video framework. All hardware functions in the reference designs use standard, open interfaces and protocols to facilitate function re-use and system design.

Specifically, the designs use the Altera Video and Image Processing Suite MegaCore® functions library, the SDI MegaCore® function, the DDR2 High Performance Memory Controller MegaCore® function, and supporting development tools.

For information about these MegaCore functions, refer to the *Video and Image Processing Suite User Guide*, *SDI MegaCore function User Guide*, and *DDR and DDR2 SDRAM High-Performance Controller User Guide*.

The Milestone 4 (M4) release of the reference design demonstrates how to deal with input resolution change of a progressive high-definition (HD) video frame through a downscaling data path.

The downscaled video frame is mixed with a second frame coming from a 1920×1080 HD source in interlaced format (1080i60) that is deinterlaced using the new motion adaptive deinterlacer and downscaled to the same resolution.

You can switch between a multiple view, where both downscaled frames are shown as thumbnails side-by-side on the graphical layer, an overlay view where either of the two frames is shown in its original size with a graphical overlay, and a single view where either of the two frames is shown in its original size without an overlay.

The switching between the modes is controlled using a graphical user interface implemented on the Nios® II softcore processor. All the user interaction is performed using the rotary encoder and push button (PB2) on the Stratix® II GX development board. Both frames are input over a 3G SDI interface and the mixed result is output via a 1080p60 DVI interface.

Video Design Flow

The M4 reference design provides a simple, yet highly parameterizable, design flow.

Each parameterizable IP block is implemented using standard interfaces:

- Avalon® Streaming (Avalon-ST) interfaces for point-to-point data connections
- Avalon® Memory-Mapped (Avalon-MM) for address based read and write transactions

For information about the Avalon-MM and Avalon-ST interfaces, refer to the *Avalon Memory-Mapped Interface Specification* and the *Avalon Streaming Interface Specification*.

These interfaces allow you to rapidly, and cleanly, develop and/or integrate:

a. video processing data paths
b. control logic
c. external memory controllers

The designs are implemented using the Quartus II software, SOPC Builder and the Nios Embedded Development Suite. The SOPC Builder system takes advantage of standard interfaces by presenting an abstracted view of the design, and generating an application specific switch fabric to construct the system. The control logic used is provided as a software project for the Nios II softcore processor.

For information on the Quartus II software and SOPC Builder, refer to the Quartus II online help.

System Requirements

The High Definition (HD) Video Monitoring Reference Design are supported on Windows XP only. You must have the following software installed on your PC:

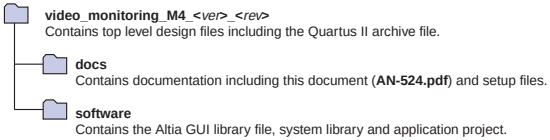
- Quartus II software, v7.2
- SOPC Builder, v7.2
- Nios II Embedded Development Suite, v7.2
- MegaCore IP Library, v7.2 (including the Video and Image Processing Suite, SDI and DDR2 MegaCore functions)
- Video and Image Processing Beta MegaCore functions and update to the IP generation engine. See "Review the Example Design" on page 20 for instructions on updating the 7.2 installation.

Installing the Reference Design

The reference design is available as a zip file from the Altera Multimedia System Solutions Group.

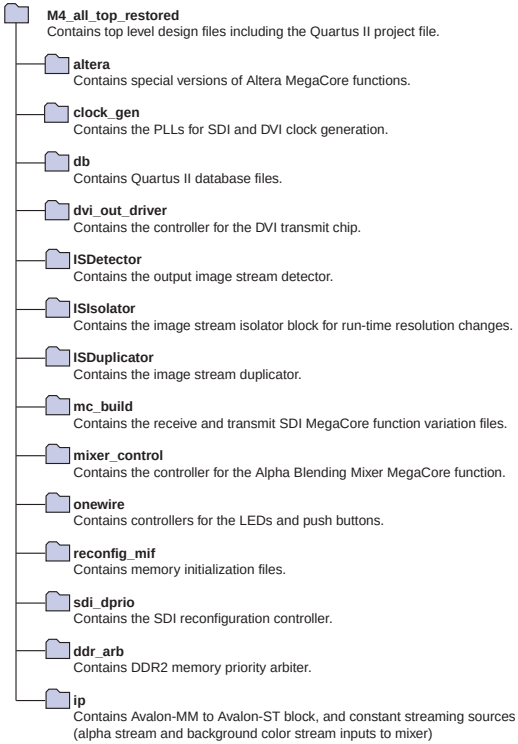
Figure 1 shows the directory structure for the reference design files when they have been extracted from the zip file.

Figure 1. Unzipped Reference Design



The top level directory contains a Quartus II archive file which can be opened in the Quartus II software. The structure shown in Figure 2 is created when you restore the Quartus II project.

Figure 2. Reference Design Directory Structure

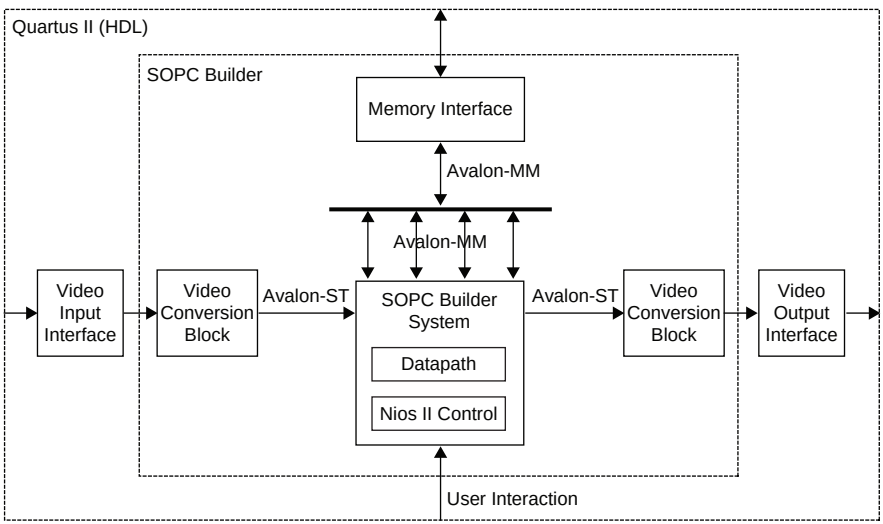


Tool Flow

The SOPC Builder system has four main external connections as shown in Figure 3:

- Video input from an external video interface. The connection to the external video interface is made using a parameterizable video conversion IP function. The IP function provides a bridge between a clocked video interface (such as a SDI MegaCore function) and the Avalon-ST flow controlled domain.
- Video output to an external video interface. The connection to the external video interface is done using a parameterizable video conversion IP function. The IP function provides a bridge between the Avalon-ST flow controlled domain and a clocked video interface (such as DVI).
- Connection to an external memory interface. This connection uses a DDR2 SDRAM Controller MegaCore function. SOPC Builder generates the application specific switch fabric to arbitrate between multiple masters trying to access the controller.
- Connection to a control block. This block handles the run-time configuration of the Video and Image Processing MegaCore functions as a response to an input resolution or frame rate change, or user interaction via the DIP switches or push buttons on the development board. Most of the control block functionality is implemented in software running on a Nios® II processor.

Figure 3. Tool Flow Block Diagram



SOPC Builder

SOPC Builder provides an abstracted design environment that simplifies the process of system design, including the datapath, control logic and external memory integration.

All the connections in the SOPC Builder system use Avalon-ST and Avalon-MM interfaces. SOPC Builder provides arbitration for multiple Avalon-MM masters accessing a single memory interface.

The parameterizable video conversion MegaCore functions (Beta release) interface to the `Datapath` block with the standard Avalon-ST interface, using the same video protocol used by the Video and Image Processing Suite MegaCore functions.

Refer to the *Interfaces* chapter in the *Video and Image Processing Suite User Guide* for a full description of this protocol.

The `Datapath` block in Figure 3 contains multiple Video and Image Processing Suite MegaCore functions that are used to perform common video processing functions, including scaling, mixing, deinterlacing, chroma resampling, and color space conversion. The `Datapath` block also contains a parameterizable Frame Buffer (Beta) MegaCore function that provides a convenient function for double or triple buffering data in external memory and supporting system rate changes.The MegaCore function GUIs are used to configure these functions in SOPC Builder.

The `SOPC Builder System` includes a Nios II processor subsystem which includes standard peripherals such as timers, and I/O interfaces. This Nios II processor is capable of rendering graphical overlays on top of the video streams. The SOPC Builder system includes an Avalon-MM to Avalon-ST block for streaming the graphical overlay out of memory. It includes a scaler to upscale the graphical overlay to the output resolution, and an alpha generator for creating transparent and semi-transparent regions in the graphics by replacing designated color patterns.

Quartus II

The SOPC Builder system is connected to the external video interfaces (implemented by a SDI MegaCore Function and DVI Controller) using HDL. Pin assignments and I/O constraints are set in the Quartus II software. The Quartus II project file is **M4_all_top.qpf**.

Features

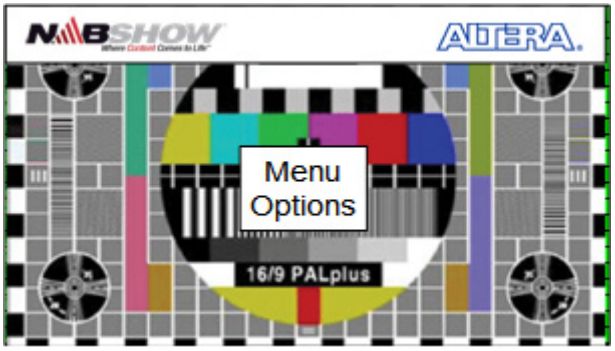
The Video Monitoring Reference Design is provided as a Quartus II project supporting:

- One background layer in format Y'CbCr, 4:4:4, consisting of a blue screen.
- One 3G 1080i60 (1920×1080, interlaced) SDI input as source 1 (stream 1).
- One 3G SDI input (progressive and variable resolution between 640×360 and 1920×1080) as source 2 (stream 2).
- A graphical overlay layer, rendered by the Nios II processor, drawn at 960×540 resolution with 16-bit color, and upscaled to 1920×1080 with 24 bit color.
- Chroma upsampling from 4:2:2 to 4:4:4 for both stream 1 and stream 2.
- Color Space conversion of both streams from Y'CbCr to R'G'B'.
- Deinterlacing of stream 1 using the motion adaptive deinterlacer.
- Downscaling of both stream 1 (1920×1080) and stream 2 (variable) to 640×360 using triple buffers to support data throughput changes and synchronization.
- Reconfiguration of the stream 2 data processing path at run-time as a result of resolution or frame rate change at source 2.
- Five mixing modes using the Alpha Blending Mixer:
  - Thumbnail view: Downscaled streams 1 and 2 side-by-side on the graphical layer (see Figure 4).

Figure 4. Alpha Blending Mixer Thumbnail View

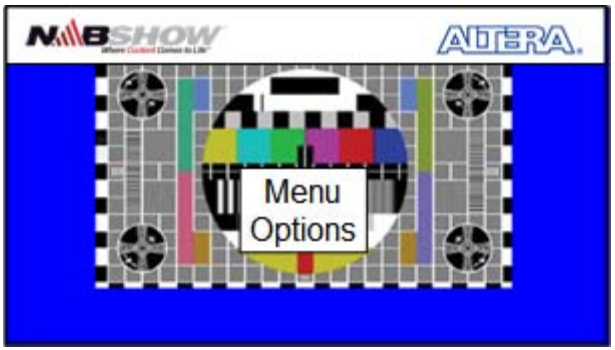
  - Overlay view (stream 1): Stream 1 in original size with a graphical overlay (see Figure 5 on page 7).

Figure 5. Alpha Blending Mixer Overlay View (Stream 1)



- Video view (stream 1): Stream 1 in original size without a graphical overlay (same as Figure 5 but without the graphical overlay).
- Overlay view (stream 2): Stream 2 in original size with a graphical overlay (see Figure 6).

Figure 6. Alpha Blending Mixer Overlay View (Stream 2)



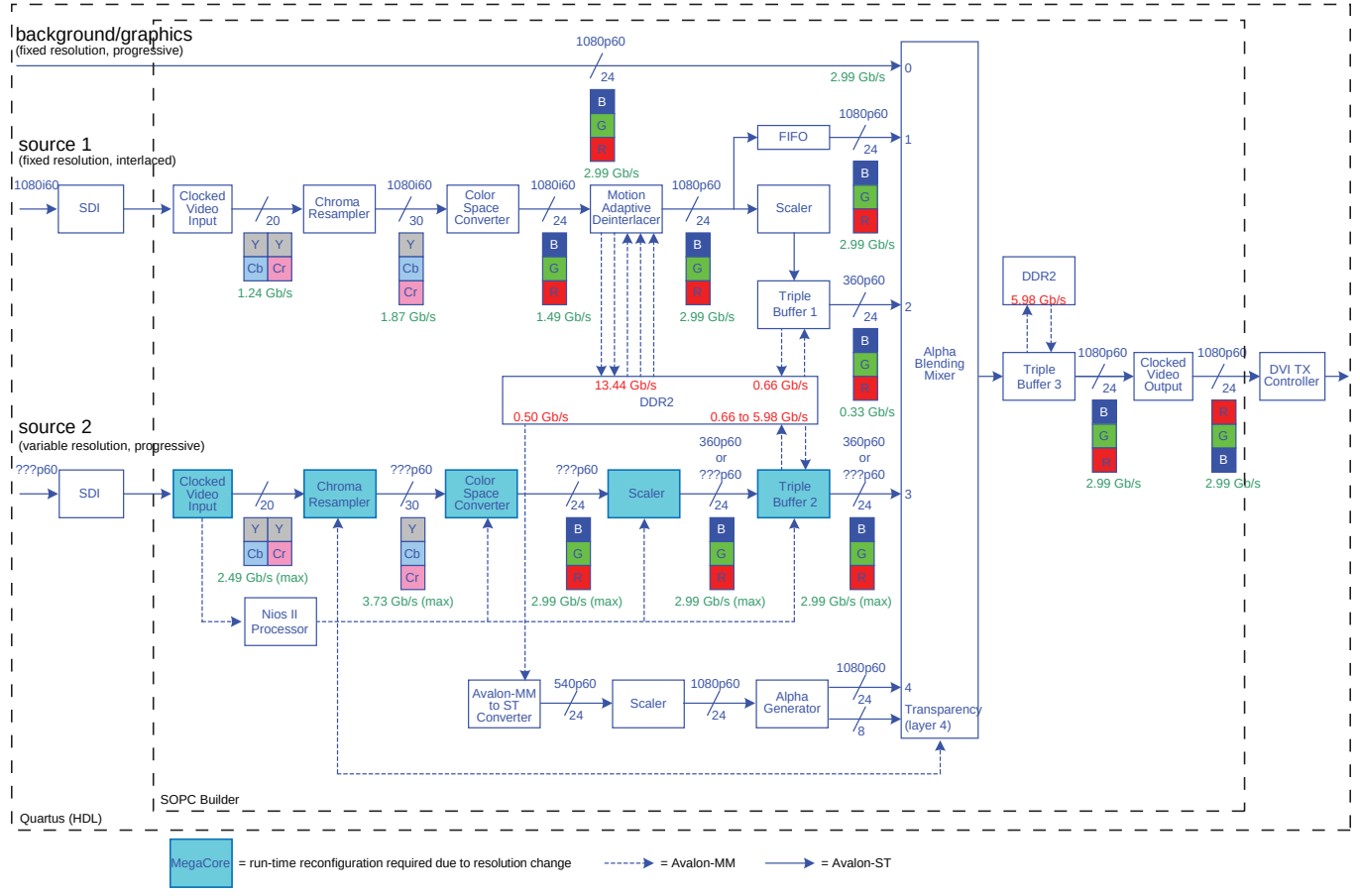
- Video view (stream 2): Stream 2 in original size without a graphical overlay (same as Figure 6 but without the graphical overlay).

- One 1080p60 (1920×1080) DVI output.

Design Description

Figure 7 on page 8 shows a block diagram of the Video Monitoring Reference Design system.

Figure 7. System Block Diagram



Notes to Figure 7:

(1) 360p60 means 640×360 progressive @ 60 Hz.

(2) The shaded blocks in the data path from source 2 require run-time configuration due to possible resolution change at the input.

Block Descriptions

The following blocks are used in the Video Monitoring reference design:

SDI MegaCore Function

The SDI MegaCore function is configured as a triple rate receiver serial digital interface. Two instances are required, one for each source. The SDI input clock frequency is 148.5 MHz or 74.25 MHz for HD video inputs and 27.0 MHz for SD video inputs. In this design, a clock frequency of 148.5 MHz is used.

For more information about the SDI MegaCore function, refer to the *SDI MegaCore Function User Guide*.

Clocked Video Input (Beta) MegaCore Function

The Clocked Video Input (Beta) MegaCore function converts a clocked video input to the image streaming protocol used by the Video and Image Processing Suite MegaCore functions (removing blanking information). This block, which will be part of the Video and Image Processing Suite in a future release, provides clock domain crossing that allows the image stream to run at a different frequency to the video input.

It has the following features:

- Support for sequential and parallel color planes (different data widths and formats)
- Support for different data streams:
  - BT656 (Composite or SD, HD & 3G SDI)
  - RGB (DVI)
- Configurable FIFO size
- Support for clock domain crossing
- Feedback about FIFO over/underflow
- SOPC Builder ready

Two instances of the Clocked Video Input block are required, one for each video stream. Both instances are configured for:

- 20-bit HD SDI (BT656) input
- FIFO depth of two 1080p lines. Each line contains 1,920 samples giving a FIFO depth of 3,840 and a width of 20 bits (9.4Kbit)
- Resolution change detection and propagation (stream 2 only)

Chroma Resampler MegaCore Function

Two instances of the Chroma Resampler MegaCore Function are required. Both instances are configured for:

- Input of two 10-bit color planes in parallel (Y′ and alternating Cb or Cr), 4:2:2
- Output of three10-bit color planes in parallel, 4:4:4
- Luma adaptive algorithm for horizontal resampling

Stream 1 has run-time control turned off with the resolution fixed as 1920×1080.

Stream 2 has run-time control turned on with the resolution variable between 640×360 and 1920×1080.

For more information about the Chroma Resampler MegaCore function, refer to the *Video and Image Processing Suite User Guide*.

Color Space Converter MegaCore Function

Two instances of the Color Space Converter MegaCore function are required. Both instances are configured for:

- Input of three 10-bit color planes in parallel (Y'CbCr)
- Output of three 8-bit color planes in parallel (R′G′B′)
- Y'CbCr: HDTV to Computer R'G'B' coefficients

Stream 1 has the resolution fixed as 1920×1080.

There is currently no run-time support for this MegaCore function but stream 2 must be configured for a resolution which works for all input resolutions between 640×360 and 1920×1080. The greatest common divisor of the supported range of resolutions should be used as compile time parameter; for example, use 640×360 if only 1920×1080, 1280×720, and 640×360 are supported. In the reference design, the resolution is set up as 80×36 pixels to support a wide range of input resolutions.

For more information about the Color Space Converter MegaCore function, refer to the *Video and Image Processing Suite User Guide*.

Deinterlacer MegaCore Function

The Deinterlacer MegaCore function is configured for:

- Fixed resolution of 1920×1080
- Input of three 8-bit color planes in parallel (R'G'B') at 1080i60
- Output of three 8-bit color planes in parallel (R'G'B') at 1080p60
- Motion-adaptive deinterlacing method
- Double-buffering with Avalon-MM port width set to 256 bits

For more information about the Deinterlacer MegaCore function, refer to the *Video and Image Processing Suite User Guide*.

Scaler MegaCore Function

Two instances of the Scaler MegaCore function are required. Both instances are configured for:

- Input and output of three 8-bit color planes in parallel (R'G'B')
- Downscale to 640×360 output resolution
- Polyphase mode with 12×12 taps and Lanczos-2 coefficients

Stream 1 has run-time control turned off with the resolution fixed as 1920×1080.

Stream 2 has run-time control turned on with the resolution variable between 640×360 and 1920×1080.

For more information about the Scaler MegaCore function, refer to the *Video and Image Processing Suite User Guide*.

Frame Buffer (Beta) MegaCore Function: Triple Buffers 1, 2, and 3

The Frame Buffer (Beta) MegaCore function takes image stream frames and buffers them into memory using an Avalon-MM connection (in this case DDR2 memory). The Frame Buffer can also drop or repeat frames where necessary to smooth out the data flow. This block, which will be part of the Video and Image Processing Suite in a future release, has the following features:

- Parameterizable GUI
- Support for different frame width/heights
- Support for different sequential/parallel color planes and different data widths
- Support for different memory data widths
- SOPC Builder ready

Three instances of the Frame Buffer MegaCore function are required, one for each input stream, and one for the output stream after the Alpha Blending Mixer. All instances are configured for:

- 24-bit wide Avalon-ST source and sink
- Single color plane (The triple buffer does not care that it actually uses three 8 bit color planes in parallel)
- 256-bit wide Avalon-MM read and write masters (for 64-bit DDR2)

Both input streams (Triple Buffers 1 and 2) are configured for:

- Resolution of 640×360 (after downscaling)
- Both frame dropping and frame repeating allowed

The output stream (Triple Buffers 3) is configured for:

- Resolution of 1920×1080
- Only frame repeating allowed

DDR2 SDRAM High Performance Controller MegaCore Function

This is the controller block for the external DDR2 SDRAM required as buffer for the Deinterlacer and the three Triple Buffers described above. It is configured for:

- Micron MT9HF6472AY-5EB38 (72-bit, 512MByte, 533MT/s, CL4, 266.7MHz)
- Data width set to use 64 bits (SOPC Builder cannot handle non power of 2 data widths)
- Memory set up in Half-Rate mode (266.7MHz internally, 133.35MHz externally)

For more information about the DDR2 SDRAM High Performance Controller MegaCore Function, refer to the *DDR and DDR2 SDRAM High Performance Controller User Guide*.

Alpha Blending Mixer MegaCore Function

This block mixes five input layers under software control at run-time. It is configured for:

- Four input layers:
  - Layer 0 (background) - 1920×1080, blue.
  - Layer 1 (stream 1) - 1920×1080, output from the motion adaptive deinterlacer (through FIFO).
  - Layer 2 (stream 1) - 640×360, output from fixed scaler.

  - Layer 3 (stream 2) - 640×360, output from run-time configurable scaler or variable resolution output of color space converter (through FIFO) depending on viewing mode.
  - Layer 4 (graphics) - 1920×1080, graphics overlay upscaled from 960×540. This layer includes an alpha channel containing transparency information on a per pixel basis.
- 1920×1080 output mixed according to five modes (see Figures 4, 5, and 6 on page 6):
  - Thumbnail view: Layers 2 and 3 side-by-side on layer 4. Layers 2 and 3 are visible due to transparent regions on layer 4.
  - Overlay view (Stream 1): Layers 1 and 4 together. Parts of layer 1 are visible due to transparent and semi-transparent regions on layer 4.
  - Video view (Stream 1): Layer 1 only.
  - Overlay view (Stream 2): Layers 3 and 4 together. Parts of layer 3 are visible due to transparent and semi-transparent regions on layer 4. Parts of the background (layer 0) are visible if the resolution of stream 2 is less than 1920×1080.
  - Video view (Stream 2): Layer 4, with some of the background (layer 0) visible if the resolution of stream 2 is less than 1920×1080.

The FIFOs buffering samples for layer 1 need to be disabled (and data discarded) if the layer is not selected by the current mode while `din_ready` for this layer must be `1`, in order to prevent the entire system from stalling.

For more information about the Alpha Blending Mixer MegaCore function, refer to the *Video and Image Processing Suite User Guide*.

Control Block (Nios II Processor)

This block is based on a Nios II embedded processor connected to DDR2-SDRAM, together with the Video and Image Processing Suite MegaCore functions, through an Avalon-MM master. The Control block initializes the run-time reconfigurable blocks of stream 2 and of the Alpha Blending Mixer MegaCore function at startup, or after mode change as caused by user interface interaction. The processor is also responsible for rendering the graphical overlay.

After resolution change detection at source 2, layer 3 of the mixer needs to be disabled, and the run-time configurable Chroma Resampler, Color Space Converter and Scaler MegaCore blocks for stream 2 need to be stopped and restarted (for parameter reconfiguration to take place). During this time, the Clocked Video Input block is isolated from the rest of the data path of stream 2, while the data path is drained of the frames of the old resolution which are padded to the correct frame length.

When a new stable resolution is detected, the Clocked Video Input block is reconnected to the rest of the data path and the blocks in stream 2 are restarted.

Clocked Video Output (Beta) MegaCore Function

The Clocked Video Output (Beta) MegaCore function takes an Avalon-ST video stream and converts it to a clocked video stream (reconstructing blanking information). This block, which will be part of the Video and Image Processing Suite in a future release, provides clock domain crossing that allows the Avalon-ST image stream to run at a different frequency to the clocked video output. It has the following features:

- Compile time parameterizable GUI
- Support for sequential and parallel color planes (different data widths and formats)
- Support for different data streams:
  - BT656 (Composite or SD, HD & 3G SDI)
  - RGB (DVI)
- Configurable FIFO size
- Supports clock domain crossing
- Feedback about FIFO over/underflow
- SOPCB ready

The Clocked Video Output block is configured for:

- 24-bit DVI (RGB) output
- FIFO depth of 2 1080p lines. Each line contains 1920 samples giving a FIFO depth of 3,840 and a width of 20 bits (9.4Kbit)

DVI TX Controller

The DVI TX Controller controls the DVI transmitter block on the Stratix II GX Audio Video development board to output the video stream. This block provides:

- Compile time parameterizable HDL
- Support for different resolutions (720p30/60 and 1080p30/60)

The DVI TX Controller block is configured for:

- 24-bit (RGB), 1080p60 (1920×1080) output
- 148.5MHz output frequency

Avalon-MM to Avalon-ST Block

This block reads pixels over a 256-bit wide Avalon-MM interface, and streams them out as an image stream. It is used for reading the graphical overlay layer from memory.

Pixels are described in memory using 16-bits per pixel RGB565 format (5-bit red, 6-bit green, 5-bit blue). Sixteen pixels are read at a time over the 256-bit Avalon-MM interface, and 32 such accesses are performed in a burst. Thus, a single burst to memory consists of 512 pixels. Each pixel is transmitted out over Avalon-ST using 24 bits (8-bits for each color).

The Avalon-MM to Avalon-ST block provides a slave control port to allow the base address of the Frame Buffer to be set. For each frame, the module reads 960×540 pixels incrementally from this address. It wraps back at the end of the frame.

Alpha Generator

This block detects fixed colors on a 24-bit Avalon-ST interface, and generates suitable 8-bit transparency (alpha) information. The block contains a look-up table with 24-bit colors to detect, 24-bit colors to replace, and 8-bit alpha values to insert. This look-up table contains two entries and can be controlled by the processor via a slave interface.

When a pixel is processed by the module, it is checked against the detect colors in the look-up table. If it is not found, then the original pixel color is output, along with a fully opaque alpha value. If a match is found, then the alpha value and output color are taken from the table.

Priority Arbiter

The reference design includes a custom priority arbiter, whose job is to ensure that sufficient memory bandwidth remains available to allow the video cores to function, even though a Nios II processor is present in the system. The arbiter has three slave ports and one master port. The video slave port accepts 256-bit wide burst accesses of up to 32 beats in length. The DMA slave port accepts 256-bit wide burst accesses of up to 32 beats in length. The Nios II slave port accepts 32-bit wide single accesses. The master port issues 256-bit wide burst accesses of up to 32 beats in length.

The high priority masters should be connected to the video port. SOPC Builder inserts round-robin arbitration to share the video port between these masters. If no accesses are in progress, this master is granted the memory. If an access is in progress, the master is granted the memory as soon as it completes.

The medium priority masters should be connected to the DMA port. SOPC Builder inserts round-robin arbitration to share the DMA port between these masters. If no accesses are in progress, this master is granted the memory. If an access is in progress, the master is granted the memory as soon as it completes, unless the video slave port is being requested, in which case the video port wins.

The Nios II instruction and data masters should be connected to the Nios II port using SOPC Builder arbitration shares of eight. The priority arbiter includes a width adaptor for converting eight accesses of width 32 (a cache line flush or fill) into a single access of width 256. Accesses from the Nios II processor into the width adaptor circuit are granted as long as they do not require an access to memory. When the access completes the cache line and requires access to DDR, the arbiter will block the Nios II processor until no other masters require the memory.

Clock Domains

The Nios II processor and memory controller subsystem run at 133.35MHz. The remainder of the SOPC Builder system, including the video datapath, run at 148.5MHz.

The DDR2 memory runs at its maximum rate of 266MHz. This requires the memory controller to run in half-rate mode.

The Clocked Video Input and Clocked Video Output blocks provide clock domain crossing which allows the DVI output and SDI input to run at the speed of the relevant standard being used.

Clock domain crossing is also used in the Deinterlacer and the Triple Buffers, as the Avalon-ST based data path runs at 148.5MHz, while the Avalon-MM based memory connections run at 133.35 MHz.

Reconfiguration Sequence

When the resolution changes at the input of video stream 2, the following sequence occurs:

1. The Clocked Video Input block interrupts the processor when the original resolution is lost.

2. The Nios II processor hides layer 3 of the mixer, if it is currently being displayed.

3. The Clocked Video Input block interrupts the Nios II processor when the new resolution signal has stabilized.

4. The Nios II processor isolates the Clocked Video Input block from the rest of the data path. The current frame in the Clocked Video Input block then gets drained out, while the incomplete frame in the rest of the data path gets padded to a full resolution frame.

5. The Control block stops the Clocked Video Input block, the Chroma Resampler, the Scaler, and the Triple Buffer in stream 2.

6. The Control block writes the new resolution information to the corresponding registers of the Chroma Resampler, Scaler, Triple Buffer and Mixer.

7. The Control block reconnects the Clocked Video Input block to the data processing blocks - these get restarted and resume processing at the new resolution.

8. The Control block re-enables layer 3 of the Mixer, depending on the current mode.

Memory Bandwidth Calculations

Access to external memory is required (through the DDR2 SDRAM High Performance Memory Controller) for the Motion Adaptive Deinterlacer (five masters), the three Triple Buffers (two masters each), the Nios II processor (two masters) and the Avalon-MM to image stream converter on the graphics layer (one master).

A priority arbiter is used to ensure that the Nios II processor does not use too much memory bandwidth and cause the video stream to become corrupt. This arbiter is arranged as follows:

- The processor is the lowest priority, as a reduction of memory bandwidth here will only cause the GUI responsiveness to be reduced.
- The Deinterlacer write path on stream 1, the Frame Buffer write path on stream 2, and the output Frame Buffer read path are the highest priority. As a loss of data here would cause video sync to be lost.
- All other masters are medium priority.

Motion Adaptive Deinterlacer

- Input format: 1080i60
  1920 × 1080 × 24bits × 60/2s = 1.493Gbit/s

- Output format: 1080p60
  1920 × 1080 × 24bits × 60 = 2.986Gbit/s

- Memory access:
  1 × write at input rate: 1.493Gbit/s
  1 × write at output rate: 2.986Gbit/s
  3 × read at output rate: 8.958Gbit/s

- Total: 13.437Gbit/s

Triple Buffer 1 (Steam 1 after Scaling)

- Input format: 640×360 progressive at 60Hz
  640 × 360 × 24bits × 60/s = 0.332Gbit/s

- Output format: 640×360 progressive at 60Hz
  640 × 360 × 24bits × 60/s = 0.332Gbit/s

- Memory access:
  1 × write at input rate: 0.332Gbit/s
  1 × write at output rate: 0.332Gbit/s

- Total (per triple buffer): 0.664Gbit/s

Triple Buffer 2 (Steam 2 after Scaling)

- Input format: Between 640×360 and 1920×1080 progressive at 60Hz
  Minimum: 640 × 360 × 24bits × 60/s = 0.332Gbit/s
  Maximum: 1920 × 1080 × 24bits × 60/s = 2.986Gbit/s

- Output format: Between 640×360 and 1920×1080 progressive at 60Hz
  Minimum: 640 × 360 × 24bits × 60/s = 0.332Gbit/s
  Maximum: 1920 × 1080 × 24bits × 60/s = 2.986Gbit/s

- Memory access:
  1 × write at input rate: Between 0.332Gbit/s and 2.986Gbit/s
  1 × write at output rate: Between 0.332Gbit/s and 2.986Gbit/s

- Total (per triple buffer): Between 0.664Gbit/s and 5.972Gbit/s

Triple Buffer 3 (Steam 1 after Mixing)

- Input format: 1080p60
  1920 × 1080 × 24bits × 60/s = 2.986Gbit/s

- Output format: 1080p60
  1920 × 1080 × 24bits × 60/s = 2.986Gbit/s

- Memory access:
  1 × write at input rate: 2.986Gbit/s
  1 × write at output rate: 2.986Gbit/s

- Total (per triple buffer): 5.972Gbit/s

Graphics Layer

- Memory access:
  1 × read master 960×540 at 60Hz
  960 × 540 × 16bits × 60/s = 0.500Gbit/s

The Nios II processor requires some extra bandwidth for its instruction and data masters, depending on the nature of its current processing.

Total Bandwidth

- Deinterlacer: 14.437Gbit/s
- Triple Buffer 1: 0.664Gbit/s
- Triple Buffer 2: Between 0.664Gbit/s and 5.972Gbit/s
- Triple Buffer 3: 5.972Gbit/s
- Total: Between 21.237Gbit/s and 26.545Gbit/s

The Stratix II GX development board when used with the Micron MT9HTF6472AY-53EB3 high-performance DDR2 SDRAM provides a maximum theoretical bandwidth of:

266.7 MHz × 64 bits × 2 (both clock edges used) = 34.133 Gbit/s

This results in a memory access efficiency requirement of over 60%.

Memory bandwidth efficiency is determined by a number of factors, such as randomness of addresses, refresh rate, turnaround times between reads and writes, and burst lengths. Altera's memory controllers can reach an efficiency of up to about 90% if the access conditions are right (long bursts of writes to the same column followed by long bursts of reads).

The use of a half-rate memory controller in order to satisfy the memory bandwidth requirements means that the local interface width between memory controller and internal FPGA logic is 256 bits (= 4 × 64 bits). Both DDR2 memory and memory controller will run at 266MHz, while the internal FPGA blocks will run at half this rate, that is, 133MHz.

Replacing the SDI Input with DVI

An all DVI system is much simpler and can be produced by the following steps:

1. Replace the SDI MegaCore function with a DVI RX Controller.
2. Configure the Clocked Video Input (Beta) MegaCore function for the DVI input.
3. Remove the Chroma Resampler and Color Space Converter MegaCore functions.
4. Regenerate the SOPC Builder system and recompile the Quartus II project.

Review the Example Design

This section describes how you can open the High Definition (HD) Video Monitoring Reference Design components in SOPC Builder.

To review the complete High Definition (HD) Video Monitoring Reference Design in SOPC Builder perform the following steps:

1. Run the Quartus II software to ensure the *QUARTUS_ROOTDIR* environment variable is correctly set.
2. Close the Quartus II software.
3. In Windows Explorer, browse to ***<install directory>*\docs** and double-click on **setup.bat** to install the Video and Image Processing toolkit blocks.
4. Re-open the Quartus II software.
5. Choose Open Project (File menu), browse to the ***<install directory>*** and select the Quartus II project file: **M4_all_top.qpf**
6. Choose **SOPC Builder** from the Tools menu in the Quartus II software.

If any blocks are missing from your SOPC Builder project, check that step 3 completed without errors. If necessary, you can add any missing directories to your IP Search Path by choosing **Options** from the Tools menu in SOPC Builder.

The complete SOPC Builder design is shown in (Figure 8 on page 21, Figure 9 on page 22, and Figure 10 on page 23).

Figure 8. Video Monitoring Reference Design in SOPC Builder (Part 1 of 3)

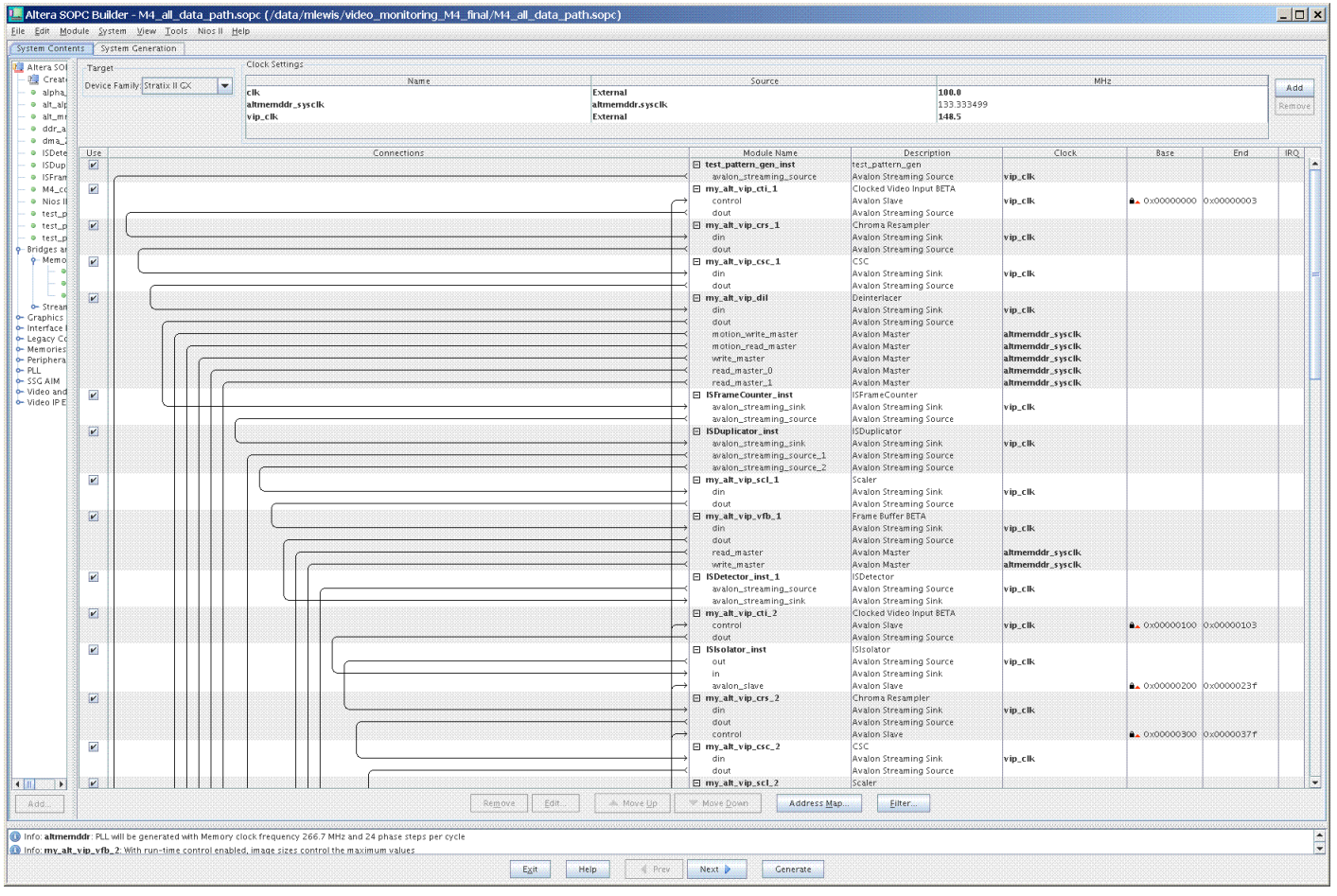


Figure 9. Video Monitoring Reference Design in SOPC Builder (Part 2 of 3)

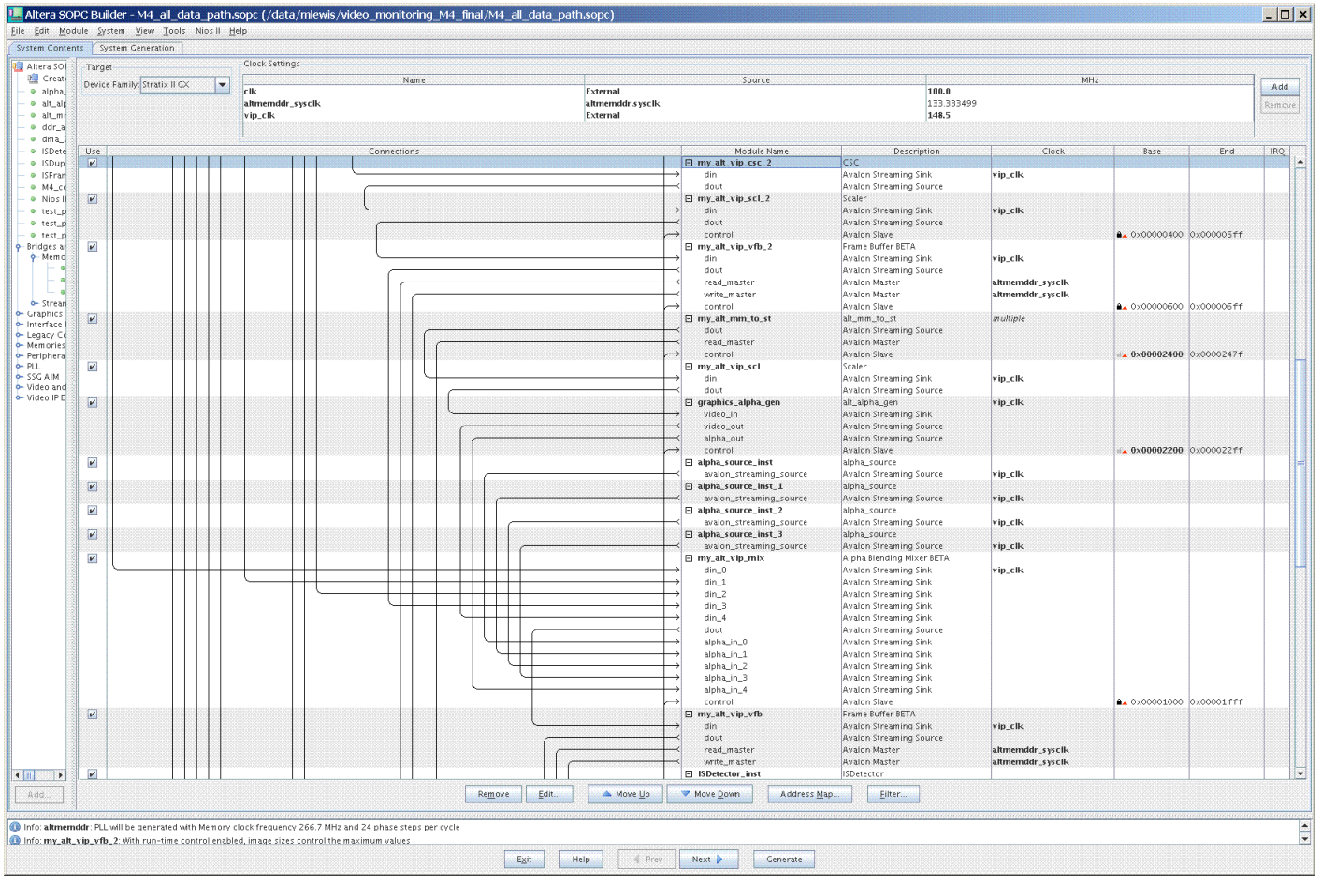
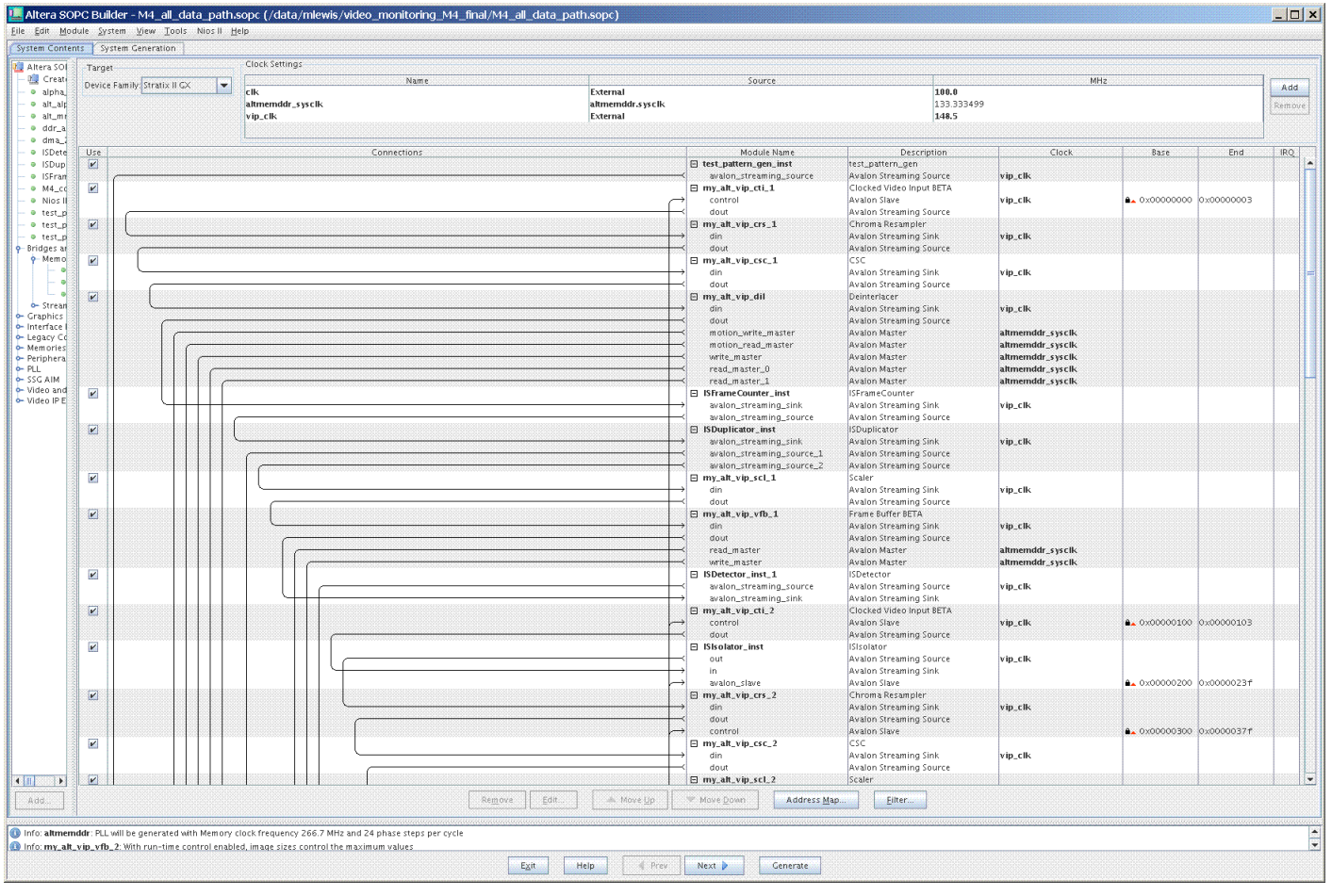


Figure 10. Video Monitoring Reference Design in SOPC Builder (Part 3 of 3)



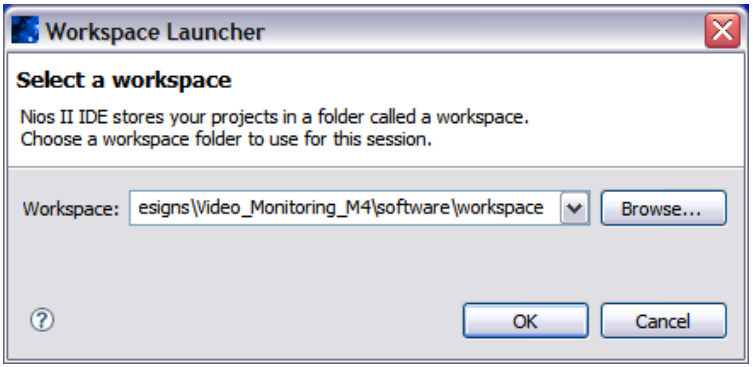
The SOPC Builder system reports eleven errors stating that pipeline bridge address ranges overlap although this is a valid system. This is because the v7.2 version of SOPC Builder incorrectly validates the system when Avalon-MM masters from a single IP function use more than one pipeline bridge. To generate the system, ignoring the errors, hold down the **Ctrl** key and click **Generate**.

Building the Software in the Nios II IDE

Perform the following steps to build the software in the Nios II Integrated Development Environment (IDE):

1. Start the Nios II IDE, v7.2 software.
2. Choose **Switch Workspac**e from the File men and browse to the **software** subdirectory of the M4 design install directory.

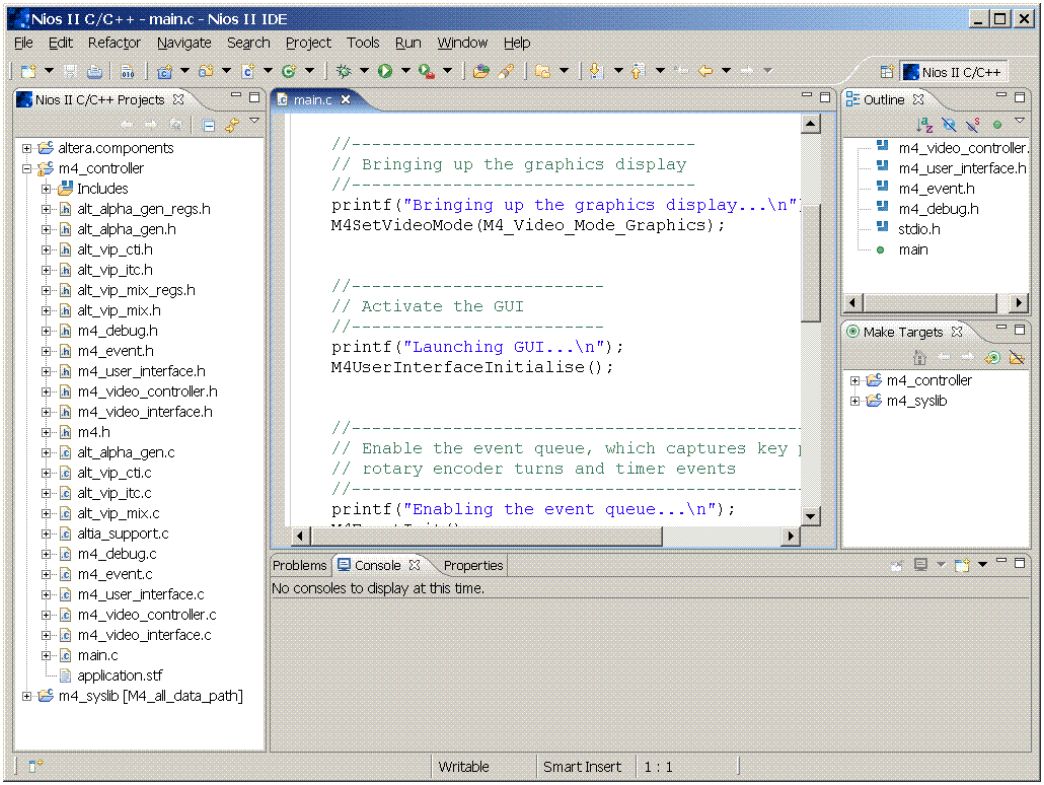
Figure 11. Nios II IDE Workspace Launcher



3. Add `workspace` to the end of the path name and click **OK** to create a new workspace.
4. Choose **Import** from the File menu and click on **Altera Nios II** in the Import dialog box. Choose **Existing Nios II IDE project into workspace** and click **Next**.
5. Browse to the application project (**m4_controller**) and click **Next**.
6. Repeat step 5 for the library project (**m4_syslib**) and click **Next**.
7. Browse to the PTF file (**M4_all_data_path.ptf**) in the Quartus II project directory and confirm that `cpu` appears in the **CPU** field. Click **Finish** to import the project from the file system.

8. Check that the application project (**m4_controller**) and system library project (**m4_syslib**) are shown in the workspace (Figure 12).

Figure 12. Nios II Integrated Development Environment (IDE) Workspace



9. Browse the application source code listed below **m4_controller**.

10. Right click on **m4_controller** and choose **System Library Properties** to browse the library properties.

11. Right click on **m4_controller** and select **Build Project**. Confirm that the **debug** directory (containing the **m4_controller.elf** file) appears after a few minutes.

12. After programming the development board with hardware, right click on **m4_controller** and select **Run As->Nios II Hardware** to download the **.elf** file.

Conclusion

The High Definition (HD) Video Monitoring Reference Design demonstrate a re-usable and flexible video framework for rapid development of video and image processing designs.

The use of standard open interfaces and protocols throughout the system allows you to build further applications, by re-using parameterizable IP from the Altera IP library or by adding your own IP to the framework.

The video framework does not preclude use of HDL to connect the IP components. However, the HD Video Monitoring Reference Designs demonstrate that the SOPC Builder environment significantly accelerates system design by:

- Automatic generation of an application specific switch fabric and ability to insert a custom priority arbitration scheme.
- Providing an abstracted view of the video system.
- Detecting and displaying Altera and user IP in an immediately accessible form.

Revision History

Table 1 shows the revision history for the *AN-524: High Definition (HD) Video Monitoring Reference Design* application note.

Table 1. AN-524 Revision History

Version	Date	Errata Summary
1.0	April 2008	First release of this application note.

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