

Arria® II Device Family Pin Connection Guidelines

PCG-01007-1.8

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The use of the pin connection guidelines for any particular design should be verified for device operation, with the datasheet and Altera.

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Arria II GX Pin Name	Arria II GZ Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
Clock and PLL Pins				
CLK[4:15]	NA	Clock, Input	Single ended clock input pin.	Connect unused pins to GND.
DIFFCLK[0:5]p	NA	Clock, Input	Clock input pin for differential clock input. OCT Rd is not supported.	Connect unused pins to GND.
DIFFCLK[0:5]n	NA	Clock, Input	Negative clock input for differential clock input. OCT Rd is not supported	Connect unused pins to GND.
PLL_[1:4]_CLKOUT1p	NA	I/O, Clock	PLL[1:4]_CLKOUT1 (except PLL1 and PLL3 in EP2AGX125 and EP2AGX260) supports 2 clock I/O pins, configured either as one single ended I/O or one differential I/O pair. PLL1 and PLL3 in EP2AGX125 and EP2AGX260 support 6 clock I/O pins, configured either as 3 single ended I/Os or 3 differential I/O pairs.	When not using this pin as a clock output, this pin may be used as a user I/O. When not using these pins, connect them as defined in Quartus II software. See Note 15.
PLL_[1:4]_CLKOUT1n	NA	I/O, Clock	PLL[1:4]_CLKOUT1 (except PLL1 and PLL3 in EP2AGX125 and EP2AGX260) supports 2 clock I/O pins, configured either as one single ended I/O or one differential I/O pair. PLL1 and PLL3 in EP2AGX125 and EP2AGX260 support 6 clock I/O pins, configured either as 3 single ended I/Os or 3 differential I/O pairs.	When not using this pin as a clock output, this pin may be used as a user I/O. When not using these pins, connect them as defined in Quartus II Software. See Note 15.
PLL_[1,3]_CLKOUT[2:3]p	NA	I/O, Clock	PLL1 and PLL3 in EP2AGX95, EP2AGX125, EP2AGX190, and EP2AGX260 support 6 clock I/O pins, configured either as 3 single ended I/Os or 3 differential I/O pairs.	When not using this pin as a clock output, this pin may be used as a user I/O. When not using these pins, connect them as defined in Quartus II software. See Notes 9 and 15.
PLL_[1,3]_CLKOUT[2:3]n	NA	I/O, Clock	PLL1 and PLL3 in EP2AGX95, EP2AGX125, EP2AGX190, and EP2AGX260 support 6 clock I/O pins, configured either as 3 single ended I/Os or 3 differential I/O pairs.	When not using this pin as a clock output, this pin may be used as a user I/O. When not using these pins, connect them as defined in Quartus II software. See Notes 9 and 15.
NA	CLK[1,3,8,10]p	Clock, Input	Dedicated high speed clock input pins 1, 3, 8, and 10 that can also be used for data inputs. OCT Rd is not supported on these pins.	Connect unused pins to GND.
NA	CLK[1,3,8,10]n	Clock, Input	Dedicated negative clock input pins for differential clock input that can also be used for data inputs. OCT Rd is not supported on these pins.	Connect unused pins to GND.
NA	CLK[0,2,9,11]p	I/O, Clock	These pins can be used as I/O pins or clock input pins. OCT Rd is supported on these pins.	These pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
NA	CLK[0,2,9,11]n	I/O, Clock	These pins can be used as I/O pins or negative clock input pins for differential clock inputs. OCT Rd is supported on these pins.	These pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
NA	CLK[4:7,12:15]p	I/O, Clock	These pins can be used as I/O pins or clock input pins. OCT Rd is not supported on these pins.	These pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
NA	CLK[4:7,12:15]n	I/O, Clock	These pins can be used as I/O pins or negative clock input pins for differential clock inputs. OCT Rd is not supported on these pins.	These pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
NA	PLL_[L1,L4,R1,R4]_CLKp	Clock, Input	Dedicated clock input pins to PLL L1, L4, R1, and R4 respectively. OCT Rd is not supported on these pins.	Connect unused pins to GND.
NA	PLL_[L1,L4,R1,R4]_CLKn	Clock, Input	Dedicated negative clock input pins for differential clock input to PLL L1, L4, R1, and R4 respectively. OCT Rd is not supported on these pins.	Connect unused pins to GND.
NA	PLL_[L1, L2, L3, L4]_CLKOUT0n PLL_[R1, R2, R3, R4]_CLKOUT0n	I/O, Clock	Each left and right PLL supports 2 clock I/O pins, configured either as 2 single ended I/O or one differential I/O pair. When using both pins as single ended I/Os, PLL_#_CLKOUT0n can be the clock output while the PLL_#_FB_CLKOUT0p is the external feedback input pin.	These pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
NA	PLL_[L1, L2, L3, L4]_FB_CLKOUT0p PLL_[R1, R2, R3, R4]_FB_CLKOUT0p	I/O, Clock	Each left and right PLL supports 2 clock I/O pins, configured either as 2 single ended I/O or one differential I/O pair. When using both pins as single ended I/Os, PLL_#_CLKOUT0n can be the clock output while the PLL_#_FB_CLKOUT0p is the external feedback input pin.	These pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.

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Arria II GX Pin Name	Arria II GZ Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
NA	PLL_[T1,T2,B1,B2]_FBp/CLKOUT1	I/O, Clock	Dual purpose I/O pins that can be used as two single-ended outputs or one differential external feedback input pin.	These pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
NA	PLL_[T1,T2,B1,B2]_FBn/CLKOUT2	I/O, Clock		These pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
NA	PLL_[T1,T2,B1,B2]_CLKOUT[3,4]	I/O, Clock	These pins can be used as I/O pins or two single-ended clock output pins.	These pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
NA	PLL_[T1,T2,B1,B2]_CLKOUT0p	I/O, Clock	I/O pins that can be used as two single-ended clock output pins or one differential clock output pair.	These pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
NA	PLL_[T1,T2,B1,B2]_CLKOUT0n	I/O, Clock		These pins can be tied to GND or left unconnected. If unconnected, use Quartus II software programmable options to internally bias these pins. They can be reserved as inputs tristate with weak pull up resistor enabled, or as outputs driving GND.
Configuration/JTAG Pins (See Note 16)				
nIO_PULLUP	nIO_PULLUP	Input	Dedicated input that chooses whether the internal pull-ups on the user I/O pins and dual-purpose I/O pins (DATA[1:7], CLKUSR, INIT_DONE, DEV_OE, DEV_CLRn) are on or off before and during configuration. A logic high (1.5 V, 1.8 V, 2.5 V, 3.0 V, or (3.3 V, Arria II GX only) turns off the weak pull-up, while a logic low turns them on.	nIO-PULLUP can be tied directly to (VCCIO3C for Arria II GX only), (VCCPGM for Arria II GZ only) using a 1kΩ pull-up resistor, or tied directly to GND depending on the desired functionality. Refer to the description column.
MSEL[0:3]	MSEL[0:3]	Input	Configuration input pins that set the FPGA device configuration scheme.	These pins are internally connected through a 5-kΩ resistor to GND. Do not leave these pins floating. When these pins are unused connect them to GND. Depending on the configuration scheme used these pins should be tied to (VCCPD3C for Arria II GX only), (VCCPGM for Arria II GZ only) or GND. Refer to the "Configuration, Design Security, and Remote System Upgrades" chapter in the Arria II GX Handbook. If only JTAG configuration is used, connect these pins to ground.
nCE	nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled.	In multi-device configuration, nCE of the first device is tied low while its nCEO pin drives the nCE of the next device in the chain. In single device configuration and JTAG programming, nCE should be connected to GND.
nCONFIG	nCONFIG	Input	Dedicated configuration control input. Pulling this pin low during user-mode will cause the FPGA to lose its configuration data, enter a reset state, and tri-state all I/O pins. Returning this pin to a logic high level will initiate reconfiguration.	If the configuration scheme uses an enhanced configuration device or EPC2, nCONFIG can be tied directly to the nINIT_CONF pin of the configuration device. If this pin is not used, it requires a connection directly or through a 10-kΩ resistor to (VCCIO3C for Arria II GX only), (VCCPGM for Arria II GZ only).

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Arria II GX Pin Name	Arria II GZ Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
CONF_DONE	CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration done pin. As a status output, the CONF_DONE pin drives low before and during configuration. Once all configuration data is received without error and the initialization cycle starts, CONF_DONE is released. As a status input, CONF_DONE goes high after all data is received. Then the device initializes and enters user mode. It is not available as a user I/O pin.	Connect this pin to a 10-kΩ pull-up resistor to an acceptable voltage for all devices in the chain which satisfies the input voltage of the receiving device. If internal pull-up resistors on the enhanced configuration device are used, external 10-kΩ pull-up resistors should not be used on this pin.
nCEO	nCEO	I/O, Output (open-drain)	Output that drives low when device configuration is complete. This pin can be used as regular I/O if not used for device configuration.	When not using this pin, you can leave it unconnected. During multi-device configuration, this pin feeds the nCE pin of a subsequent device. In this case, tie the 10-kΩ pull-up resistor to an acceptable voltage for all devices in the chain which satisfies the input voltage of the receiving device. During single device configuration, this pin can be used as a regular I/O.
nSTATUS	nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin. The FPGA drives nSTATUS low immediately after power-up and releases it after POR time. As a status output, the nSTATUS is pulled low if an error occurs during configuration. As a status input, the device enters an error state when nSTATUS is driven low by an external source during configuration or initialization. It is not available as an user I/O pin.	Connect this pin to a 10-kΩ pull-up resistor to an acceptable voltage for all devices in the chain which satisfies the input voltage of the receiving device. The OE and nCE pins of the enhanced configuration devices and EPC2 devices have optional internal programmable pull-up resistors. If internal pull-up resistors on the enhanced configuration device are used, external 10-kΩ pull-up should not be used on these pins. When not using external configuration devices, connect this pin to an external 10-kΩ pull-up resistor to (VCCIO3C for Arria II GX only), (VCCPGM for Arria II GZ only).
TCK	TCK	Input	Dedicated JTAG test clock input pin.	Connect this pin to a 1-kΩ pull-down resistor to GND.
TMS	TMS	Input	Dedicated JTAG test mode select input pin.	Connect this pin to a 1-kΩ - 10-kΩ pull-up resistor to VCCIO for Arria II GX or VCCPD for Arria II GZ. To disable the JTAG circuitry connect TMS to logic high via a 1-kΩ resistor.
TDI	TDI	Input	Dedicated JTAG test data input pin.	Connect this pin to a 1-kΩ - 10-kΩ pull-up resistor to VCCIO for Arria II GX or VCCPD for Arria II GZ. To disable the JTAG circuitry connect TDI to logic high via a 1-kΩ resistor.
TDO	TDO	Output	Dedicated JTAG test data output pin.	The JTAG circuitry can be disabled by leaving TDO unconnected.
NA	TRST	Input	Dedicated active low JTAG test reset input pin. TRST is used to asynchronously reset the JTAG boundary-scan circuit.	Utilization of TRST is optional. When using this pin ensure that TMS is held high or TCK is static when TRST is changed from low to high. If not using TRST, tie this pin to a 1-kΩ to 10-kΩ pull-up resistor to VCCPD. To disable the JTAG circuitry, tie this pin to GND.
NA	PORSEL	Input	Dedicated input which selects between a POR time of 4 -12 ms or 100 - 300 ms. A logic high (1.8V, 2.5V, 3.0V) selects a POR time of 4 -12 ms and a logic low selects POR time of 100 - 300 ms.	The PORSEL pin should be tied directly to VCCPGM or GND.
nCSO	nCSO	Output	Dedicated output control signal from the FPGA to the serial configuration device in AS mode that enables the configuration device.	When not programming the device in AS mode nCSO is not used. Also, when this pin is not used as an output then it is recommended to leave the pin unconnected.
ASDO	ASDO	Output	Control signal from the FPGA to the serial configuration device in AS mode used to read out configuration data.	When not programming the device in AS mode ASDO is not used. Also, when this pin is not used as an output then it is recommended to leave the pin unconnected.
DCLK	DCLK	I/O (PS, FPP) Output (AS)	Dedicated configuration clock pin. In PS and FPP configuration, DCLK is used to clock configuration data from an external source into the FPGA. In AS mode, DCLK is an output from the FPGA that provides timing for the configuration interface.	Do not leave this pin floating. Drive this pin either high or low.
CRC_ERROR	CRC_ERROR	I/O, Output (open-drain)	Active high signal that indicates that the error detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error detection circuit is enabled. This pin can be used as regular I/O if not used for CRC error detection.	When using this pin connect it to an external 10-kΩ pull-up resistor to an acceptable voltage for all devices in the chain which satisfies the input voltage of the receiving device. When not using this pin, it can be left floating.
DEV_CLRn	DEV_CLRn	I/O, Input	Optional pin that allows designers to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as programmed.	When the dedicated input DEV_CLRn is not used and this pin is not used as an I/O then it is recommended to tie this pin to ground.

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DEV_OE	DEV_OE	I/O, Input	Optional pin that allows designers to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design.	When the dedicated input DEV_OE is not used and this pin is not used as an I/O then it is recommended to tie this pin to ground.
DATA0	DATA0	Input	DATA[0] is a dedicated pin that is used for both the passive and active configuration modes	When the dedicated input for DATA[0] is not used on Arria II GX, then it is recommended to tie this pin to GND. For Arria II GZ, connect this pin as defined in the Quartus II software.
DATA[7:1]	DATA[7:1]	I/O, Input	Dual-purpose configuration input data pins. The DATA[7:0] pins can be used for byte-wide configuration. DATA[7:1] pins can also be used as user I/O pins after configuration, but not DATA0.	When the dedicated inputs for DATA[7:1] are not used and these pins are not used as an I/O then connect them as defined in Quartus. (See Note 15).
INIT_DONE	INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high at the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration.	When using this pin connect it to an external 10-kΩ pull-up resistor to an acceptable voltage for all devices in the chain which satisfies the input voltage of the receiving device. When not using this pin, it can be left floating or tied to GND.
CLKUSR	CLKUSR	I/O, Input	Optional user-supplied clock input. If this pin is not enabled for use as a user-supplied configuration clock, it can be used as an user I/O pin.	If the CLKUSR pin is not used as a configuration clock input and the pin is not used as an I/O then it is recommended to connect this pin to ground.
Differential I/O Pins (See Note 12)				
DIFFIO_RX_[T,B,R][##]p, DIFFIO_RX_[T,B,R][##]n	DIFFIO_RX_[T,B,L,R][##]p, DIFFIO_RX_[T,B,L,R][##]n	I/O, RX channel	Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins. For Arria II GX, these are true LVDS receiver channels with OCT Rd support. For Arria II GZ, only DIFFIO_RX_[L,R]* pins are true LVDS receiver channels with OCT Rd support.	When these IO pins are not used they can be tied to GND. Connect unused pins as defined in Quartus II software.
DIFFIO_TX_[T,B,R][##]p, DIFFIO_TX_[T,B,R][##]n	DIFFIO_TX_[L,R][##]p, DIFFIO_TX_[L,R][##]n	I/O, TX channel	These are true LVDS transmitter channels. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins. For Arria II GX if not used as true LVDS transmitter channels, these pins can be configured as true LVDS receiver channels without OCT Rd support (DIFFIN_[T,B,R][##][p,n]).	When these IO pins are not used they can be tied to GND. Connect unused pins as defined in Quartus II software.
DIFFIN_[T,B,R][##]p, DIFFIN_[T,B,R][##]n	NA	I/O, RX channel	These are true LVDS receiver channels without OCT Rd support. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used as true LVDS receiver channels without OCT Rd support, these pins can be configured as true LVDS transmitter channels (DIFFIO_TX_[T,B,R][##][p,n]). If not used for differential signaling, these pins are available as user I/O pin.	When these IO pins are not used they can be tied to GND. Connect unused pins as defined in Quartus II software.

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DIFFOUT_[T,B,R][##]p, DIFFOUT_[T,B,R][##]n	DIFFOUT_[T,B,L,R][##]p, DIFFOUT_[T,B,L,R][##]n	I/O, TX channel	<p>These are emulated LVDS output channels. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.</p> <p>On Arria II GX I/O banks there are true LVDS input buffers but no true LVDS output buffers. However, all user I/Os, including I/Os with true LVDS input buffers, (DIFFIO_RX_[T,B,R][##][p,n] , DIFFIN_[T,B,R][##][p,n]) can be configured as emulated LVDS output buffers.</p> <p>On Arria II GZ column I/O banks there are true LVDS input buffers but no true LVDS output buffers. However, all column user I/Os, including I/Os with true LVDS input buffers, can be configured as emulated LVDS output buffers.</p>	When these IO pins are not used they can be tied to GND. Connect unused pins as defined in Quartus II software.
External Memory Interface Pins (See Note 12)				
DQS[##][T,B,R]	DQS[##][T,B,L,R]	I/O, DQS	Optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry. The shifted DQS signal can also drive to internal logic.	When these IO pins are not used they can be tied to GND. Connect unused pins as defined in Quartus II software.
DQSn[##][T,B,R]	DQSn[##][T,B,L,R]	I/O, DQSn	Optional complementary data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry.	When these IO pins are not used they can be tied to GND. Connect unused pins as defined in Quartus II software. See Note 11.
DQ[##][T,B,R]	DQ[##][T,B,L,R]	I/O, DQ	Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important; however, use caution when making pin assignments if you plan on migrating to a different memory interface that has a different DQ bus width. Analyze the available DQ pins across all pertinent DQS columns in the pin list.	When these IO pins are not used they can be tied to GND. Connect unused pins as defined in Quartus II software.
CQ[##][T,B,R]	CQ[##][T,B,L,R]	DQS	Optional data strobe signal for use in QDR II SRAM. These are the pins for echo clocks.	When these IO pins are not used they can be tied to GND. Connect unused pins as defined in Quartus II software.
CQn[##][T,B,R]	CQn[##][T,B,L,R]	DQS	Optional complementary data strobe signal for use in QDR II SRAM. These are the pins for echo clocks.	When these IO pins are not used they can be tied to GND. Connect unused pins as defined in Quartus II software. See Note 11.
Reference Pins				
RUP[0:2]	RUP[1:8]A	I/O, Input	Reference pins for I/O banks. The RUP pins share the same VCCIO with the I/O bank where they are located. The external precision resistor RUP must be connected to the designated RUP pin within the bank. If not required, this pin is a regular I/O pin.	When the device does not use this dedicated input for the external precision resistor or as an I/O it is recommended that the pin be connected to the VCCIO of the bank in which the RUP pin resides or GND. When using OCT tie these pins to the required banks VCCIO through either a 25 Ω or 50 Ω resistor, depending on the desired I/O standard. Refer to the Arria II GX handbook for the desired resistor value for the I/O standard used.
RDN[0:2]	RDN[1:8]A	I/O, Input	Reference pins for I/O banks. The RDN pins share the same GND with the I/O bank where they are located. The external precision resistor RDN must be connected to the designated RDN pin within the bank. If not required, this pin is a regular I/O pin.	When the device does not use this dedicated input for the external precision resistor or as an I/O it is recommended that the pin be connected to GND. When using OCT tie these pins to GND through either a 25 Ω or 50 Ω resistor depending on the desired I/O standard. Refer to the Arria II GX handbook for the desired resistor value for the I/O standard used.
DNU	DNU	Do Not Use	Do Not Use (DNU).	Do not connect to power, ground or any other signal. These pins must be left floating.
NC	NC	No Connect	Do not drive signals into these pins.	When designing for device migration these pins may be connected to power, ground, or a signal trace depending on the pin assignment of the devices selected for migration. However, if device migration is not a concern leave these pins floating.

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Arria II GX Pin Name	Arria II GZ Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
Supply Pins (See Note 8 and 17)				
VCC	VCC	Power	VCC supplies power to the core and periphery.	<p>All VCC pins require a 0.9 V supply. Use the Arria II GX or Arria II GZ Early Power Estimator to determine the current requirements for VCC and other power supplies. To successfully power-up and exit POR, fully power VCC before VCCAUX begins to ramp. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 3, 6 and 17.</p> <p>For Arria II GX, with a proper isolation filter VCCD_PLL may be sourced from the same regulator as VCC. To support the startup current as reported by the Early Power Estimator (EPE) for Arria II GX devices, fully power VCC before VCCCB begins to ramp.</p> <p>For Arria II GZ, these pins may be tied to the same 0.9V plane as VCCHIP_L. With a proper isolation filter VCCD_PLL may be sourced from the same regulator as VCC.</p>
VCCD_PLL_[1:6]	VCCD_PLL_[L,R][1:4], VCCD_PLL_[T,B][1:2]	Power	Digital power for PLL[1:6] and PLL[L[1:4],R[1:4],T[1:2],B[1:2]].	<p>You are required to connect these pins to 0.9 V, even if the PLL is not used. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 3 and 6.</p> <p>For Arria II GX, with a proper isolation filter these pins may be sourced from the same regulator as VCC.</p> <p>For Arria II GZ, with a proper isolation filter these pins may be sourced from the same regulator as VCC and/or VCCHIP_L.</p>
VCCCB	VCCCB	Power	Configuration RAM bits power supply.	<p>Connect VCCCB to a 1.5 V power supply. These pins may be sourced from the same regulator as VCCH_GXB with a proper isolation filter. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 3, 6, and 7.</p> <p>For Arria II GX, use a linear regulator or switching power supply with ±5% maximum voltage ripple (See note 14). To support the startup current as reported by the Early Power Estimator (EPE) for Arria II GX devices, fully power VCC before VCCCB begins to ramp.</p> <p>For Arria II GZ, use a linear or low noise switching regulator.</p>
VCCA_PLL_[1:6]	VCCA_PLL_[L,R][1:4], VCCA_PLL_[T,B][1:2]	Power	Analog power for PLL [1:6] and PLL [L[1:4],R[1:4],T[1:2],B[1:2]].	<p>You are required to connect these pins to 2.5 V, even if the PLL is not used. It is advised to keep this pin isolated from other VCC for better jitter performance. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 3, 6, and 7.</p> <p>For Arria II GX, use an isolated linear regulator or switching power supply with ±5% maximum voltage ripple. These pins may share the same linear regulator as VCCA with a proper isolation filter. (See note 14)</p> <p>For Arria II GZ, use a linear or low noise switching regulator. With a proper isolation filter, these pins may be tied to the same regulator as VCCIO, VCCPD, VCCPGM and VCC_CLKIN, but only if each of these supplies require 2.5V sources. With a proper isolation filter these pins may be sourced from the same regulator as VCCAUX and VCCA_[L,R], but only if each of these rails requires 2.5V.</p>
NA	VCCAUX	Power	Auxiliary supply for configuration.	<p>VCCAUX can be connected to an isolated 2.5V linear or low noise switching power supply. With a proper isolation filter these pins may be sourced from the same regulator as VCCA_PLL and VCCA_[L,R], but only if each of these rails requires 2.5V. Also, with a proper isolation filter, these pins may be tied to the same regulator as VCCIO, VCCPD, VCCPGM, and VCC_CLKIN, but only if each of these supplies require 2.5V sources. To successfully power-up and exit POR, fully power VCC before VCCAUX begins to ramp. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 3, 6, 7 and 19.</p>
NA	VCCPGM	Power	Configuration pins power supply. Can be connected to 1.8V, 2.5V or 3.0V depending on the particular design.	<p>Connect this pin to either a 1.8V, 2.5V or 3.0V power supply. VCCPGM must ramp-up from 0V to VCCPGM within 100 ms when PORSEL is low or 4 ms when PORSEL is high to ensure successful configuration. When these pins require 2.5V they may be tied to the same regulator as VCC_CLKIN, VCCIO and VCCPD, but only if each of these supplies require 2.5V sources. VCC_CLKIN has a set voltage of 2.5V, so excluding VCC_CLKIN you may tie these pins to the same regulator as VCCPD and/or VCCIO as long as they all require the same voltage. Also, when these pins use 2.5V they may be sourced from the same regulator as VCCAUX and VCCA_PLL with a proper isolation filter. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 3 and 6.</p>

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Arria II GX Pin Name	Arria II GZ Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
VCCIO[3:8][A,B]	VCCIO[1:8][A,C], VCCIO[3,4,7,8]B	Power	These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all LVDS, LVCMOS(1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.0 V, (3.3 V, Arria II GX only)), HSTL(12, 15, 18), SSTL(15, 18, 2), 3.0 V PCI/PCI-X I/O as well as LVTTTL (1.8 V, 2.5 V, 3.0 V, (3.3 V, Arria II GX only)) I/O standards. VCCIO also supplies power to the input buffers used for LVCMOS(1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.0 V, (3.3 V, Arria II GX only)), 3.0 V PCI/PCI-X, and LVTTTL (1.8 V, 2.5 V, 3.0 V, (3.3 V, Arria II GX only)) I/O standards.	Connect these pin to 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.0 V, or (3.3 V, Arria II GX only) supplies, depending on the I/O standard connected to the specified bank. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 3 and 6. For Arria II GX, these pins may be tied to the same regulator as VCCPD, but only if each of these supplies require the same voltage level. For Arria II GZ, when these pins require 2.5V they may be tied to the same regulator as VCC_CLKIN, VCCPGM and VCCPD, but only if each of these supplies require 2.5V sources. VCC_CLKIN has a set voltage of 2.5V, so excluding VCC_CLKIN you may tie these pins to the same regulator as VCCPGM and/or VCCPD as long as they all require the same voltage. Also, when these pins use 2.5V they may be sourced from the same regulator as VCCAUX and VCCA_PLL with a proper isolation filter.
VCCIO[3,8]C	NA	Power	These are configuration and JTAG supply voltage pins for banks 3C and 8C. Each bank can support a different voltage level. For AS/PS/FPP configuration schemes, VCCIO8C supports 1.8 V, 2.5 V, 3.0 V or 3.3 V. JTAG can support 1.5 V, 1.8 V, 2.5 V, 3.0 V or 3.3 V.	Connect these pin to 1.5 V, 1.8 V, 2.5 V, 3.0 V, or 3.3 V supplies, depending on the I/O standard connected to the specified bank. When using configuration schemes that require external configuration devices, the voltage level of these pins must match that of the configuration device. These pins may be tied to the same regulator as VCCPD, but only if each of these supplies require the same voltage level. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 3 and 6.
VCCPD[3:8][A,B], VCCPD[3,8]C	VCCPD[1:8][A,C], VCCPD[3,4,7,8]B	Power	Dedicated power pins. This supply is used to power the I/O pre-drivers and the input buffers for HSTL/SSTL input buffers. This can be connected to (3.3 V Arria II GX only), 3.0 V or 2.5 V. For 3.3 V I/O standard connect VCCPD to 3.3 V, for 3.0 V I/O standard connect VCCPD to 3.0 V and for 2.5 V/1.8 V/1.5 V/1.2 V I/O standards connect VCCPD to 2.5 V.	The VCCPD pins require 2.5 V, 3.0 V, or (3.3 V, Arria II GX only) and must ramp-up from 0 V to 2.5 V, 3.0 V, or (3.3 V, Arria II GX only) within 100 ms to ensure successful configuration. When these pins require 2.5 V, 3.0 V, or (3.3 V, Arria II GX only) they may be tied to the same regulator as VCCIO, but only if each of these supplies require the same voltage level. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 3 and 6. For Arria II GZ VCCPD must ramp-up from 0V to VCCPD within 100 ms when PORSEL is low or 4 ms when PORSEL is high to ensure successful configuration. When these pins require 2.5V they may be tied to the same regulator as VCC_CLKIN, VCCPGM and VCCIO, but only if each of these supplies require 2.5V sources. VCC_CLKIN has a set voltage of 2.5V, so excluding VCC_CLKIN you may tie these pins to the same regulator as VCCPGM and/or VCCIO as long as they all require the same voltage. Also, when these pins use 2.5V they may be sourced from the same regulator as VCCAUX and VCCA_PLL with a proper isolation filter.
NA	VCC_CLKIN[3,4,7,8]C	Power	Differential clock input power supply for top and bottom I/O banks. Connect to 2.5V.	Connect these pins to 2.5V power source. These pins may be tied to the same regulator as VCCIO, VCCPGM and VCCPD, but only if each of these supplies require 2.5V sources. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Note 3. For Arria II GZ, with a proper isolation filter these pins may be sourced from the same regulator as VCCAUX and VCCA_PLL.
VCCBAT	VCCBAT	Power	Battery back-up power supply for design security volatile key register.	Connect this pin to a Non-volatile battery power source in the range of (1.2 V - 3.3 V, for Arria II GX) or 1.2 V - 3.0 V, for Arria II GZ) when using design security volatile key. 3.0 V is the typical power selected for this supply. When not using the volatile key, tie this to a 3.0 V supply or GND. Do not share this source with other FPGA power supplies.
GND	GND	Ground	Device ground pins.	All GND pins should be connected to the board ground plane.
VREF[3:8][A,B]N0	VREF[1:8][A,C], VREF[3,4,7,8]B	Power	Input reference voltage for each I/O bank. If a bank uses a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for the bank. These pins cannot be used as regular I/Os.	If VREF pins are not used, designers should connect them to either the VCCIO in the bank in which the pin resides or GND. Decoupling depends on the design decoupling requirements of the specific board. See Note 3.

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Arria II GX Pin Name	Arria II GZ Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
Transceiver Pins (See Note 8)				
NA	VCCHIP_L	Power	PCIe Hard IP digital power supply, specific to the left (L) side of the device.	All VCCHIP_L pins require a 0.9V supply. When not using HIP these pins may be connected to GND. These pins may be tied to the same 0.9V plane as VCC. With a proper isolation filter these pins may be sourced from the same regulator as VCCD_PLL. Decoupling for these pins depends on the design decoupling requirements of the specific board. See Notes 3 and 6.
NA	VCCR_[L,R]	Power	Analog power, receiver, specific to the left (L) side or right (R) side of the device.	VCCR_[L,R] can be connected to a 1.1V linear or low noise switching regulator. These pins may be tied to the same 1.1V plane as VCCL_GXB[L,R] and/or VCCT_[L,R]. However, for better jitter performance at high data rates this plane should be isolated from all other power supplies. Decoupling for these pins depends on the design decoupling requirements of the specific board design. See Notes 3, 6, 17, 18 and 19.
NA	VCCT_[L,R]	Power	Analog power, transmitter, specific to the left (L) side or right (R) side of the device.	VCCT_[L,R] can be connected to a 1.1V linear or low noise switching regulator. These pins may be tied to the same 1.1V plane as VCCL_GXB[L,R], and/or VCCR_[L,R]. However, for better jitter performance at high data rates this plane should be isolated from all other power supplies. Decoupling for these pins depends on the design decoupling requirements of the specific board design. See Notes 3, 6, 17, 18 and 19.
VCCL_GXB	VCCL_GXB[L,R][0:2]	Power	Supplies power to the transceiver PMA TX, PMA RX and clocking.	VCCL_GXB[L,R] can be connected to a 1.1V linear or low noise switching regulator. These pins may be tied to the same 1.1V plane as VCCT_[L,R] and/or VCCR_[L,R]. However, for better jitter performance at high data rates this plane should be isolated from all other power supplies. To enhance jitter performance, it is recommended to use a separate power supply for the respective transceiver blocks. Decoupling for these pins depends on the design decoupling requirements of the specific board design. See Notes 3, 6, 7 and 18.
VCCH_GXB	VCCH_GXB[L,R][0:2]	Power	Supplies power to the transceiver PMA output (TX) buffer.	Connect VCCH_GXB to a 1.5V power supply. These pins may be sourced from the same regulator as VCCCB with a proper isolation filter. Decoupling for these pins depends on the design decoupling requirements of the specific board design. See Notes 3, 6, 7 and 18. For Arria II GX, use a linear regulator or switching power supply with $\pm 5\%$ maximum voltage ripple. (See Note 14) For Arria II GZ, use a linear or low noise switching regulator.

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Arria II GX Pin Name	Arria II GZ Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
VCCA	VCCA_[L,R]	Power	Supplies power to the transceiver PMA regulator.	Decoupling depends on the design decoupling requirements of the specific board design. See Notes 3, 6, 7 and 18. For Arria II GX, connect VCCA to a 2.5V linear regulator or switching power supply with $\pm 5\%$ maximum voltage ripple. (See note 14) These pins may be sourced from the same linear regulator as VCCA_PLL with a proper isolation filter. For Arria II GZ, VCCA_[L,R] can be connected to a 2.5V or 3.0V linear or low noise switching regulator. Connect these pins to 3.0V if the TX PLL and/or RX CDR are configured at a base data rate > 4.25Gbps. Connect these pins to 2.5V or 3.0V if the TX PLL and/or RX CDR are configured at a base data rate \leq 4.25Gbps. For data rates \leq 4.25Gbps, if VCCA_[L,R] is 2.5V these pins may be sourced from the same linear regulator as VCCAUX and/or VCCA_PLL with a proper isolation filter.
GXB_RX[0:15]p	GXB_RX_[L,R][0:11]p	Input	High speed positive differential receiver channels.	These pins may be AC-coupled or DC-coupled when used. (Note 4) Connect all unused GXB_RXp pins either individually to GND through a 10-k Ω resistor or tie all unused pins together through a single 10-k Ω resistor. Ensure that the trace from the pins to the resistor(s) are as short as possible. See Note 2.
GXB_RX[0:15]n	GXB_RX_[L,R][0:11]n	Input	High speed negative differential receiver channels.	These pins may be AC-coupled or DC-coupled when used. (Note 4) Connect all unused GXB_RXn pins either individually to GND through a 10-k Ω resistor or tie all unused pins together through a single 10-k Ω resistor. Ensure that the trace from the pins to the resistor(s) are as short as possible. See Note 2.
GXB_TX[0:15]p	GXB_TX_[L,R][0:11]p	Output	High speed positive differential transmitter channels.	Leave all unused GXB_TXp pins floating. See Note 2.
GXB_TX[0:15]n	GXB_TX_[L,R][0:11]n	Output	High speed negative differential transmitter channels.	Leave all unused GXB_TXn pins floating. See Note 2.
REFCLK[0:7]p	REFCLK_[L,R][0:5]p, GXB_CMURX_[L,R][0:5]p	Input	High speed differential reference clock positive.	These pins should be AC-coupled when used (see Note 5). Connect all unused pins either individually to GND through a 10-k Ω resistor or tie all unused pins together through a single 10-k Ω resistor. Ensure that the trace from the pins to the resistor(s) are as short as possible.
REFCLK[0:7]n	REFCLK_[L,R][0:5]n, GXB_CMURX_[L,R][0:5]n	Input	High speed differential reference clock complement.	These pins should be AC-coupled when used (see Note 5). Connect all unused pins either individually to GND through a 10-k Ω resistor or tie all unused pins together through a single 10-k Ω resistor. Ensure that the trace from the pins to the resistor(s) are as short as possible.

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Arria II GX Pin Name	Arria II GZ Pin Name	Pin Type (1st and 2nd Function)	Pin Description	Connection Guidelines
RREF[0:1]	RREF_[L,R][0:1]	Input	Reference resistor for transceiver.	If any REFCLK pin or transceiver channel on one side (left or right) of the device is used, you must connect each RREF pin on that side of the device to its own individual 2.00-kΩ +/- 1% resistor to GND. Otherwise, you may connect each RREF pin on that side of the device directly to GND. In the PCB layout, the trace from this pin to the resistor needs to be routed so that it avoids any aggressor signals.

Altera provides these guidelines only as recommendations. It is the responsibility of the designer to apply simulation results to the design to verify proper device functionality.

Notes:

- 1) This pin connection guideline is created based on the Arria II GX and Arria II GZ devices. Shaded cells indicate pin name differences between the Arria II GX and Arria II GZ.
- 2) Transceiver signals GXB_RX[0:15] and GXB_TX[0:15] are device specific.
- 3) Capacitance values for the power supply should be selected after consideration of the amount of power they need to supply over the frequency of operation of the particular circuit being decoupled. A target impedance for the power plane should be calculated based on current draw and voltage droop requirements of the device/supply. The power plane should then be decoupled using the appropriate number of capacitors. On-board capacitors do not decouple higher than 100 MHz due to "Equivalent Series Inductance" of the mounting of the packages. Proper board design techniques such as interplane capacitance with low inductance should be considered for higher frequency decoupling. To assist in decoupling analysis Altera's Power Distribution Network (PDN) design tool serves as an excellent decoupling analysis tool.

[Power Distribution Network Design Tool](#)

- 4) For AC-coupled links, the AC-coupling capacitor can be placed anywhere along the channel. PCI Express protocol requires the AC-coupling capacitor to be placed on the transmitter side of the interface that permits adapters to be plugged and unplugged.
- 5) In PCI Express configuration, DC-coupling is allowed on REFCLK if the selected REFCLK I/O standard is HCSL (High-Speed Current Steering Logic).
- 6) Use the Arria II GX or Arria II GZ Early Power Estimator to determine the current requirements for VCC and other power supplies.
- 7) These supplies may share power planes across multiple Arria II GX or Arria II GZ devices.
- 8) Refer to Example 1 and Figure 1 on the "Power Regs" tab below for the minimum power supply regulator recommendations.
- 9) PLL[1,3]_CLKOUT[2:3]p/n are only available in PLL1 and PLL3 in EP2AGX95, EP2AGX125, EP2AGX190, and EP2AGX260.
- 10) Some of the pull-up /pull-down resistors mentioned in the table above may not be required, depending on the exact device configuration scheme. The ability to NC or short them may be valuable during the debug phase, should you be required to use a different configuration scheme. Refer to the Configuring Arria II GX Devices chapter in the Arria II GX Device Handbook for more information.
- 11) When not used as clocks, the CQn and DQSn pins can be used as DQ pins.
- 12) For Arria II GX some of these pins are assigned to a group of 16 I/O pins. These groups are referred to as I/O modules. Refer to the "I/O module" column in the pin tables to determine which pins are grouped together. The following guideline must be adhered to for each of the I/O modules.
 - a) A maximum of 12 HSTL/SSTL output or bidirectional pins are allowed per I/O module. When assigning 12 HSTL/SSTL output or bidirectional pins in a module the remaining 4 pins must be input only. Differential assignment is not available in this case.
 - b) When 11 or fewer HSTL/SSTL output or bidirectional pins are assigned to an I/O module, then differential HSTL/SSTL output or bidirectional assignments are available for the remaining pins. If any pins remain after this assignment, then upto the first 4 pins must be input only. If there are more than 4 pins, these remaining pins may be input , output or bidirectional.
- 13) The LVDS bank utilization limits the percentage of pins used based on the current setting and I/O standard. For the best jitter performance, adhere to the following guidelines:
 - 100% of the pins in the bank can be used when using 2.5V LVTTTL 4 mA, 50 Ω or 25 Ω, SSTL2.5V CI 8 mA and 12 mA
 - 90% of the pins in the bank can be used when using 2.5V LVTTTL 8 mA
 - 60% of the pins in the bank can be used when using 2.5V LVTTTL 12 mA
 - 50% of the pins in the bank can be used when using 2.5V LVTTTL 16 mA
 - 60% of the pins in the bank can be used when using SSTL2.5V CII 16 mA
 - If the bank contains mixture of 2.5V I/O Standards, the equation to use is

$$\sum_{n=1}^N \left(a \times \frac{1}{b} \right) \leq \frac{c}{100\%}$$

Where n = number of different I/O standards, for example: n = 2 if there are SSTL2.5V CII 16 mA and 2.5V LVTTTL 16 mA in the bank

a = number of aggressors with that particular I/O standard

b = percentage of aggressor that can be toggle for that specific I/O standard, for example: b = 50% for 2.5V LVTTTL 16 mA

c = (total pins in that bank – number of LVDS pins)

14) VCCA_PLL, VCCCB, VCCA and VCCH_GXB may use a switching regulator with a voltage ripple of ±5% maximum.

15) Unused I/O pins need to be tied high, tristated or tied low to match your Quartus II design.

16) All dedicated configuration pins reside in banks 3C and 8C. However, dual function (I/O and config) configuration pins may be located in banks 3A, 6A, or 8A.

17) Altera highly recommends using an independent PCB via for each independent power or ground ball on the package. Sharing power or ground pin vias on the PCB could lead to noise coupling into the device and result in reduced jitter performance.

18) If one or more transceivers are used on a particular side of the device (left [L] or right [R]) all of the transceiver power pins on that side of the device must be connected to its required power supply. However, if no transceivers are used on one side, then all of the transceiver power pins and the GXB_RX pins need to be connected to GND.

19) Low Noise Switching Regulator - defined as a switching regulator circuit encapsulated in a thin surface mount package containing the switch controller, power FETs, inductor, and other support components. The switching frequency is usually between 800kHz and 1MHz and has fast transient response.

Line Regulation < 0.4%

Load Regulation < 1.2%

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Example 1. Arria II GX Power Supply Sharing Guidelines

Example Requiring 5 Power Regulators

Power Pin Name	Regulator Count	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC (See Note 1) VCCD_PLL[1:6]	1	0.9	± 30 mV	Switcher	Share	May be able to share VCCD_PLL with VCC with a proper isolation filter. If not sharing the regulator with VCC the VCCD_PLL supply should not exceed a tolerance of ± 5%.
Isolate						
VCCL_GXB	2	1.1	± 5 %	Linear or Switcher	Share	Depending on the regulator capabilities this supply may be shared with multiple Arria II GX devices. Use the EPE (Early Power Estimation) tool within Quartus II to assist in determining the power required for your specific design.
VCCH_GXB VCCCB (See Note 1)	3	1.5	± 5 %	Linear or Switcher (*)	Share	May be able to share VCCCB with VCCH_GXB with a proper isolation filter. Depending on the regulator capabilities this supply may be shared with multiple Arria II GX devices. Use the EPE tool to assist in determining the power required for your specific design. If not sharing a regulator the VCCH_GXB supply should not exceed a tolerance of ± 5%.
Isolate						
VCCA VCCA_PLL_[1:6]	4	2.5	± 5 %	Linear or Switcher (*)	Share	May be able to share VCCA_PLL and VCCA with a proper isolation filter. Depending on the regulator capabilities this supply may be shared with multiple Arria II GX devices. Use the EPE tool to assist in determining the power required for your specific design.
Isolate						
VCCIO[3:8][A,B], VCCIO[3,8]C VCCPD[3:8][A,B], VCCPD[3,8]C	5	Varies	± 5 %	Switcher	Share if 2.5 V, 3.0 V or 3.3 V	If all of these supplies require 2.5 V, 3.0 V or 3.3 V and the regulator selected satisfies the power specifications then these supplies may all be tied in common. Use the EPE tool to assist in determining the power required for your specific design.
2.5, 3.0, or 3.3						

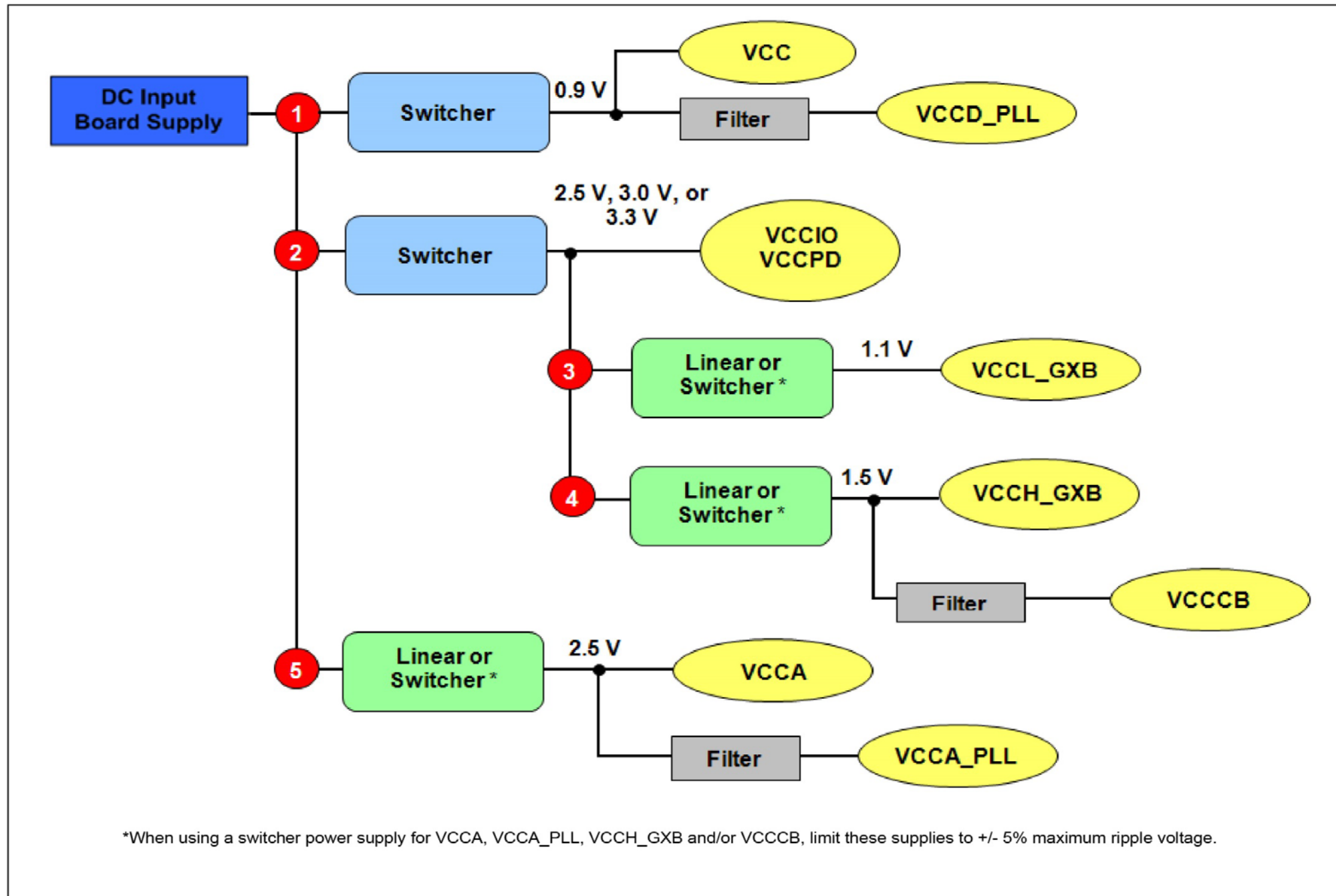
Note:

1) To support the startup current as reported by the Early Power Estimator (EPE) for Arria II GX devices, fully power VCC before VCCCB begins to ramp.

* When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in note 19 in the Pin Connection Guidelines sheet.

Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram is provided in Figure 1.

Figure 1. Example Arria II GX Power Supplies Block Diagram



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Example 2. Arria II GZ Power Supply Sharing Guidelines for Data Rates <= 4.25 Gpbs

Example Requiring 5 Power Regulators

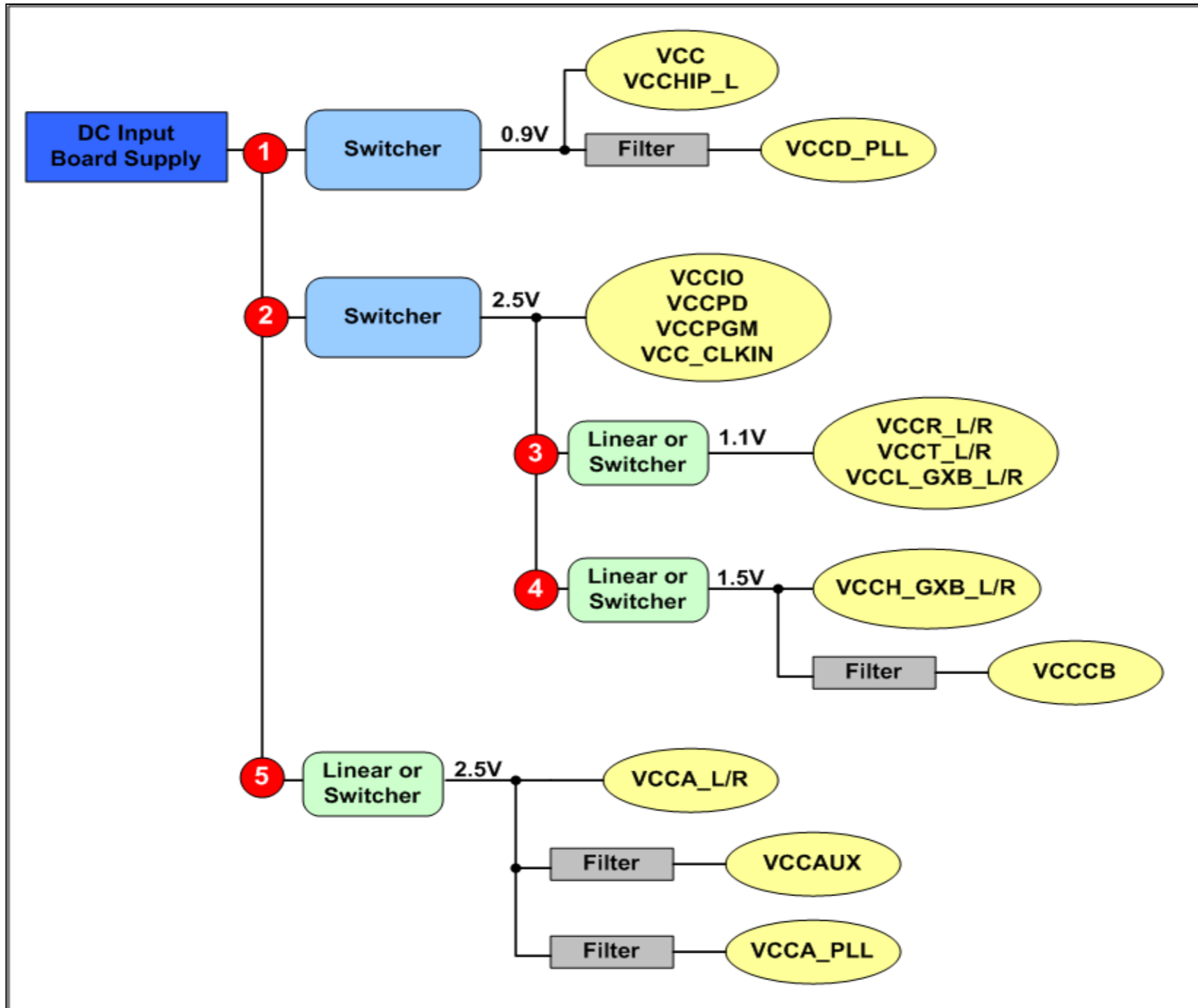
Power Pin Name	Regulator Count	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes
VCC (**) VCCHIP_L	1	0.9	± 30mV	Switcher	Share	VCC and VCCHIP may share regulators. If not using HIP, VCCHIP may be tied to GND.
VCCD_PLL_[L,R][1:4], VCCD_PLL_[T,B][1:2]					Isolate	May be able to share VCCD_PLL with VCC and VCCHIP with a proper isolation filter. If not sharing the regulator with VCC and/or VCCHIP the VCCD_PLL supply should not exceed a tolerance of ± 5%.
VCCIO[1:8][A,C], VCCIO[3,4,7,8]B	2	Varies	± 5%	Switcher	Share if 2.5V	If all of these supplies require 2.5V and the regulator selected satisfies the power specifications then these supplies may all be tied in common. However, for any other voltage you will require a 2.5V regulator for VCC_CLKIN and as many regulators as there are variations of supplies in your specific design. Use the EPE tool to assist in determining the power required for your specific design.
VCCPD[1:8][A,C], VCCPD[3,4,7,8]B						
VCCPGM VCC_CLKIN[3,4,7,8]C						
VCCR_[L,R] VCCT_[L,R]	3	1.1	± 50mV	Linear or Switcher (*)	Share	The left [L] and [R] may share the same regulator. Depending on the regulator capabilities this supply may be shared with multiple Arria II GZ devices. Use the EPE (Early Power Estimation) tool within Quartus II to assist in determining the power required for your specific design.
VCCL_GXB[L,R][0:2] VCCH_GXB[L,R][0:2]						
VCCCB	4	1.5	± 50mV	Linear or Switcher (*)	Share	May be able to share VCCCB with VCCH_GXB with a proper isolation filter. Depending on the regulator capabilities this supply may be shared with multiple Arria II GZ devices. Use the EPE tool to assist in determining the power required for your specific design. If not sharing a regulator the VCCH_GXB supply should not exceed a tolerance of ± 5%.
VCCA_PLL_[L,R][1:4], VCCA_PLL_[T,B][1:2]	5	2.5	± 5%	Linear or Switcher (*)	Isolate/Share	VCCAUX, VCCA_[L,R] and VCCA_PLL may be able to share a regulator with the proper isolation filter. Depending on the regulator capabilities this supply may be shared with multiple Arria II GZ devices. Use the EPE tool to assist in determining the power required for your specific design.
VCCAUX (**)						
VCCA_[L,R]						

* When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in note 19 in the Pin Connection Guidelines sheet.

** To successfully power-up and exit POR, fully power VCC before VCCAUX begins to ramp.

Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Arria II GZ device for data rates less than or equal to 4.25Gbps is provided in Figure 2.

Figure 2. Example Arria II GZ Power Supplies Block Diagram for Data Rates <= 4.25 Gpbs



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Example 3. Arria II GZ Power Supply Sharing Guideline for Data Rates Between 4.25 Gbps and 6.375 Gbps

Example Requiring 5 Power Regulators

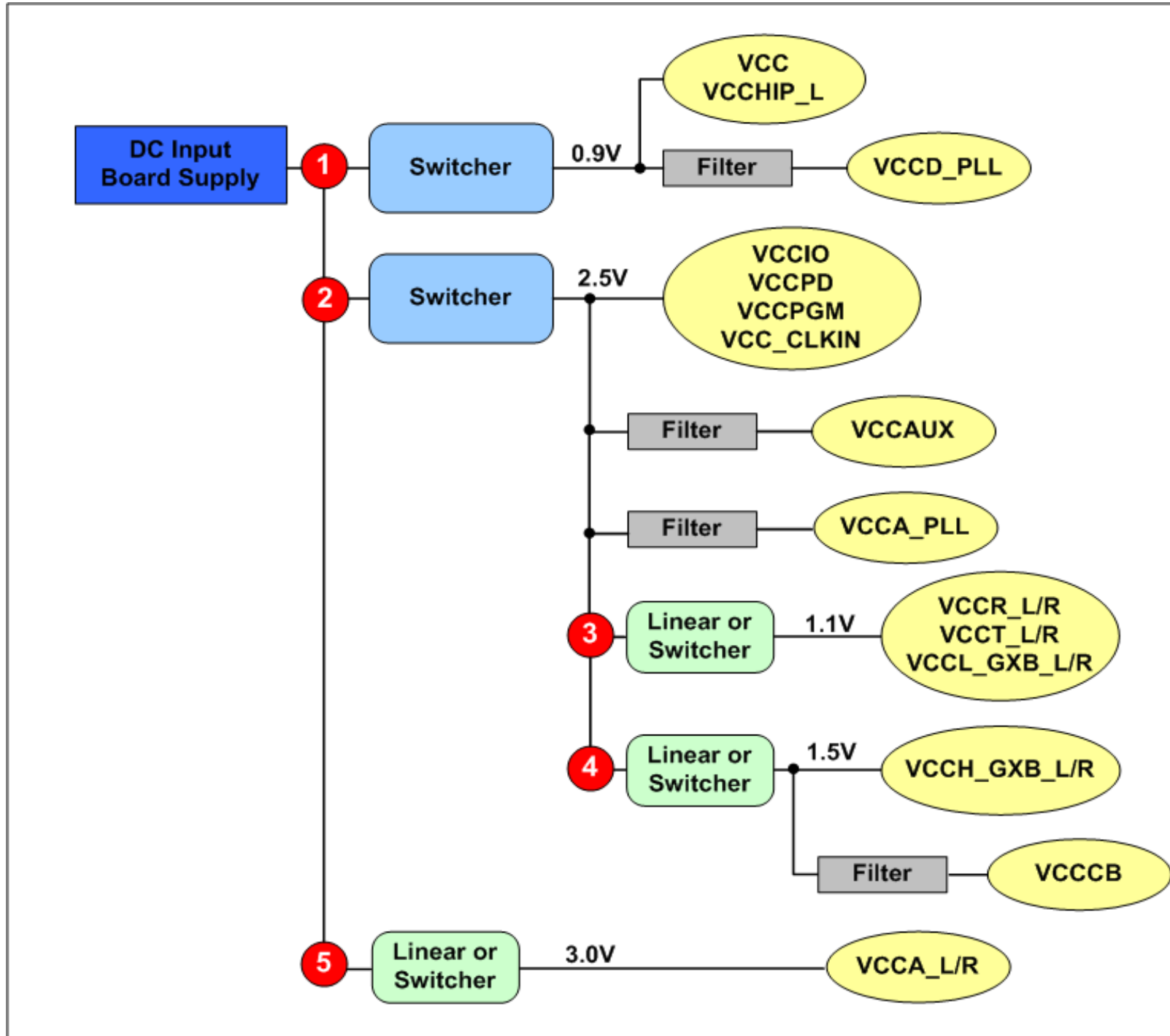
Power Pin Name	Regulator Count	Voltage Level (V)	Supply Tolerance	Power Source	Regulator Sharing	Notes	
VCC (**) VCCHIP_L	1	0.9	± 30mV	Switcher	Share	VCC and VCCHIP may share regulators. If not using HIP, VCCHIP may be tied to GND.	
VCCD_PLL_[L,R][1:4], VCCD_PLL_[T,B][1:2]					Isolate	May be able to share VCCD_PLL with VCC and VCCHIP with a proper isolation filter. If not sharing the regulator with VCC and/or VCCHIP the VCCD_PLL supply should not exceed a tolerance of ± 5%.	
VCCIO[1:8][A,C], VCCIO[3,4,7,8]B	2	Varies	± 5%	Switcher	Share if 2.5V	If all of these supplies require 2.5V and the regulator selected satisfies the power specifications then these supplies may all be tied in common. However, for any other voltage you will require a 2.5V regulator for VCC_CLKIN and as many regulators as there are variations of supplies in your specific design. Use the EPE tool to assist in determining the power required for your specific design.	
VCCPD[1:8][A,C], VCCPD[3,4,7,8]B					Isolate/Share		VCCAUX and VCCA_PLL may be able to share a regulator with the proper isolation filter.
VCCPGM							
VCC_CLKIN[3,4,7,8]C		2.5					
VCCAUX (**) VCCA_PLL_[L,R][1:4], VCCA_PLL_[T,B][1:2]							
VCCR_[L,R] VCCT_[L,R]	3	1.1	± 50mV	Linear or Switcher (*)	Share	The left [L] and [R] may share the same regulator. Depending on the regulator capabilities this supply may be shared with multiple Arria II GZ devices. Use the EPE (Early Power Estimation) tool within Quartus II to assist in determining the power required for your specific design.	
VCCL_GXB[L,R][0:2]							
VCCH_GXB[L,R][0:2]	4	1.5	± 50mV	Linear or Switcher (*)	Share	May be able to share VCCCB with VCCH_GXB with a proper isolation filter. Depending on the regulator capabilities this supply may be shared with multiple Arria II GZ devices. Use the EPE tool to assist in determining the power required for your specific design. If not sharing a regulator the VCCH_GXB supply should not exceed a tolerance of ± 5%.	
VCCCB							
VCCA_[L,R]	5	3.0	± 5%	Linear or Switcher (*)	Share	Depending on the regulator capabilities this supply may be shared with multiple Arria II GZ devices. Use the EPE tool to assist in determining the power required for your specific design.	

* When using a switcher to supply these voltages the switcher must be a low noise switcher as defined in note 19 in the Pin Connection Guidelines sheet.

** To successfully power-up and exit POR, fully power VCC before VCCAUX begins to ramp.

Each board design requires its own power analysis to determine the required power regulators needed to satisfy the specific board design requirements. An example block diagram using the Arria II GZ device for data rates between 4.25 Gbps and 6.375 Gbps is provided in Figure 3.

Figure 3. Example Arria II GZ Power Supplies Block Diagram for data rates between 4.25 Gbps and 6.375 Gbps



**Arria® II Device Family Pin Connection Guidelines
PCG-01007-1.8**

Revision History

Revision	Description of Changes	Date
1.0	Initial Release.	2/8/2009
1.1	Added DNU pins and updated NC guidelines, added note 17, updated Power Regs diagram, updated note references.	5/18/2009
1.2	Removed Note 12a, Note 12b becomes Note 12a, added 1.5 V level to VCCPD	11/2/2009
1.3	Updated Note 13	1/29/2010
1.4	Added Arria II GZ device information. Changed the title of the document. Added table and diagram for Arria II GZ device.	11/2/2010
1.5	Added VCCAUX to GZ pin name field, updated Note 9, PLL_[1,3]_CLKOUT[2:3]p/n pin description, updated TMS/TDI/VCC/VCCCB connection guidelines, updated Example 2 and Example 3 VCCR_[L,R]/VCCT_[L,R]/VCCL_GXB[L,R][0:2] supply tolerance. Removed Preliminary.	6/28/2011
1.6	<ul style="list-style-type: none"> • Updated VCCL_GXB with ' To enhance jitter performance, it is recommended to use a separate power supply for the respective transceiver blocks.' • Updated Note 14. with '±5%'. • Updated Note 18. with ' However, if no transceivers are used on one side, then all of the transceiver power pins and the GXB_RX pins need to be connected to GND.' 	4/12/2013
1.7	Updated connection guidelines for VCCCB, VCCA_PLL, VCCA, and VCCH_GXB with '±5%'.	5/10/2013
1.8	Updated Figure 1. Example Arria II GX Power Supplies Block Diagram with '±5%'.	8/6/2013