















Bank Number	VREF	PinName/Function (2), (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152 (4)	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for BDR# (5)	HMC pin assignment for LPODR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		GND					AB27									
		GND					AB28									
		GND					AB30									
		GND					AB31									
		GND					AB32									
		GND					AC30									
		GND					AC33									
		GND					AC34									
		GND					AD11									
		GND					AD32									
		GND					AE30									
		GND					AE33									
		GND					AE34									
		GND					AF31									
		GND					AF32									
		GND					AG29									
		GND					AG33									
		GND					AG34									
		GND					AH31									
		GND					AH32									
		GND					AJ30									
		GND					AJ33									
		GND					AJ34									
		GND					AK31									
		GND					AK32									
		GND					AL33									
		GND					AL34									
		GND					E34									
		GND					F31									
		GND					F32									
		GND					G30									
		GND					G33									
		GND					G34									
		GND					H31									
		GND					H32									
		GND					J30									
		GND					J33									
		GND					J34									
		GND					K31									
		GND					K32									
		GND					L30									
		GND					L33									
		GND					L34									
		GND					M30									
		GND					M31									
		GND					M32									
		GND					N28									
		GND					N29									
		GND					N33									
		GND					N34									
		GND					P27									
		GND					P31									
		GND					P32									
		GND					R28									
		GND					R30									
		GND					R33									
		GND					R34									
		GND					T27									
		GND					T29									
		GND					T31									
		GND					T32									
		GND					U28									
		GND					U33									
		GND					U34									
		GND					V27									
		GND					V31									
		GND					V32									
		GND					W28									
		GND					W30									
		GND					W33									
		GND					W34									
		GND					Y27									
		GND					Y29									
		GND					Y31									
		GND					Y32									
		GND					AA1									
		GND					AA2									
		GND					AB3									
		GND					AB4									
		GND					AC1									
		GND					AC2									
		GND					AC5									
		GND					AD3									
		GND					AD4									
		GND					AE1									
		GND					AE2									
		GND					AE5									
		GND					AF3									
		GND					AF4									
		GND					AG1									
		GND					AG2									
		GND					AG5									
		GND					AH3									
		GND					AH4									
		GND					AJ1									
		GND					AJ2									
		GND					AJ6									
		GND					AK3									
		GND					AK4									
		GND					AL1									
		GND					AL2									
		GND					AL3									
		GND					AN1									
		GND					V3									
		GND					V4									
		GND					V7									
		GND					W1									
		GND					W2									
		GND					W5									
		GND					Y3									
		GND					Y4									
		GND					Y6									
		GND					Y8									
		VCCP					R18									
		VCCP					T21									
		VCCP					V06									
		VCCP					W10									
		VCCP					Y10									
		VCCP					Y12									
		VCCP					Y22									



Bank Number	VREF	PinName/Function (2), (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152 (4)	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for BDR3 (5)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		VCCP					Y24									
		VCCP					Y25									
		VCCA_FPLL					V26									
		VCCA_FPLL					V9									
		VCCA_FPLL					T86									
		VCCPLL_HPS					M9									
		VCCBRAT					M27									
		VCC_AUX					AA24									
		VCC_AUX					Y11									
		VCC_AUX					R24									
		VCC_AUX_SHARED					R12									
		VCCD_FPLL					V26									
		VCCD_FPLL					Y9									
		VCCD_FPLL					P26									
		VCCA_GXBLO					V28									
		VCCA_GXBRO					Y7									
		VCCA_GXBL1					T28									
		VCCD_GXBLO					V28									
		VCCD_GXBRO					Y8									
		VCCD_GXBL1					P28									
		VCCD_GXBLO					V29									
		VCCD_GXBLO					V30									
		VCCD_GXBRO					Y5									
		VCCD_GXBRO					Y5									
		VCCD_GXBL1					P29									
		VCCD_GXBL1					P30									
		VCCR_GXBL					AA30									
		VCCR_GXBL					AA29									
		VCCR_GXBL					R30									
		VCCR_GXBL					R29									
		VCCR_GXBR					AA5									
		VCCR_GXBR					AB6									
		VCCR_GXBR					AB5									
		VCCD_GXBLO					T30									
		VCCD_GXBLO					U29									
		VCCD_GXBLO					U30									
		VCCD_GXBRO					W6									
		VCCD_GXBRO					AA6									
		VCCD_GXBL1					W29									
		VCCD_GXBL1					Y30									
		VCC					AA20									
		VCC					T19									
		VCC					T23									
		VCC					T35									
		VCC					V24									
		VCC					U18									
		VCC					U20									
		VCC					U22									
		VCC					U24									
		VCC					V15									
		VCC					V17									
		VCC					V19									
		VCC					V20									
		VCC					V21									
		VCC					V22									
		VCC					V23									
		VCC					W16									
		VCC					W14									
		VCC					W20									
		VCC					W22									
		VCC					W24									
		VCC					Y13									
		VCC					Y14									
		VCC					Y15									
		VCC					Y16									
		VCC					Y17									
		VCC					Y19									
		VCC					V21									
		VCC					Y23									
		VCC					W18									
		VCC_HPS					T11									
		VCC_HPS					U10									
		VCC_HPS					U12									
		VCC_HPS					U14									
		VCC_HPS					V11									
		VCC_HPS					V12									
		VCC_HPS					V13									
		VCC_HPS					W12									
		VCCD03A					AF27									
		VCCD03A					AF30									
		VCCD03A					AF30									
		VCCD03A					AJ28									
		VCCD03A					AK30									
		VCCD03A					AN29									
		VCCD03B					AF25									
		VCCD03B					AK24									
		VCCD03B					AN24									
		VCCD03C					AK21									
		VCCD03C					AF21									
		VCCD03C					AJ21									
		VCCD03C					AM21									
		VCCD03D					AE18									
		VCCD03D					AH18									
		VCCD03B					AL18									
		VCCD04A					AD5									
		VCCD04A					AE8									
		VCCD04A					AF5									
		VCCD04A					AH5									
		VCCD04A					AK5									
		VCCD04B					AD11									
		VCCD04B					AF10									
		VCCD04B					AJ10									
		VCCD04B					AM9									
		VCCD04C					AE13									
		VCCD04C					AH12									
		VCCD04C					AJ12									
		VCCD04B					AF15									
		VCCD04D					AJ15									
		VCCD04D					AM15									
		VCCD04D					AN17									
		VCCD06A_HPS					B3									
		VCCD06A_HPS					C6									
		VCCD06A_HPS					D3									
		VCCD06A_HPS					D8									
		VCCD06A_HPS					E6									
		VCCD06A_HPS					F3									
		VCCD06A_HPS					H5									
		VCCD06A_HPS					H7									
		VCCD06A_HPS					H9									
		VCCD06B_HPS					L4									



Bank Number	VREF	PinName/Function (2), (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152 (4)	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for BDR# (5)	HMC pin assignment for LPCR#2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		VCCIO6B_HPS					M1									
		VCCIO6B_HPS					N8									
		VCCIO6B_HPS					P3									
		VCCIO6B_HPS					R6									
		VCCIO6B_HPS					U5									
		VCCIO6B_HPS					V2									
		VCCIO7A_HPS					R9									
		VCCIO7A_HPS					D11									
		VCCIO7A_HPS					E13									
		VCCIO7A_HPS					K11									
		VCCIO7B_HPS					B13									
		VCCIO7B_HPS					L13									
		VCCIO7C_HPS					H15									
		VCCIO7D_HPS					E17									
		VCCIO7D_HPS					H18									
		VCCIO7E_HPS					L18									
		VCCIO8A					G27									
		VCCIO8A					C30									
		VCCIO8A					E28									
		VCCIO8A					E32									
		VCCIO8A					G27									
		VCCIO8A					A27									
		VCCIO8B					B24									
		VCCIO8B					F24									
		VCCIO8B					J24									
		VCCIO8C					B22									
		VCCIO8C					D21									
		VCCIO8C					G21									
		VCCIO8C					L21									
		VCCIO8D					B18									
		VCCIO8D					B20									
		VCCIO8E					H20									
		VCCIOD1					AA21									
		VCCIOD1					AA23									
		VCCIOD1					AB28									
		VCCIOD1					AC28									
		VCCIOD4					AB8									
		VCCPD4BCD					AA11									
		VCCPD4BCD					AA14									
		VCCPD4BCD					AA15									
		VCCPD4BCD					AB9									
		VCCPD4AB6_HPS					P9									
		VCCPD4AB6_HPS					R8									
		VCCPD4AB6_HPS					U7									
		VCCPD4AB6_HPS					U8									
		VCCPD7A_HPS					R11									
		VCCPD7B_HPS					R13									
		VCCPD7C_HPS					T15									
		VCCPD7D_HPS					R16									
		VCCPD7E_HPS					P17									
		VCCPD8					P23									
		VCCPD8					P25									
		VCCPD8					R20									
		VCCPD8					R22									
		VCCPD8					H13									
		VCCPSM					AC29									
		VCCPSSTJLK_HPS					H9									
		VCC_HPS					R10									
		VCC_HPS					R14									
		VCC_HPS					T13									
		VCC_HPS					T9									
	VREFB7A/B7C/D7E/0_HPS	VREFB7A/B7C/D7E/0_HPS					P15									
		GND					A19									
		GND					A22									
		GND					A5									
		GND					AA10									
		GND					AA13									
		GND					AA16									
		GND					AA19									
		GND					AA22									
		GND					AA25									
		GND					AB9									
		GND					AB7									
		GND					AC8									
		GND					AD10									
		GND					AD13									
		GND					AD16									
		GND					AD19									
		GND					AD22									
		GND					AD25									
		GND					AD28									
		GND					AD7									
		GND					AG10									
		GND					AG13									
		GND					AG16									
		GND					AG19									
		GND					AG22									
		GND					AG25									
		GND					AG28									
		GND					AG7									
		GND					AK10									
		GND					AK13									
		GND					AK16									
		GND					AK19									
		GND					AK22									
		GND					AK25									
		GND					AK28									
		GND					AK7									
		GND					AN10									
		GND					AN13									
		GND					AN16									
		GND					AN19									
		GND					AN22									
		GND					AN25									
		GND					AN28									
		GND					AN31									
		GND					AN4									
		GND					AN7									
		GND					B11									
		GND					B16									
		GND					B2									
		GND					B25									
		GND					B28									
		GND					B31									
		GND					B33									
		GND					B8									
		GND					C19									
		GND					C22									
		GND					C5									
		GND					D2									



Bank Number	VREF	PinName/Function (2), (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152 (4)	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for DDR3 (5)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		GND					D30									
		GND					E14									
		GND					E25									
		GND					E28									
		GND					E8									
		GND					F19									
		GND					F22									
		GND					F5									
		GND					G11									
		GND					G2									
		GND					H25									
		GND					H28									
		GND					H8									
		GND					J13									
		GND					J19									
		GND					J22									
		GND					J5									
		GND					K16									
		GND					K2									
		GND					L25									
		GND					L28									
		GND					L8									
		GND					M19									
		GND					M22									
		GND					M5									
		GND					N11									
		GND					N15									
		GND					N2									
		GND					N24									
		GND					P13									
		GND					P18									
		GND					P8									
		GND					V18									
		GND					V14									
		GND					V16									
		GND					V8									
		GND					W11									
		GND					W13									
		GND					W15									
		GND					W17									
		GND					W19									
		GND					W21									
		GND					W23									
		GND					W25									
		GND					W8									
		GND					Y18									
		GND					Y20									
		GND					R17									
		GND					R19									
		GND					R21									
		GND					R23									
		GND					R25									
		GND					R5									
		GND					R9									
		GND					T10									
		GND					T12									
		GND					T14									
		GND					T16									
		GND					T2									
		GND					T20									
		GND					T22									
		GND					T24									
		GND					U11									
		GND					U13									
		GND					U17									
		GND					U19									
		GND					U21									
		GND					U23									
		GND					U25									
		GND					U6									
		GND					U9									
		GND					V19									

Notes:  
(1) For more information about pin definitions and pin connection guidelines, refer to the [Arria V Device Family Pin Connection Guidelines](#).  
(2) GNR\_REFCLK pin is not supported in current Quartus II version, but will be supported in future Quartus II release version.  
(3) Pins with \* contains similar name with other pins in the same column. For the selection of the HPS pins, refer to the "HPS Pin Mux Select" columns.  
(4) Pins with ~ are the 10 Gbps transceiver channels. For more information about the 10 Gbps transceiver channels clocking recommendation, refer to the [Transceiver Clocking in Arria V Devices chapter](#).  
(5) RESET pin is only applicable for DDR3 device.



Bank Number	VREF	PinName/Function (2), (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517 (4)	DQS for X0/X3	DQS for X16/X18	DQS for X32/X36	HMC pin assignment for DQS3 (0)	HMC pin assignment for FCODE2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		DNU					A58									
		DREF_TL					B58									
		REFCLK2p					U32									
		REFCLK2n					U31									
		GXB_TX_L17n					C30*									
		GXB_TX_L17p					C37*									
		GXB_RX_L17n					D30*									
		GXB_RX_L17p					D37*									
		GXB_TX_L16p					E36									
		GXB_TX_L16n					E37									
		GXB_RX_L16p					F36									
		GXB_RX_L16n					F37									
		GXB_TX_L15p					G36*									
		GXB_TX_L15n					G37*									
		GXB_RX_L15p					H36*									
		GXB_RX_L15n					H37*									
		GXB_TX_L14p					J36*									
		GXB_TX_L14n					J37*									
		GXB_RX_L14p					K36*									
		GXB_RX_L14n					K37*									
		GXB_TX_L13p					L36									
		GXB_TX_L13n					L37									
		GXB_RX_L13p					M36									
		GXB_RX_L13n					M37									
		GXB_TX_L12p					N36*									
		GXB_TX_L12n					N37*									
		GXB_RX_L12p					P36*									
		GXB_RX_L12n					P37*									
		REFCLK3p					Q32									
		REFCLK3n					Q31									
		REFCLK2p					AA32									
		REFCLK2n					AA31									
		GXB_TX_L11n					R36*									
		GXB_TX_L11p					R37*									
		GXB_RX_L11n					T36*									
		GXB_RX_L11p					T37*									
		GXB_TX_L10n					U36									
		GXB_TX_L10p					U37									
		GXB_RX_L10n					V36									
		GXB_RX_L10p					V37									
		GXB_TX_L9n					W36*									
		GXB_TX_L9p					W37*									
		GXB_RX_L9n					Y36*									
		GXB_RX_L9p					Y37*									
		GXB_TX_L8n					AA36*									
		GXB_TX_L8p					AA37*									
		GXB_RX_L8n					AB36*									
		GXB_RX_L8p					AB37*									
		GXB_TX_L7n					AC36									
		GXB_TX_L7p					AC37									
		GXB_RX_L7n					AD36									
		GXB_RX_L7p					AD37									
		GXB_TX_L6n					AE36*									
		GXB_TX_L6p					AE37*									
		GXB_RX_L6n					AF36*									
		GXB_RX_L6p					AF37*									
		GXB_TX_L5n					AG36*									
		GXB_TX_L5p					AG37*									
		GXB_RX_L5n					AH36*									
		GXB_RX_L5p					AH37*									
		REFCLK4p					AI32									
		REFCLK4n					AI31									
		REFCLK1n					AE32									
		REFCLK1p					AE31									
		GXB_TX_L4n					AG36*									
		GXB_TX_L4p					AG37*									
		GXB_RX_L4n					AH36*									
		GXB_RX_L4p					AH37*									
		GXB_TX_L3n					AI37									
		GXB_TX_L3p					AJ37									
		GXB_RX_L3n					AK36									
		GXB_RX_L3p					AK37									
		GXB_TX_L2n					AL36*									
		GXB_TX_L2p					AL37*									
		GXB_RX_L2n					AM36*									
		GXB_RX_L2p					AM37*									
		GXB_TX_L1n					AN36									
		GXB_TX_L1p					AN37									
		GXB_RX_L1n					AP36									
		GXB_RX_L1p					AP37									
		GXB_TX_L0n					AR36*									
		GXB_TX_L0p					AR37*									
		GXB_RX_L0n					AS36*									
		GXB_RX_L0p					AS37*									
		REFCLK5p					AT32									
		REFCLK5n					AT31									
		GXB_TX_L0n					AW36*									
		GXB_TX_L0p					AW37*									
		GXB_RX_L0n					AX36*									
		GXB_RX_L0p					AX37*									
		DNU					AG32									
3A		TDO		TDO			AK31									
3A		TMS		TMS			AT34									
3A		TCX		TCX			AM35									
3A		TDI		TDI			AK34									
3A		DNCLK		DNCLK			AW34									
3A		AS_DATA0		DATA0			AK34									
3A		AS_DATA3		DATA3			AK34									
3A		AS_DATA2		DATA2			AK33									
3A		AS_DATA1		DATA1			AK33									
3A		AS_DATAASD0		DATA0			AV33									
3A	VREFBAND	IO	RZQ_0				AK33									
3A	VREFBAND	IO	CLK0n				AK33	DO1B								
3A	VREFBAND	IO	CLK0p				AK34	DO1B								
3A	VREFBAND	IO	CLK0n				AK36	DO1B								
3A	VREFBAND	IO	CLK0p				AK37	DO1B								
3A	VREFBAND	IO	CLK1n				AK36	DO1B								
3A	VREFBAND	IO	CLK1p				AK37	DO1B								
3A	VREFBAND	IO	FRLL_B0_CLKOUT1/FRLL_B0_CLKOUT0/FRLL_B0_FRB				AK34	DO1B								
3A	VREFBAND	IO	FRLL_B1_CLKOUT1/FRLL_B1_CLKOUT0/FRLL_B1_FRB				AK34	DO1B								
3A	VREFBAND	IO	FRLL_B2_CLKOUT1/FRLL_B2_FRB				AK33	DO1B								
3A	VREFBAND	IO	FRLL_B3_CLKOUT1/FRLL_B3_FRB				AK33	DO1B								
3A	VREFBAND	IO	VREFBAND				AK31									
3A	VREFBAND	IO	CLK2n				AK33	DO1B								
3A	VREFBAND	IO	CLK2p				AK33	DO1B								

Bank Number	VREF	PinName/Function (2), (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517 (4)	QDS for X0/0	QDS for X16/18	QDS for X32/36	HMC pin assignment for DQES (6)	HMC pin assignment for FPDS (7)	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
1A	VREFBAND	I0			DIFFIO_TX_B16n	DIFFOUT_B16n	AU31	DO38			A_3A_11					
1A	VREFBAND	I0			DIFFIO_TX_B18n	DIFFOUT_B18n	AU31	DO38			A_3A_10					
1A	VREFBAND	I0			DIFFIO_TX_B17n	DIFFOUT_B17n	AV31	DO38			A_3A_7					
1A	VREFBAND	I0			DIFFIO_TX_B19n	DIFFOUT_B19n	AV31	DO38			A_3A_8	CA_3A_8				
1A	VREFBAND	I0			DIFFIO_TX_B16n	DIFFOUT_B16n	AV30	DO38			A_3A_7	CA_3A_7				
1A	VREFBAND	I0			DIFFIO_TX_B18n	DIFFOUT_B18n	AV30	DO38			A_3A_6	CA_3A_6				
1A	VREFBAND	I0			DIFFIO_TX_B17n	DIFFOUT_B17n	AV30	DO38			A_3A_5	CA_3A_5				
1A	VREFBAND	I0			DIFFIO_TX_B19n	DIFFOUT_B19n	AV30	DO38			A_3A_4	CA_3A_4				
1A	VREFBAND	I0			DIFFIO_TX_B20n	DIFFOUT_B20n	AU30				A_3A_3	CA_3A_3				
1A	VREFBAND	I0			DIFFIO_TX_B20n	DIFFOUT_B20n	AV30	DO38			A_3A_2	CA_3A_2				
1A	VREFBAND	I0			DIFFIO_TX_B21n	DIFFOUT_B21n	AU29	DO38			A_3A_1	CA_3A_1				
1A	VREFBAND	I0			DIFFIO_RX_B21n	DIFFOUT_B21n	AU29	DO38			A_3A_0	CA_3A_0				
1A	VREFBAND	I0			DIFFIO_RX_B21n	DIFFOUT_B21n	AV29	DO38			CA_3A_0					
1A	VREFBAND	I0			DIFFIO_TX_B22n	DIFFOUT_B22n	AV30	DO38			CA_3A_1	CA_3A_1				
1A	VREFBAND	I0			DIFFIO_TX_B22n	DIFFOUT_B22n	AV29	DO38			CA_3A_0	CA_3A_0				
1A	VREFBAND	I0			DIFFIO_RX_B23n	DIFFOUT_B23n	AV29	DO38			CA_3A_0	CA_3A_0				
1A	VREFBAND	I0			DIFFIO_RX_B23n	DIFFOUT_B23n	AV29	DO38			CA_3A_0	CA_3A_0				
1A	VREFBAND	I0			DIFFIO_TX_B24n	DIFFOUT_B24n	AV29	DO38			CA_3A_0	CA_3A_0				
1A	VREFBAND	I0			DIFFIO_TX_B24n	DIFFOUT_B24n	AV29	DO38			CA_3A_0	CA_3A_0				
1B	VREFBAND	I0			DIFFIO_RX_B25n	DIFFOUT_B25n	AV28	DO48	DO28		DO1_38_8	DO1_38_8				
1B	VREFBAND	I0			DIFFIO_RX_B25n	DIFFOUT_B25n	AV28	DO48	DO28		DO1_38_7	DO1_38_7				
1B	VREFBAND	I0			DIFFIO_RX_B25n	DIFFOUT_B25n	AV28	DO48	DO28		DO1_38_6	DO1_38_6				
1B	VREFBAND	I0			DIFFIO_RX_B25n	DIFFOUT_B25n	AV28	DO48	DO28		DO1_38_5	DO1_38_5				
1B	VREFBAND	I0			DIFFIO_RX_B27n	DIFFOUT_B27n	AV28	DO48	DO28		DO1_38_4	DO1_38_4				
1B	VREFBAND	I0			DIFFIO_RX_B27n	DIFFOUT_B27n	AV27	DO48	DO28		DO1_38_3	DO1_38_3				
1B	VREFBAND	I0			DIFFIO_RX_B27n	DIFFOUT_B27n	AV27	DO48	DO28		DO1_38_2	DO1_38_2				
1B	VREFBAND	I0			DIFFIO_RX_B29n	DIFFOUT_B29n	AV27	DO48	DO28		DO1_38_1	DO1_38_1				
1B	VREFBAND	I0			DIFFIO_RX_B29n	DIFFOUT_B29n	AV27	DO48	DO28		DO1_38_0	DO1_38_0				
1B	VREFBAND	I0			DIFFIO_RX_B30n	DIFFOUT_B30n	AV27	DO48	DO28		DO2_38_8	DO2_38_8				
1B	VREFBAND	I0			DIFFIO_RX_B30n	DIFFOUT_B30n	AV27	DO48	DO28		DO2_38_7	DO2_38_7				
1B	VREFBAND	I0			DIFFIO_TX_B31n	DIFFOUT_B31n	AV28	DO48	DO28		DO2_38_6	DO2_38_6				
1B	VREFBAND	I0			DIFFIO_TX_B31n	DIFFOUT_B31n	AV28	DO48	DO28		DO2_38_5	DO2_38_5				
1B	VREFBAND	I0			DIFFIO_TX_B32n	DIFFOUT_B32n	AV28	DO48	DO28		DO2_38_4	DO2_38_4				
1B	VREFBAND	I0			DIFFIO_TX_B32n	DIFFOUT_B32n	AV27	DO48	DO28		DO2_38_3	DO2_38_3				
1B	VREFBAND	I0			DIFFIO_RX_B33n	DIFFOUT_B33n	AV27	DO48	DO28		DO2_38_2	DO2_38_2				
1B	VREFBAND	I0			DIFFIO_RX_B33n	DIFFOUT_B33n	AV27	DO48	DO28		DO2_38_1	DO2_38_1				
1B	VREFBAND	I0			DIFFIO_RX_B33n	DIFFOUT_B33n	AV27	DO48	DO28		DO2_38_0	DO2_38_0				
1B	VREFBAND	I0			DIFFIO_TX_B34n	DIFFOUT_B34n	AV27	DO48	DO28		DO3_38_8	DO3_38_8				
1B	VREFBAND	I0			DIFFIO_TX_B34n	DIFFOUT_B34n	AV27	DO48	DO28		DO3_38_7	DO3_38_7				
1B	VREFBAND	I0			DIFFIO_TX_B35n	DIFFOUT_B35n	AV27	DO48	DO28		DO3_38_6	DO3_38_6				
1B	VREFBAND	I0			DIFFIO_TX_B35n	DIFFOUT_B35n	AV27	DO48	DO28		DO3_38_5	DO3_38_5				
1B	VREFBAND	I0			DIFFIO_RX_B36n	DIFFOUT_B36n	AV27	DO48	DO28		DO3_38_4	DO3_38_4				
1B	VREFBAND	I0			DIFFIO_RX_B36n	DIFFOUT_B36n	AV27	DO48	DO28		DO3_38_3	DO3_38_3				
1B	VREFBAND	I0			DIFFIO_TX_B37n	DIFFOUT_B37n	AV27	DO48	DO28		DO3_38_2	DO3_38_2				
1B	VREFBAND	I0			DIFFIO_TX_B37n	DIFFOUT_B37n	AV27	DO48	DO28		DO3_38_1	DO3_38_1				
1B	VREFBAND	I0			DIFFIO_RX_B38n	DIFFOUT_B38n	AV27	DO48	DO28		DO3_38_0	DO3_38_0				
1B	VREFBAND	I0			DIFFIO_RX_B38n	DIFFOUT_B38n	AV27	DO48	DO28		DO3_38_0	DO3_38_0				
1C	VREFBAND	I0			DIFFIO_TX_B39n	DIFFOUT_B39n	AV27	DO48	DO28		DO4_38_8	DO4_38_8				
1C	VREFBAND	I0			DIFFIO_TX_B39n	DIFFOUT_B39n	AV27	DO48	DO28		DO4_38_7	DO4_38_7				
1C	VREFBAND	I0			DIFFIO_RX_B40n	DIFFOUT_B40n	AV27	DO48	DO28		DO4_38_6	DO4_38_6				
1C	VREFBAND	I0			DIFFIO_RX_B40n	DIFFOUT_B40n	AV27	DO48	DO28		DO4_38_5	DO4_38_5				
1C	VREFBAND	I0			DIFFIO_TX_B41n	DIFFOUT_B41n	AV27	DO48	DO28		DO4_38_4	DO4_38_4				
1C	VREFBAND	I0			DIFFIO_TX_B41n	DIFFOUT_B41n	AV27	DO48	DO28		DO4_38_3	DO4_38_3				
1C	VREFBAND	I0			DIFFIO_TX_B42n	DIFFOUT_B42n	AV27	DO48	DO28		DO4_38_2	DO4_38_2				
1C	VREFBAND	I0			DIFFIO_TX_B42n	DIFFOUT_B42n	AV27	DO48	DO28		DO4_38_1	DO4_38_1				
1C	VREFBAND	I0			DIFFIO_RX_B43n	DIFFOUT_B43n	AV28	DO48	DO28		DO4_38_0	DO4_38_0				
1C	VREFBAND	I0			DIFFIO_RX_B43n	DIFFOUT_B43n	AV28	DO48	DO28		DO4_38_0	DO4_38_0				
1C	VREFBAND	I0			DIFFIO_RX_B44n	DIFFOUT_B44n	AV28	DO48	DO28		DO5_38_8	DO5_38_8				
1C	VREFBAND	I0			DIFFIO_RX_B44n	DIFFOUT_B44n	AV28	DO48	DO28		DO5_38_7	DO5_38_7				
1C	VREFBAND	I0			DIFFIO_TX_B45n	DIFFOUT_B45n	AV28	DO48	DO28		DO5_38_6	DO5_38_6				
1C	VREFBAND	I0			DIFFIO_TX_B45n	DIFFOUT_B45n	AV28	DO48	DO28		DO5_38_5	DO5_38_5				
1C	VREFBAND	I0			DIFFIO_RX_B46n	DIFFOUT_B46n	AV28	DO48	DO28		DO5_38_4	DO5_38_4				
1C	VREFBAND	I0			DIFFIO_RX_B46n	DIFFOUT_B46n	AV28	DO48	DO28		DO5_38_3	DO5_38_3				
1C	VREFBAND	I0			DIFFIO_TX_B47n	DIFFOUT_B47n	AV28	DO48	DO28		DO5_38_2	DO5_38_2				
1C	VREFBAND	I0			DIFFIO_TX_B47n	DIFFOUT_B47n	AV28	DO48	DO28		DO5_38_1	DO5_38_1				
1C	VREFBAND	I0			DIFFIO_RX_B48n	DIFFOUT_B48n	AV28	DO48	DO28		DO5_38_0	DO5_38_0				
1C	VREFBAND	I0			DIFFIO_RX_B48n	DIFFOUT_B48n	AV28	DO48	DO28		DO5_38_0	DO5_38_0				
1C	VREFBAND	I0			DIFFIO_TX_B49n	DIFFOUT_B49n	AV28	DO48	DO28		DO6_38_8	DO6_38_8				
1C	VREFBAND	I0			DIFFIO_TX_B49n	DIFFOUT_B49n	AV28	DO48	DO28		DO6_38_7	DO6_38_7				
1C	VREFBAND	I0			DIFFIO_RX_B50n	DIFFOUT_B50n	AV28	DO48	DO28		DO6_38_6	DO6_38_6				
1C	VREFBAND	I0			DIFFIO_RX_B50n	DIFFOUT_B50n	AV28	DO48	DO28		DO6_38_5	DO6_38_5				
1C	VREFBAND	I0			DIFFIO_TX_B51n	DIFFOUT_B51n	AV28	DO48	DO28		DO6_38_4	DO6_38_4				
1C	VREFBAND	I0			DIFFIO_TX_B51n	DIFFOUT_B51n	AV28	DO48	DO28		DO6_38_3	DO6_38_3				
1C	VREFBAND	I0			DIFFIO_RX_B52n	DIFFOUT_B52n	AV28	DO48	DO28		DO6_38_2	DO6_38_2				
1C	VREFBAND	I0			DIFFIO_RX_B52n	DIFFOUT_B52n	AV28	DO48	DO28		DO6_38_1	DO6_38_1				
1C	VREFBAND	I0			DIFFIO_TX_B53n	DIFFOUT_B53n	AV28	DO48	DO28		DO6_38_0	DO6_38_0				
1C	VREFBAND	I0			DIFFIO_TX_B53n	DIFFOUT_B53n	AV28	DO48	DO28		DO6_38_0	DO6_38_0				
1C	VREFBAND	I0			DIFFIO_RX_B54n	DIFFOUT_B54n	AV28	DO48	DO28		DO7_38_8	DO7_38_8				
1C	VREFBAND	I0			DIFFIO_RX_B54n	DIFFOUT_B54n	AV28	DO48	DO28		DO7_38_7	DO7_38_7				
1C	VREFBAND	I0			DIFFIO_TX_B55n	DIFFOUT_B55n	AV28	DO48	DO28		DO7_38_6	DO7_38_6				
1C	VREFBAND	I0			DIFFIO_TX_B55n	DIFFOUT_B55n	AV28	DO48	DO28		DO7_38_5	DO7_38_5				
1C	VREFBAND	I0			DIFFIO_RX_B56n	DIFFOUT_B56n	AV28	DO48	DO28		DO7_38_4	DO7_38_4				
1C	VREFBAND	I0			DIFFIO_RX_B56n	DIFFOUT_B56n	AV28	DO48	DO28		DO7_38_3	DO7_38_3				
1C	VREFBAND	I0			DIFFIO_TX_B57n	DIFFOUT_B57n	AV28	DO48	DO28		DO7_38_2	DO7_38_2				
1C	V															



Bank Number	VREF	PinName/Function (2), (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517 (4)	DQS for X0/X0	DQS for X16/X18	DQS for X32/X36	HMC pin assignment for DQS0 (5)	HMC pin assignment for FPDQS (6)	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0	
3D	VREFB3D0	I0	CLK6n		DIFFIO_RX_B79n	DIFFOUT_B79n	AE21	DQ11B	DQ5B	DQ25B							
3D	VREFB3D0	I0	CLK6n		DIFFIO_TX_B79n	DIFFOUT_B79n	AE21	DQ11B	DQ5B	DQ25B							
3D	VREFB3D0	I0	FPLL_BC_CLKOUT0>FPLL_BC_CLKOUT1>FPLL_BC_CLKOUT2		DIFFIO_TX_B79p	DIFFOUT_B79p	AE22	DQ11B	DQ5B	DQ25B							
3D	VREFB3D0	I0	FPLL_BC_CLKOUT3>FPLL_BC_CLKOUT4>FPLL_BC_CLKOUT5>FPLL_BC_CLKOUT6>FPLL_BC_CLKOUT7>FPLL_BC_CLKOUT8>FPLL_BC_CLKOUT9		DIFFIO_RX_B80n	DIFFOUT_B80n	AE21	DQS014BQK14B	DQS0B	DQS50B							
3D	VREFB3D0	I0	FPLL_BC_CLKOUT1>FPLL_BC_CLKOUT2>FPLL_BC_CLKOUT3>FPLL_BC_CLKOUT4>FPLL_BC_CLKOUT5>FPLL_BC_CLKOUT6>FPLL_BC_CLKOUT7>FPLL_BC_CLKOUT8>FPLL_BC_CLKOUT9		DIFFIO_RX_B80p	DIFFOUT_B80p	AE21	DQS014BQK14BQK14B	DQS0B	DQS50B							
3D	VREFB3D0	I0			DIFFIO_TX_B81n	DIFFOUT_B81n	AE20	DQ11B	DQ5B	DQ25B							
3D	VREFB3D0	I0			DIFFIO_TX_B81p	DIFFOUT_B81p	AE20	DQ11B	DQ5B	DQ25B							
3D	VREFB3D0	I0	CLK6n		DIFFIO_RX_B82n	DIFFOUT_B82n	AE21	DQ11B	DQ5B	DQ25B							
3D	VREFB3D0	I0	CLK6p		DIFFIO_RX_B82p	DIFFOUT_B82p	AE20	DQ11B	DQ5B	DQ25B							
3D	VREFB3D0	I0			DIFFIO_TX_B83n	DIFFOUT_B83n	AE20	DQ11B	DQ5B	DQ25B							
3D	VREFB3D0	I0			DIFFIO_TX_B83p	DIFFOUT_B83p	AE20	DQ11B	DQ5B	DQ25B							
3D	VREFB3D0	I0	CLK6n		DIFFIO_TX_B84n	DIFFOUT_B84n	AE20	DQ11B	DQ5B	DQ25B							
3D	VREFB3D0	I0	CLK6p		DIFFIO_RX_B84p	DIFFOUT_B84p	AE20	DQ11B	DQ5B	DQ25B							
3D	VREFB3D0	I0	LVCC0 FPLL		DIFFIO_RX_B84n	DIFFOUT_B84n	AE20	DQ11B	DQ5B	DQ25B							
3D	VREFB3D0	I0	VCC0 FPLL				AE20										
4D	VREFB4D0	I0			DIFFIO_TX_B85n	DIFFOUT_B85n	AE18	DQ12B									
4D	VREFB4D0	I0			DIFFIO_RX_B85n	DIFFOUT_B85n	AE18	DQ12B									
4D	VREFB4D0	I0			DIFFIO_TX_B86n	DIFFOUT_B86n	AE18	DQ12B									
4D	VREFB4D0	I0			DIFFIO_RX_B86n	DIFFOUT_B86n	AE18	DQ12B									
4D	VREFB4D0	I0			DIFFIO_TX_B87n	DIFFOUT_B87n	AE19	DQ12B									
4D	VREFB4D0	I0			DIFFIO_RX_B87n	DIFFOUT_B87n	AE19	DQ12B									
4D	VREFB4D0	I0			DIFFIO_TX_B88n	DIFFOUT_B88n	AE19	DQS012BQK12B									
4D	VREFB4D0	I0			DIFFIO_RX_B88n	DIFFOUT_B88n	AE19	DQS012BQK12BQK12B									
4D	VREFB4D0	I0			DIFFIO_TX_B89n	DIFFOUT_B89n	AE18	DQ12B									
4D	VREFB4D0	I0			DIFFIO_RX_B89n	DIFFOUT_B89n	AE18	DQ12B									
4D	VREFB4D0	I0			DIFFIO_RX_B90n	DIFFOUT_B90n	AE19	DQ12B									
4D	VREFB4D0	I0			DIFFIO_TX_B91n	DIFFOUT_B91n	AE19	DQ12B									
4D	VREFB4D0	I0			DIFFIO_TX_B91p	DIFFOUT_B91p	AE19	DQ12B									
4D	VREFB4D0	I0			DIFFIO_RX_B92n	DIFFOUT_B92n	AE17	DQ12B									
4D	VREFB4D0	I0			DIFFIO_RX_B92p	DIFFOUT_B92p	AE16	DQ12B									
4D	VREFB4D0	I0			DIFFIO_TX_B93n	DIFFOUT_B93n	AK17	DQ13B	DQ6B				CSE_4D_1	CSE_4D_1			
4D	VREFB4D0	I0			DIFFIO_RX_B94n	DIFFOUT_B94n	AT17	DQ13B	DQ6B				CSE_4D_0	CSE_4D_0			
4D	VREFB4D0	I0			DIFFIO_RX_B94p	DIFFOUT_B94p	AU17	DQ13B	DQ6B				A_4D_15				
4D	VREFB4D0	I0			DIFFIO_TX_B95n	DIFFOUT_B95n	AE19	DQ13B					ODT_4D_1	ODT_4D_1			
4D	VREFB4D0	I0			DIFFIO_RX_B95n	DIFFOUT_B95n	AE19	DQ13B	DQ6B				ODT_4D_0	ODT_4D_0			
4D	VREFB4D0	I0			DIFFIO_RX_B96n	DIFFOUT_B96n	AP18	DQS013BQK13B	DQ5B				WEF_4D				
4D	VREFB4D0	I0			DIFFIO_RX_B96p	DIFFOUT_B96p	AP18	DQS013BQK13BQK13B	DQ5B				CSE_4D				
4D	VREFB4D0	I0			DIFFIO_TX_B97n	DIFFOUT_B97n	AD17	DQ13B					FASE_4D				
4D	VREFB4D0	I0			DIFFIO_TX_B97p	DIFFOUT_B97p	AE18	DQ13B	DQ6B				BA_4D_2				
4D	VREFB4D0	I0			DIFFIO_RX_B98n	DIFFOUT_B98n	AE18	DQ13B	DQ6B				BA_4D_1				
4D	VREFB4D0	I0			DIFFIO_RX_B98p	DIFFOUT_B98p	AE18	DQ13B	DQ6B				BA_4D_0				
4D	VREFB4D0	I0	VREFB4D0				AE18	DQ13B	DQ6B				A_4D_14				
4D	VREFB4D0	I0			DIFFIO_RX_B99n	DIFFOUT_B99n	AL18	DQ13B	DQ6B				A_4D_13				
4D	VREFB4D0	I0			DIFFIO_RX_B99p	DIFFOUT_B99p	AM18	DQ13B	DQ6B				A_4D_12				
4D	VREFB4D0	I0			DIFFIO_TX_1000n	DIFFOUT_1000n	AM17	DQ14B					A_4D_11				
4D	VREFB4D0	I0			DIFFIO_TX_1000p	DIFFOUT_1000p	AM17	DQ14B					A_4D_10				
4D	VREFB4D0	I0			DIFFIO_RX_1001n	DIFFOUT_1001n	AM17	DQ14B					A_4D_9				
4D	VREFB4D0	I0			DIFFIO_RX_1001p	DIFFOUT_1001p	AM17	DQ14B					A_4D_8				
4D	VREFB4D0	I0			DIFFIO_TX_1002n	DIFFOUT_1002n	DM17	DQ14B	DQ8B				A_4D_7	CA_4D_7			
4D	VREFB4D0	I0			DIFFIO_TX_1002p	DIFFOUT_1002p	AE16	DQ14B	DQ8B				A_4D_6	CA_4D_6			
4D	VREFB4D0	I0			DIFFIO_RX_1003n	DIFFOUT_1003n	AV16	DQS014BQK14B	DQ5B				A_4D_5	CA_4D_5			
4D	VREFB4D0	I0			DIFFIO_RX_1003p	DIFFOUT_1003p	AV16	DQS014BQK14BQK14B	DQS0B				A_4D_4	CA_4D_4			
4D	VREFB4D0	I0			DIFFIO_TX_1004n	DIFFOUT_1004n	AK16	DQ14B	DQ8B				A_4D_3	CA_4D_3			
4D	VREFB4D0	I0			DIFFIO_TX_1004p	DIFFOUT_1004p	AK16	DQ14B	DQ8B				A_4D_2	CA_4D_2			
4D	VREFB4D0	I0			DIFFIO_RX_1005n	DIFFOUT_1005n	AM16	DQ14B	DQ8B				A_4D_1	CA_4D_1			
4D	VREFB4D0	I0			DIFFIO_RX_1005p	DIFFOUT_1005p	AM16	DQ14B	DQ8B				A_4D_0	CA_4D_0			
4D	VREFB4D0	I0			DIFFIO_TX_1006n	DIFFOUT_1006n	AL16	DQ14B					CSE_4D_1	CSE_4D_1			
4D	VREFB4D0	I0			DIFFIO_TX_1006p	DIFFOUT_1006p	AM16	DQ14B	DQ8B				CSE_4D_0	CSE_4D_0			
4D	VREFB4D0	I0			DIFFIO_RX_1007n	DIFFOUT_1007n	AM15	DQ14B	DQ8B				CSE_4D				
4C	VREFB4C0	I0			DIFFIO_TX_1008n	DIFFOUT_1008n	AP15	DQ15B					CK_4D	CK_4D			
4C	VREFB4C0	I0			DIFFIO_TX_1008p	DIFFOUT_1008p	AP15	DQ15B					RES574_4D				
4C	VREFB4C0	I0			DIFFIO_RX_1009n	DIFFOUT_1009n	AV14	DQ15B	DQ7B				DQ1_4C_7	DQ1_4C_7			
4C	VREFB4C0	I0			DIFFIO_RX_1009p	DIFFOUT_1009p	AV14	DQ15B	DQ7B				DQ1_4C_6	DQ1_4C_6			
4C	VREFB4C0	I0			DIFFIO_TX_1100n	DIFFOUT_1100n	AC16	DQ15B					DQ1_4C_5	DQ1_4C_5			
4C	VREFB4C0	I0			DIFFIO_TX_1100p	DIFFOUT_1100p	AD16	DQ15B					DQ1_4C_4	DQ1_4C_4			
4C	VREFB4C0	I0			DIFFIO_RX_1101n	DIFFOUT_1101n	AE16	DQS015BQK15B	DQ7B				DM1_4C	DM1_4C			
4C	VREFB4C0	I0			DIFFIO_RX_1101p	DIFFOUT_1101p	AE16	DQS015BQK15BQK15B	DQ7B				DQS01_4C	DQS01_4C			
4C	VREFB4C0	I0			DIFFIO_TX_1102n	DIFFOUT_1102n	AK15	DQ15B					DO1_4C	DO1_4C			
4C	VREFB4C0	I0			DIFFIO_TX_1102p	DIFFOUT_1102p	AL15	DQ15B					DO1_4C_2	DO1_4C_2			
4C	VREFB4C0	I0			DIFFIO_RX_1103n	DIFFOUT_1103n	AV13	DQ15B					DO1_4C_1	DO1_4C_1			
4C	VREFB4C0	I0			DIFFIO_RX_1103p	DIFFOUT_1103p	AV13	DQ15B					DO1_4C_0	DO1_4C_0			
4C	VREFB4C0	I0			DIFFIO_TX_1104n	DIFFOUT_1104n	AM15	DQ15B					DO1_4C_3	DO1_4C_3			
4C	VREFB4C0	I0			DIFFIO_TX_1104p	DIFFOUT_1104p	AM15	DQ15B					DO1_4C_2	DO1_4C_2			
4C	VREFB4C0	I0			DIFFIO_RX_1114n	DIFFOUT_1114n	AM15	DQ15B					DO1_4C_1	DO1_4C_1			
4C	VREFB4C0	I0			DIFFIO_RX_1114p	DIFFOUT_1114p	AM15	DQ15B					DO1_4C_0	DO1_4C_0			
4C	VREFB4C0	I0			DIFFIO_TX_1115n	DIFFOUT_1115n	AC15	DQ16B	DQ3B				DQ2_4C_6	DQ2_4C_6			
4C	VREFB4C0	I0			DIFFIO_TX_1115p	DIFFOUT_1115p	AD14	DQ16B	DQ3B				DQ2_4C_5	DQ2_4C_5			
4C	VREFB4C0	I0			DIFFIO_RX_1116n	DIFFOUT_1116n	AL14	DQ16B					DQ2_4C_4	DQ2_4C_4			
4C	VREFB4C0	I0			DIFFIO_RX_1116p	DIFFOUT_1116p	AL14	DQ16B					DQ2_4C_3	DQ2_4C_3			
4C	VREFB4C0	I0			DIFFIO_TX_1117n	DIFFOUT_1117n	AT13	DQ16B					DQ2_4C_2	DQ2_4C_2			
4C	VREFB4C0	I0			DIFFIO_TX_1117p	DIFFOUT_1117p	AU13	DQ16B					DQ2_4C_1	DQ2_4C_1			
4C	VREFB4C0	I0			DIFFIO_RX_1118n	DIFFOUT_1118n	AE16	DQS016BQK16B	DQ3B				DM2_4C	DM2_4C			
4C	VREFB4C0	I0			DIFFIO_RX_1118p	DIFFOUT_1118p	AE15	DQS016BQK16BQK16B	DQS0B				DQS02_4C	DQS02_4C			
4C	VREFB4C0	I0			DIFFIO_TX_1119n	DIFFOUT_1119n	AK14	DQ16B					DQ3_4C				
4C	VREFB4C0	I0			DIFFIO_TX_1119p	DIFFOUT_1119p	AK14	DQ16B					DQ3_4C_5	DQ3_4C_5			
4C	VREFB4C0	I0			DIFFIO_RX_1120n	DIFFOUT_1120n	AM14	DQ16B	DQ3B				DQ3_4C_4	DQ3_4C_4			
4C	VREFB4C0	I0			DIFFIO_RX_1120p	DIFFOUT_1120p	AM14	DQ16B	DQ3B				DQ3_4C_3	DQ3_4C_3			
4C	VREFB4C0	I0			DIFFIO_TX_1121n	DIFFOUT_1121n	AE14	DQ16B					DQ3_4C_2	DQ3_4C_2			
4C	VREFB4C0	I0			DIFFIO_TX_1121p	DIFFOUT_1121p	AE14	DQ16B					DQ3_4C_1	DQ3_4C_1			
4C	VREFB4C0	I0			DIFFIO_RX_1122n	DIFFOUT_1122n	AD15	DQ16B					DQ3_4C_0	DQ3_4C_0			
4C	VREFB4C0	I0			DIFFIO_RX_1122p	DIFFOUT_1122p	AE15	DQ16B					DQ3_4C_0	DQ3_4C_0			
4B	VREFB4B0	I0			DIFFIO_TX_1123n	DIFFOUT_1123n	AP13	DQ17B					DO3_4B_7	DO3_4B_7			
4B	VREFB4B0	I0			DIFFIO_RX_1123n	DIFFOUT_1123n	AP13	DQ17B					DO3_4B_6	DO3_4B_6			
4B	VREFB4B0	I0			DIFFIO_TX_1124n	DIFFOUT_1124n	AE13	DQ17B	DQ5B				DO3_4B_5	DO3_4B_5			
4B	VREFB4B0	I0			DIFFIO_RX_1124n	DIFFOUT_1124n	AE13	DQ17B	DQ5B				DO3_4B_4	DO3_4B_4			
4B	VREFB4B0	I0			DIFFIO_TX_1125n	DIFFOUT_1125n	AE12	DQ17B					DO3_4B_3	DO3_4B_3			
4B	VREFB4B0	I0			DIFFIO_RX_1125n	DIFFOUT_											



Bank Number	VREF	PinName/Function (2), (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517 (4)	DQS for X0/X3	DQS for X16/X18	DQS for X32/X36	HMC pin assignment for DQES3 pin	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0	
4B	VREFBAND	IO			DIFFIO_TX_B139b	DIFFOUT_B139b	AD11	DQ10B		DQ10B	DQ5_4B_8	DQ5_4B_8					
4B	VREFBAND	IO			DIFFIO_RX_B139b	DIFFOUT_B139b	AE12	DQ10B		DQ10B	DQ5_4B_7	DQ5_4B_7					
4B	VREFBAND	IO			DIFFIO_TX_B140a	DIFFOUT_B140a	A79	DQ10B		DQ10B	DQ5_4B_6	DQ5_4B_6					
4B	VREFBAND	IO			DIFFIO_RX_B140a	DIFFOUT_B140a	A89	DQ10B		DQ10B	DQ5_4B_5	DQ5_4B_5					
4B	VREFBAND	IO			DIFFIO_RX_B141a	DIFFOUT_B141a	A511	DQ5a19B/Q10B		DQ10B	DQ5a5_4B	DQ5a5_4B					
4B	VREFBAND	IO			DIFFIO_TX_B142a	DIFFOUT_B142a	D112	DQ10B		DQ10B	DQ5_4B_4	DQ5_4B_4					
4B	VREFBAND	IO			DIFFIO_TX_B142b	DIFFOUT_B142b	AE12	DQ10B		DQ10B	DQ5_4B_3	DQ5_4B_3					
4B	VREFBAND	IO			DIFFIO_RX_B143a	DIFFOUT_B143a	AP10	DQ10B		DQ10B	DQ5_4B_2	DQ5_4B_2					
4B	VREFBAND	IO			DIFFIO_TX_B143b	DIFFOUT_B143b	AE10	DQ10B		DQ10B	DQ5_4B_1	DQ5_4B_1					
4B	VREFBAND	IO			DIFFIO_TX_B144a	DIFFOUT_B144a	AK11	DQ10B		DQ10B	DQ5_4B_0	DQ5_4B_0					
4B	VREFBAND	IO			DIFFIO_RX_B144b	DIFFOUT_B144b	AK11	DQ10B		DQ10B							
4B	VREFBAND	IO			DIFFIO_RX_B145a	DIFFOUT_B145a	AM10	DQ10B		DQ10B							
4B	VREFBAND	IO			DIFFIO_RX_B145b	DIFFOUT_B145b	AM10	DQ10B		DQ10B							
4A	VREFBAND	IO			DIFFIO_TX_B146a	DIFFOUT_B146a	AL9	DQ20B		DQ20B							
4A	VREFBAND	IO		DATA10	DIFFIO_TX_B146b	DIFFOUT_B146b	AM9	DQ20B		DQ20B							
4A	VREFBAND	IO		DATA11	DIFFIO_RX_B147a	DIFFOUT_B147a	AV7	DQ20B		DQ20B							
4A	VREFBAND	IO		DATA5	DIFFIO_RX_B147b	DIFFOUT_B147b	AV6	DQ20B		DQ20B							
4A	VREFBAND	IO			DIFFIO_TX_B148a	DIFFOUT_B148a	AV7	DQ20B		DQ20B							
4A	VREFBAND	IO		DATA6	DIFFIO_TX_B148b	DIFFOUT_B148b	AV6	DQ20B		DQ20B							
4A	VREFBAND	IO		DATA12	DIFFIO_RX_B149a	DIFFOUT_B149a	AV6	DQ20B/Q0KB		DQ20B							
4A	VREFBAND	IO		DATA13	DIFFIO_RX_B149b	DIFFOUT_B149b	AV5	DQ20B/Q0KB/Q10B		DQ20B							
4A	VREFBAND	IO		DATA7	DIFFIO_TX_B150a	DIFFOUT_B150a	A99	DQ20B		DQ20B							
4A	VREFBAND	IO		DATA8	DIFFIO_TX_B150b	DIFFOUT_B150b	AE10	DQ20B		DQ20B							
4A	VREFBAND	IO		DATA14	DIFFIO_RX_B151a	DIFFOUT_B151a	AU7	DQ20B		DQ20B							
4A	VREFBAND	IO		DATA15	DIFFIO_RX_B151b	DIFFOUT_B151b	AV8	DQ20B		DQ20B							
4A	VREFBAND	IO		DATA9	DIFFIO_TX_B152a	DIFFOUT_B152a	AP9	DQ20B		DQ20B							
4A	VREFBAND	IO		CLKUSR	DIFFIO_TX_B152b	DIFFOUT_B152b	AP9	DQ20B		DQ20B							
4A	VREFBAND	IO			DIFFIO_RX_B153a	DIFFOUT_B153a	AP9	DQ20B		DQ20B							
4A	VREFBAND	IO			DIFFIO_RX_B153b	DIFFOUT_B153b	AP9	DQ20B		DQ20B							
4A	VREFBAND	IO			PR_ERROR	DIFFIO_TX_B154a	DIFFOUT_B154a	AE10	DQ21B								
4A	VREFBAND	IO			PR_READY	DIFFIO_TX_B154b	DIFFOUT_B154b	AE10	DQ21B								
4A	VREFBAND	IO			PR_DONE	DIFFIO_RX_B155a	DIFFOUT_B155a	AE10	DQ21B								
4A	VREFBAND	IO			PR_REQUEST	DIFFIO_RX_B155b	DIFFOUT_B155b	AE11	DQ21B								
4A	VREFBAND	IO			PERST10	DIFFIO_TX_B156a	DIFFOUT_B156a	AA6	DQ21B								
4A	VREFBAND	IO			PERST10	DIFFIO_TX_B156b	DIFFOUT_B156b	AA6	DQ21B								
4A	VREFBAND	IO			PERST11	DIFFIO_RX_B156c	DIFFOUT_B156c	AA6	DQ21B								
4A	VREFBAND	IO			CAP_COMPDONE	DIFFIO_RX_B157a	DIFFOUT_B157a	AA6	DQ21B/Q0KB								
4A	VREFBAND	IO			CAP_ERROR	DIFFIO_RX_B157b	DIFFOUT_B157b	AA6	DQ21B/Q0KB/Q10B								
4A	VREFBAND	IO			DEV_OK	DIFFIO_TX_B158a	DIFFOUT_B158a	AA9	DQ21B								
4A	VREFBAND	IO			DEV_CLK#	DIFFIO_TX_B158b	DIFFOUT_B158b	AA9	DQ21B								
4A	VREFBAND	IO			INT_DONE	DIFFIO_RX_B159a	DIFFOUT_B159a	AA6	DQ21B								
4A	VREFBAND	IO			CEO	DIFFIO_RX_B159b	DIFFOUT_B159b	AA6	DQ21B								
4A	VREFBAND	IO		VREFBAND			AA7	DQ21B		DQ21B							
4A	VREFBAND	IO			CLK11n	DIFFIO_RX_B160a	DIFFOUT_B160a	AJ7	DQ21B								
4A	VREFBAND	IO			CLK12p	DIFFIO_RX_B160b	DIFFOUT_B160b	AJ7	DQ21B								
4A	VREFBAND	IO			PPL_BR_CLKOUT1/PPL_BR_CLKOUT1	DIFFIO_TX_B161a	DIFFOUT_B161a	AJ7	DQ21B								
4A	VREFBAND	IO			PPL_BR_CLKOUT1/PPL_BR_CLKOUT1/PPL_BR_FB0	DIFFIO_TX_B161b	DIFFOUT_B161b	AM7	DQ22B								
4A	VREFBAND	IO			PPL_BR_CLKOUT1/PPL_BR_FB0	DIFFIO_RX_B162a	DIFFOUT_B162a	AA9	DQ22B								
4A	VREFBAND	IO			PPL_BR_CLKOUT1/PPL_BR_FB0/PPL_BR_FB1	DIFFIO_RX_B162b	DIFFOUT_B162b	AA9	DQ22B								
4A	VREFBAND	IO			CLK10n	DIFFIO_TX_B163a	DIFFOUT_B163a	AT8	DQ22B								
4A	VREFBAND	IO			CLK10p	DIFFIO_TX_B163b	DIFFOUT_B163b	AT8	DQ22B								
4A	VREFBAND	IO			DIFFIO_RX_B164a	DIFFOUT_B164a	AE7	DQ5a19B/Q10B/Q20B		DQ22B							
4A	VREFBAND	IO			DIFFIO_TX_B165a	DIFFOUT_B165a	AE7	DQ5a19B/Q10B/Q20B/Q30B		DQ22B							
4A	VREFBAND	IO			DIFFIO_TX_B165b	DIFFOUT_B165b	AK8	DQ22B		DQ22B							
4A	VREFBAND	IO			DIFFIO_RX_B166a	DIFFOUT_B166a	AL3	DQ22B		DQ22B							
4A	VREFBAND	IO			DIFFIO_RX_B166b	DIFFOUT_B166b	AL1	DQ22B		DQ22B							
4A	VREFBAND	IO			DIFFIO_RX_B166c	DIFFOUT_B166c	AW4	DQ22B		DQ22B							
4A	VREFBAND	IO			RZQ_1	DIFFIO_TX_B167a	DIFFOUT_B167a	AN7	DQ22B								
4A	VREFBAND	IO			RZQ_2	DIFFIO_TX_B167b	DIFFOUT_B167b	AP7	DQ22B								
4A	VREFBAND	IO			CLK8n	DIFFIO_RX_B168a	DIFFOUT_B168a	AP6	DQ22B								
4A	VREFBAND	IO			CLK8p	DIFFIO_RX_B168b	DIFFOUT_B168b	AP6	DQ22B								
					RREF_BR		AW2	DQ10B		DQ10B							
					DN0		AV3										
					DN1		AP3										
					REFCLK0p		AE5										
GXB_R0					REFCLK0B		AP7										
GXB_R0					GXB_RX_R0a/GXB_REFCLK_R0a		AE3										
GXB_R0					GXB_RX_R0b/GXB_REFCLK_R0b		AU1										
GXB_R0					GXB_TX_R0a		AT3										
GXB_R0					GXB_TX_R0b		AT4										
GXB_R0					GXB_RX_R1a/GXB_REFCLK_R1a		AR2										
GXB_R0					GXB_RX_R1b/GXB_REFCLK_R1b		AR1										
GXB_R0					GXB_TX_R1a		AP3										
GXB_R0					GXB_TX_R1b		AP4										
GXB_R0					GXB_RX_R2a/GXB_REFCLK_R2a		AA8										
GXB_R0					GXB_RX_R2b/GXB_REFCLK_R2b		AN1										
GXB_R0					GXB_TX_R2a		AA3										
GXB_R0					GXB_TX_R2b		AA4										
GXB_R0					GXB_RX_R3a/GXB_REFCLK_R3a		AL2										
GXB_R0					GXB_RX_R3b/GXB_REFCLK_R3b		AL1										
GXB_R0					GXB_TX_R3a		AK4										
GXB_R0					GXB_RX_R4a/GXB_REFCLK_R4a		AJ2										
GXB_R0					GXB_RX_R4b/GXB_REFCLK_R4b		AJ1										
GXB_R0					GXB_TX_R4a		AP3										
GXB_R0					GXB_TX_R4b		AP4										
GXB_R0					GXB_RX_R5a/GXB_REFCLK_R5a		AM2										
GXB_R0					GXB_RX_R5b/GXB_REFCLK_R5b		AM1										
GXB_R0					GXB_TX_R5a		AE4										
GXB_R0					GXB_TX_R5b		AE5										
GXB_R0					REFCLK18p		AP9										
GXB_R1					REFCLK18n		AM8										
GXB_R1					REFCLK20p		AP9										
GXB_R1					REFCLK20n		AM9										
GXB_R1					GXB_RX_R6a/GXB_REFCLK_R6a		AE7										
GXB_R1					GXB_RX_R6b/GXB_REFCLK_R6b		AE1										
GXB_R1					GXB_TX_R6a		AD3										



Bank Number	VFREF	PinName/Function (2), (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517 (4)	DQS for X0/X3	DQS for X16/X18	DQS for X32/X36	HMC pin assignment for DQES (5)	HMC pin assignment for LPDQES (6)	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
EB	VREFBAND_HPS	HPS_DDR					L1									
EB	VREFBAND_HPS	HPS_DDR					L2				HPS_DO_35	HPS_DO_35				
EB	VREFBAND_HPS	HPS_DDR					F1				HPS_DO_31	HPS_DO_31				
EB	VREFBAND_HPS	HPS_DDR					G1				HPS_DO_21	HPS_DO_21				
EB	VREFBAND_HPS	HPS_GPI0					K3				HPS_DO_34	HPS_DO_34				
EB	VREFBAND_HPS	HPS_GPI1					J2				HPS_DO_32	HPS_DO_32				
EB	VREFBAND_HPS	HPS_DDR					D1				HPS_DM_3	HPS_DM_3				
EB	VREFBAND_HPS	HPS_GPI0					K2									
EB	VREFBAND_HPS	HPS_DDR					E1				HPS_DO_31	HPS_DO_31				
EB	VREFBAND_HPS	HPS_DDR					F2				HPS_DO_29	HPS_DO_29				
EB	VREFBAND_HPS	HPS_DDR					M3				HPS_DO_30	HPS_DO_30				
EB	VREFBAND_HPS	HPS_DDR					G2				HPS_DO_28	HPS_DO_28				
EB	VREFBAND_HPS	VREFBAND_HPS					M8									
EB	VREFBAND_HPS	HPS_DDR					C2				HPS_DQS_3	HPS_DQS_3				
EB	VREFBAND_HPS	HPS_GPI0					B1									
EB	VREFBAND_HPS	HPS_DDR					D3				HPS_DQS_3	HPS_DQS_3				
EB	VREFBAND_HPS	HPS_DDR					C1				HPS_DQS_27	HPS_DQS_27				
EB	VREFBAND_HPS	HPS_DDR					A3				HPS_DO_25	HPS_DO_25				
EB	VREFBAND_HPS	HPS_DDR					F7				HPS_DO_28	HPS_DO_28				
EB	VREFBAND_HPS	HPS_DDR					A2				HPS_DO_24	HPS_DO_24				
EB	VREFBAND_HPS	HPS_GPI0					N5									
EB	VREFBAND_HPS	HPS_DDR					K3									
EB	VREFBAND_HPS	HPS_DDR					D3				HPS_DM_2	HPS_DM_2				
EB	VREFBAND_HPS	HPS_GPI0					K4									
EB	VREFBAND_HPS	HPS_DDR					C3				HPS_DO_23	HPS_DO_23				
EB	VREFBAND_HPS	HPS_DDR					J4				HPS_DO_21	HPS_DO_21				
EB	VREFBAND_HPS	HPS_DDR					M5				HPS_DO_22	HPS_DO_22				
EB	VREFBAND_HPS	HPS_DDR					M6				HPS_DO_20	HPS_DO_20				
EB	VREFBAND_HPS	HPS_GPI0					L4									
EB	VREFBAND_HPS	HPS_DDR					G4				HPS_DQS_2	HPS_DQS_2				
EB	VREFBAND_HPS	HPS_DDR					E3				HPS_RESETr	HPS_RESETr				
EB	VREFBAND_HPS	HPS_DDR					H4				HPS_DQS_2	HPS_DQS_2				
EB	VREFBAND_HPS	HPS_DDR					F3				HPS_DO_19	HPS_DO_19				
EB	VREFBAND_HPS	HPS_DDR					K7				HPS_DO_17	HPS_DO_17				
EB	VREFBAND_HPS	HPS_DDR					N6				HPS_DO_18	HPS_DO_18				
EB	VREFBAND_HPS	HPS_GPI0					J5				HPS_DO_16	HPS_DO_16				
EB	VREFBAND_HPS	HPS_GPI4					M6									
EA	VREFBAND_HPS	HPS_GPI3					C4									
EA	VREFBAND_HPS	HPS_DDR					E4				HPS_DM_1	HPS_DM_1				
EA	VREFBAND_HPS	HPS_GPI2					B4									
EA	VREFBAND_HPS	HPS_DDR					F4									
EA	VREFBAND_HPS	HPS_DDR					A5				HPS_DO_15	HPS_DO_15				
EA	VREFBAND_HPS	HPS_DDR					R9				HPS_DO_13	HPS_DO_13				
EA	VREFBAND_HPS	HPS_DDR					R9				HPS_DO_14	HPS_DO_14				
EA	VREFBAND_HPS	HPS_DDR					A4				HPS_DO_12	HPS_DO_12				
EA	VREFBAND_HPS	HPS_DDR					R8				HPS_CK_0	HPS_CK_0				
EA	VREFBAND_HPS	HPS_DDR					D5				HPS_DQS_1	HPS_DQS_1				
EA	VREFBAND_HPS	HPS_DDR					F5				HPS_CK_1	HPS_CK_1				
EA	VREFBAND_HPS	HPS_DDR					E6				HPS_DQS_1	HPS_DQS_1				
EA	VREFBAND_HPS	HPS_DDR					G6				HPS_DO_11	HPS_DO_11				
EA	VREFBAND_HPS	HPS_DDR					G6				HPS_CK_1	HPS_CK_1				
EA	VREFBAND_HPS	HPS_DDR					N8				HPS_DO_9	HPS_DO_9				
EA	VREFBAND_HPS	HPS_DDR					N8				HPS_DO_10	HPS_DO_10				
EA	VREFBAND_HPS	HPS_DDR					M9				HPS_DO_8	HPS_DO_8				
EA	VREFBAND_HPS	HPS_GPI0					B6									
EA	VREFBAND_HPS	HPS_DDR					C8				HPS_DM_0	HPS_DM_0				
EA	VREFBAND_HPS	HPS_DDR					D6				HPS_DO_7	HPS_DO_7				
EA	VREFBAND_HPS	HPS_DDR					A7				HPS_DO_5	HPS_DO_5				
EA	VREFBAND_HPS	HPS_DDR					L6				HPS_DO_6	HPS_DO_6				
EA	VREFBAND_HPS	HPS_DDR					A6				HPS_DO_4	HPS_DO_4				
EA	VREFBAND_HPS	HPS_DDR					K6				HPS_ODT_1	HPS_ODT_1				
EA	VREFBAND_HPS	HPS_DDR					F7				HPS_DQS_0	HPS_DQS_0				
EA	VREFBAND_HPS	HPS_DDR					H7				HPS_ODT_0	HPS_ODT_0				
EA	VREFBAND_HPS	HPS_DDR					E7				HPS_DQS_0	HPS_DQS_0				
EA	VREFBAND_HPS	HPS_DDR					G7				HPS_DO_3	HPS_DO_3				
EA	VREFBAND_HPS	HPS_DDR					C7				HPS_DO_1	HPS_DO_1				
EA	VREFBAND_HPS	HPS_DDR					F10				HPS_DO_2	HPS_DO_2				
EA	VREFBAND_HPS	HPS_DDR					D7				HPS_DO_0	HPS_DO_0				
EA	VREFBAND_HPS	VREFBAND_HPS					F10									
EA	VREFBAND_HPS	HPS_DDR					N8				HPS_A_0	HPS_A_0				
EA	VREFBAND_HPS	HPS_DDR					M9				HPS_A_1	HPS_A_1				
EA	VREFBAND_HPS	HPS_DDR					AB				HPS_A_4	HPS_A_4				
EA	VREFBAND_HPS	HPS_DDR					N10				HPS_A_2	HPS_A_2				
EA	VREFBAND_HPS	HPS_DDR					B7				HPS_A_5	HPS_A_5				
EA	VREFBAND_HPS	HPS_DDR					M10				HPS_A_3	HPS_A_3				
EA	VREFBAND_HPS	HPS_DDR					A11				HPS_CK	HPS_CK				
EA	VREFBAND_HPS	HPS_DDR					B9				HPS_A_6	HPS_A_6				
EA	VREFBAND_HPS	HPS_DDR					C9				HPS_CK	HPS_CK				
EA	VREFBAND_HPS	HPS_DDR					AB				HPS_CK	HPS_CK				
EA	VREFBAND_HPS	HPS_DDR					B10				HPS_BA_1	HPS_BA_1				
EA	VREFBAND_HPS	HPS_DDR					L7				HPS_BA_0	HPS_BA_0				
EA	VREFBAND_HPS	HPS_DDR					D8				HPS_BA_2	HPS_BA_2				
EA	VREFBAND_HPS	HPS_DDR					G9				HPS_CASB	HPS_CASB				
EA	VREFBAND_HPS	HPS_DDR					G9				HPS_RASB	HPS_RASB				
EA	VREFBAND_HPS	HPS_DDR					D9				HPS_A_8	HPS_A_8				
EA	VREFBAND_HPS	HPS_DDR					K7				HPS_A_10	HPS_A_10				
EA	VREFBAND_HPS	HPS_DDR					C10				HPS_A_9	HPS_A_9				
EA	VREFBAND_HPS	HPS_DDR					J7				HPS_A_11	HPS_A_11				
EA	VREFBAND_HPS	HPS_DDR					F9				HPS_CSB_0	HPS_CSB_0				
EA	VREFBAND_HPS	HPS_DDR					F9				HPS_A_17	HPS_A_17				
EA	VREFBAND_HPS	HPS_DDR					J8				HPS_CSB_1	HPS_CSB_1				
EA	VREFBAND_HPS	HPS_DDR					E9				HPS_A_13	HPS_A_13				
EA	VREFBAND_HPS	HPS_DDR					D11				HPS_A_14	HPS_A_14				
EA	VREFBAND_HPS	HPS_DDR					J8				HPS_W#	HPS_W#				
EA	VREFBAND_HPS	HPS_DDR					D10				HPS_A_15	HPS_A_15				
EA	VREFBAND_HPS	HPS_DQS_0					K9									
EA	VREFBAND_HPS	HPS_DQS_0					B12									
EA	VREFBAND_HPS	HPS_DQS_0					C11									
EA	VREFBAND_HPS	HPS_DQS_0					A12									
EA	VREFBAND_HPS	HPS_DQS_0					B12									
EA	VREFBAND_HPS	HPS_DQS_0					F10									
EA	VREFBAND_HPS	HPS_DQS_0					G10									
EA	VREFBAND_HPS	HPS_DQS_0					F11									
EA	VREFBAND_HPS	HPS_DQS_0					H10									
EA	VREFBAND_HPS	HPS_DQS_0					M11									
EA	VREFBAND_HPS	HPS_DQS_0					C12									
EA	VREFBAND_HPS	HPS_CLK1					N11									
EA	VREFBAND_HPS	HPS_CLK2					D12									
EA	VREFBAND_HPS	TRACE_CLK					L11						TRACE_CLK			
EA	VREFBAND_HPS	TRACE_DO					K12						SPR0_CLK	UART0_RX		HPS_GP1048
EA	VREFBAND_HPS	TRACE_D1					X11						TRACE_D0			
EA	VREFBAND_HPS	TRACE_D0					J12						SPR0_M0B	UART0_TX		HPS_GP1049
EA	VREFBAND_HPS	TRACE_D2					H12						TRACE_D2			
EA	VREFBAND_HPS	TRACE_D3					H12						SPR0_SSD	I2C1_SCL		HPS_GP1050
EA	VREFBAND_HPS	TRACE_D4					F12						TRACE_D4			
EA	VREFBAND_HPS	TRACE_D5					G11						SPR1_M0B			HPS_GP1051
EA	VREFBAND_HPS	TRACE_D6					F12						TRACE_D5			
EA	VREFBAND_HPS	TRACE_D7					A13						SPR1_SSD	I2C0_SDA		HPS_GP1052
EA	VREFBAND_HPS	SP1M0_CLK					P12						TRACE_D7			
EA	VREFBAND_HPS	SP1M0_CLK					F12						SP1M0_CLK	I2C1_SDA	UART0_CTS	HPS_GP1057
EA	VREFBAND_HPS	SP1M0_M0B					A14						SPR1_M0B	I2C1_SCL	UART0_RTS	HPS_GP1058
EA	VREFBAND_HPS	SP1M0_M0B					N12						SPR1_M0B	I2C0_SCL		HPS_GP1059
EA	VREFBAND_HPS	SP1M0_SS0/00TSSEL0					B15						SPR1M0_SS0	UART1_RTS		HPS_GP1060
EA	VREFBAND_HPS	UART0_RX					B14						UART0_RX			
EA	VREFBAND_HPS	UART0_TX/CLKSEL1														



Bank Number	REF	PinName/Function (2), (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517 (4)	DQS for X8/X9	DQS for X16/X18	DQS for X32/X36	HMC pin assignment for DQES J0	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
7A	VREF7A7B7C7D7E7HPS	SPB1_M0B0					E13						SPB1_M0S0	SPM1_M0S0		HPS_GP068
7A	VREF7A7B7C7D7E7HPS	SPB1_M0B1					E13						SPB1_M0S1	SPM1_M0S1		HPS_GP069
7A	VREF7A7B7C7D7E7HPS	SPB1_S0B0					G13						SPB1_S0S0	SPM1_S0S0		HPS_GP070
7A	VREF7A7B7C7D7E7HPS	LIART1_RX					G13						LIART1_TX	SPM1_S0S1		HPS_GP069
7A	VREF7A7B7C7D7E7HPS	LIART1_TX					N13						SPM1_CLK	SPM1_S0S2		HPS_GP069
7A	VREF7A7B7C7D7E7HPS	R13					R13						ZC1_S0A	SPM1_M0S1		HPS_GP064
7A	VREF7A7B7C7D7E7HPS	ZC1_SCL					M14						ZC1_SCL	SPM1_M0S0		HPS_GP065
7A	VREF7A7B7C7D7E7HPS	SPM1_S0B0					F13						SPM1_S0S0	SPM1_S0S0		HPS_GP074
7A	VREF7A7B7C7D7E7HPS	SPB0_CLK					H13						SPB0_CLK	SPM1_S0S1		HPS_GP067
7A	VREF7A7B7C7D7E7HPS	SPB0_M0B0					C14						SPB0_M0S0			HPS_GP068
7A	VREF7A7B7C7D7E7HPS	SPB0_M0D0					J13						SPB0_M0S0			HPS_GP069
7A	VREF7A7B7C7D7E7HPS	SPB0_S0B0					D14						SPB0_S0S0			HPS_GP070
7B	VREF7A7B7C7D7E7HPS	NAND_ALE					A16						NAND_ALE	RGM1I_TX_CLK	QSPI_S03	HPS_GP014
7B	VREF7A7B7C7D7E7HPS	NAND_C0					F15						RGM1I_TXD0	USB1_D0		HPS_GP015
7B	VREF7A7B7C7D7E7HPS	NAND_C1E					A17						RGM1I_TXD1	USB1_D1		HPS_GP016
7B	VREF7A7B7C7D7E7HPS	NAND_AE					F15						RGM1I_TXD2	USB1_D2		HPS_GP017
7B	VREF7A7B7C7D7E7HPS	NAND_S0					C16						RGM1I_TXD3	USB1_D3		HPS_GP018
7B	VREF7A7B7C7D7E7HPS	NAND_D00					G14						RGM1I_RXD0			HPS_GP019
7B	VREF7A7B7C7D7E7HPS	NAND_D01					B17						RGM1I_M0D0	ZC1_S0A		HPS_GP020
7B	VREF7A7B7C7D7E7HPS	NAND_D02					H14						RGM1I_M0C0	ZC1_SCL		HPS_GP021
7B	VREF7A7B7C7D7E7HPS	NAND_D03					L15						RGM1I_RX_CTL	USB1_D4		HPS_GP022
7B	VREF7A7B7C7D7E7HPS	NAND_D04					F14						RGM1I_TX_CTL	USB1_D5		HPS_GP023
7B	VREF7A7B7C7D7E7HPS	NAND_D05					K16						RGM1I_RX_CLK	USB1_D6		HPS_GP024
7B	VREF7A7B7C7D7E7HPS	NAND_D06					R14						RGM1I_RXD1	USB1_D7		HPS_GP025
7B	VREF7A7B7C7D7E7HPS	NAND_D07					K14						RGM1I_TXD1	USB1_D7		HPS_GP026
7B	VREF7A7B7C7D7E7HPS	NAND_WP					C15						RGM1I_RXD0	QSPI_S02		HPS_GP027
7B	VREF7A7B7C7D7E7HPS	NAND_WE_BOOTSEL1					L16						QSPI_S01			HPS_GP028
7B	VREF7A7B7C7D7E7HPS	QSPI_D0					D15						QSPI_D1	USB1_CLK		HPS_GP029
7B	VREF7A7B7C7D7E7HPS	QSPI_D1					G15						QSPI_D0	USB1_STP		HPS_GP030
7B	VREF7A7B7C7D7E7HPS	QSPI_D2					H15						QSPI_D3	USB1_DK1		HPS_GP031
7B	VREF7A7B7C7D7E7HPS	QSPI_D3					H15						QSPI_D2	USB1_NXT		HPS_GP032
7B	VREF7A7B7C7D7E7HPS	QSPI_S0_BOOTSEL1					N15						QSPI_S00			HPS_GP033
7B	VREF7A7B7C7D7E7HPS	QSPI_CLK					F15						QSPI_CLK			HPS_GP034
7B	VREF7A7B7C7D7E7HPS	QSPI_S01					E15						QSPI_S01			HPS_GP035
7C	VREF7A7B7C7D7E7HPS	SDMMC_CMD					D16						SDMMC_CMD	USB0_D0		HPS_GP036
7C	VREF7A7B7C7D7E7HPS	SDMMC_P10EN					F16						SDMMC_P10EN	USB0_D1		HPS_GP037
7C	VREF7A7B7C7D7E7HPS	SDMMC_D0					C17						SDMMC_D0	USB0_D2		HPS_GP038
7C	VREF7A7B7C7D7E7HPS	SDMMC_D1					N16						SDMMC_D1	USB0_D3		HPS_GP039
7C	VREF7A7B7C7D7E7HPS	SDMMC_D4					F16						SDMMC_D4	USB0_D4		HPS_GP040
7C	VREF7A7B7C7D7E7HPS	SDMMC_D6					G16						SDMMC_D6	USB0_D5		HPS_GP041
7C	VREF7A7B7C7D7E7HPS	SDMMC_D8					F16						SDMMC_D8	USB0_D6		HPS_GP042
7C	VREF7A7B7C7D7E7HPS	SDMMC_D7					H16						SDMMC_D7	USB0_D7		HPS_GP043
7C	VREF7A7B7C7D7E7HPS	HPS_GP044					K16						USB0_CLK			HPS_GP044
7C	VREF7A7B7C7D7E7HPS	SDMMC_CLK_OUT					L16						USB0_STP			HPS_GP045
7C	VREF7A7B7C7D7E7HPS	SDMMC_D9					J16						SDMMC_CLK_OUT			HPS_GP046
7C	VREF7A7B7C7D7E7HPS	SDMMC_D3					M16						USB0_NXT			HPS_GP047
7D	VREF7A7B7C7D7E7HPS	RGM1I_TX_CLK					R17						RGM1I_TX_CLK			HPS_GP050
7D	VREF7A7B7C7D7E7HPS	RGM1I_TXD0					F17						USB1_D0			HPS_GP051
7D	VREF7A7B7C7D7E7HPS	RGM1I_TXD1					F17						USB1_D1			HPS_GP052
7D	VREF7A7B7C7D7E7HPS	RGM1I_TXD2					F18						USB1_D2			HPS_GP053
7D	VREF7A7B7C7D7E7HPS	RGM1I_TXD3					E18						USB1_D3			HPS_GP054
7D	VREF7A7B7C7D7E7HPS	RGM1I_RXD0					K17						USB1_D4			HPS_GP055
7D	VREF7A7B7C7D7E7HPS	RGM1I_M0D0					D18						USB1_D5	ZC1_S0A		HPS_GP056
7D	VREF7A7B7C7D7E7HPS	RGM1I_M0C0					A17						USB1_D6	ZC1_SCL		HPS_GP057
7D	VREF7A7B7C7D7E7HPS	RGM1I_RX_CTL					B17						RGM1I_RX_CTL	USB1_D7		HPS_GP058
7D	VREF7A7B7C7D7E7HPS	RGM1I_TX_CTL					A18						RGM1I_TX_CTL			HPS_GP059
7D	VREF7A7B7C7D7E7HPS	RGM1I_RX_CLK					C18						RGM1I_RX_CLK	USB1_CLK		HPS_GP060
7D	VREF7A7B7C7D7E7HPS	RGM1I_RXD1					A19						RGM1I_RXD1	USB1_STP		HPS_GP061
7D	VREF7A7B7C7D7E7HPS	RGM1I_RXD2					C19						RGM1I_RXD2	USB1_DK2		HPS_GP062
7D	VREF7A7B7C7D7E7HPS	RGM1I_RXD3					G18						RGM1I_RXD3	USB1_NXT		HPS_GP063
7D	VREF7A7B7C7D7E7HPS	RGM1I_TX_CLK					D19						RGM1I_TX_CLK			HPS_GP064
7D	VREF7A7B7C7D7E7HPS	RGM1I_TXD0					H18						RGM1I_TXD0			HPS_GP065
7D	VREF7A7B7C7D7E7HPS	RGM1I_TXD1					F19						RGM1I_TXD1			HPS_GP066
7D	VREF7A7B7C7D7E7HPS	RGM1I_TX_CTL					H19						RGM1I_TX_CTL			HPS_GP067
7D	VREF7A7B7C7D7E7HPS	RGM1I_RXD0					E19						RGM1I_RXD0			HPS_GP068
7D	VREF7A7B7C7D7E7HPS	RGM1I_RXD1					M17						RGM1I_RXD1			HPS_GP069
7E	VREF7A7B7C7D7E7HPS	RGM1I_M0D0					J18						SPM1_M0S0	SPM1_M0S0		HPS_GP054
7E	VREF7A7B7C7D7E7HPS	RGM1I_M0C0					L18						RGM1I_M0C0	SPM1_M0S1	SPM1_M0S1	HPS_GP055
7E	VREF7A7B7C7D7E7HPS	RGM1I_TXD0					E18						RGM1I_TXD0	SPM1_M0S2	SPM1_M0S2	HPS_GP056
7E	VREF7A7B7C7D7E7HPS	RGM1I_TXD1					F18						RGM1I_TXD1	SPM1_S0S0	SPM1_S0S0	HPS_GP057
7E	VREF7A7B7C7D7E7HPS	RGM1I_TXD2					G17						RGM1I_TXD2	SPM1_S0S1	SPM1_S0S1	HPS_GP058
7E	VREF7A7B7C7D7E7HPS	RGM1I_RX_CLK					G21						RGM1I_RX_CLK	SPM1_CLK	SPM1_CLK	HPS_GP059
7E	VREF7A7B7C7D7E7HPS	RGM1I_RX_CTL					H19						RGM1I_RX_CTL	SPM1_M0S0	SPM1_M0S0	HPS_GP060
7E	VREF7A7B7C7D7E7HPS	RGM1I_RXD2					G20						RGM1I_RXD2	SPM1_M0S1	SPM1_M0S1	HPS_GP061
7E	VREF7A7B7C7D7E7HPS	RGM1I_RXD3					G19						RGM1I_RXD3	SPM1_S0S0	SPM1_S0S0	HPS_GP062
7G	VREF7GND				DIFFO_RX_T16p	DIFFOUT_T16p	R19									
7G	VREF7GND				DIFFO_RX_T16n	DIFFOUT_T16n	T19									
7G	VREF7GND						F20									
7G	VREF7GND			VREF7GND			P19									
7G	VREF7GND				DIFFO_RX_T17p	DIFFOUT_T17p	J19									
7G	VREF7GND				DIFFO_RX_T17n	DIFFOUT_T17n	L19									
7G	VREF7GND				DIFFO_TX_T18p	DIFFOUT_T18p	L19									
7G	VREF7GND				DIFFO_RX_T19p	DIFFOUT_T19p	P20									
7G	VREF7GND				DIFFO_RX_T19n	DIFFOUT_T19n	P20									
7G	VREF7GND				DIFFO_TX_T20p	DIFFOUT_T20p	M19									
7G	VREF7GND				DIFFO_RX_T21p	DIFFOUT_T21p	L20									
7G	VREF7GND				DIFFO_RX_T21n	DIFFOUT_T21n	M20									
	VCCP_FPLL						V19									
	CLK1p						F20									
8D	VREF8DND			CLK1p	DIFFO_RX_T31p	DIFFOUT_T31p	G20	DOIT								DOIT
8D	VREF8DND			CLK1Bn												







Bank Number	VREF	PinName/Function (2), (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517 (4)	DQS for X0/X9	DQS for X16/X18	DQS for X32/X36	HMC pin assignment for DQS3 (5)	HMC pin assignment for PDS2 (6)	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
BA	VREFBAND	I0			DIFFIO_TX_T112n	DIFFFOUT_T112n	G32									
BA	VREFBAND	I0	CL200b		DIFFIO_RX_T113p	DIFFFOUT_T113p	G34	DQ11T								
BA	VREFBAND	I0	CL200b		DIFFIO_RX_T113p	DIFFFOUT_T113p	G34	DQ11T								
BA	VREFBAND	I0			DIFFIO_TX_T114p	DIFFFOUT_T114p	E33	DQ11T								
BA	VREFBAND	I0	RZQ_6		DIFFIO_TX_T114n	DIFFFOUT_T114n	F33									
BA		MSEL0		MSEL0			H35									
BA		MSEL1		MSEL1			A34									
BA		MSEL2		MSEL2			D35									
BA		MSEL3		MSEL3			A37									
BA		MSEL4		MSEL4			IP34									
BA		CONF_DONE		CONF_DONE			K35									
BA		nSTATUS		nSTATUS			F35									
BA		nCE		nCE			M35									
BA		nCONENFG		nCONENFG			A36									
		GND					P35									
		VCC_IOPS					V16									
		GND					W16									
		GND					AA33									
		GND					AA35									
		GND					AA38									
		GND					AA39									
		GND					AB31									
		GND					AB32									
		GND					AB34									
		GND					AB36									
		GND					AB37									
		GND					AC33									
		GND					AC38									
		GND					AC39									
		GND					AD32									
		GND					AD36									
		GND					AD37									
		GND					AE33									
		GND					AE35									
		GND					AE38									
		GND					AE39									
		GND					AF31									
		GND					AF32									
		GND					AF34									
		GND					AF36									
		GND					AG37									
		GND					AG38									
		GND					AG39									
		GND					AH33									
		GND					AH33									
		GND					AH34									
		GND					AH35									
		GND					AH36									
		GND					AM37									
		GND					AL35									
		GND					AJ38									
		GND					AJ39									
		GND					AK36									
		GND					AK37									
		GND					AL35									
		GND					AL38									
		GND					AL39									
		GND					AM38									
		GND					AM37									
		GND					AN35									
		GND					AN38									
		GND					AN39									
		GND					AP38									
		GND					AP37									
		GND					AP35									
		GND					AP38									
		GND					AP39									
		GND					AT36									
		GND					AT37									
		GND					AU35									
		GND					AU38									
		GND					AV39									
		GND					AV35									
		GND					AV38									
		GND					AV37									
		GND					AV38									
		GND					AV39									
		GND					AV35									
		GND					AV38									
		GND					BA36									
		GND					B37									
		GND					C35									
		GND					C38									
		GND					C39									
		GND					D36									
		GND					D37									
		GND					E35									
		GND					E38									
		GND					E39									
		GND					F36									
		GND					F37									
		GND					G35									
		GND					G38									
		GND					G39									
		GND					H35									
		GND					H37									
		GND					J35									
		GND					J38									
		GND					J39									
		GND					K36									
		GND					K37									
		GND					L36									
		GND					L39									
		GND					M35									
		GND					M37									
		GND					N35									
		GND					N38									
		GND					N39									
		GND					P36									
		GND					P37									
		GND					R34									
		GND					R38									
		GND					R39									
		GND					T32									
		GND					T38									
		GND					T37									
		GND					U33									
		GND					U35									
		GND					U36									
		GND					U39									
		GND					V32									
		GND					V34									
		GND					V36									
		GND					V37									
		GND					W33									
		GND					W38									
		GND					W39									
		GND					Y31									
		GND					Y32									



Bank Number	VREF	PinName/Function (2), (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517 (4)	DQS for X8/X9	DQS for X16/X18	DQS for X32/X36	HMC pin assignment for DQS3 (5)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		GND					Y36									
		GND					Y35									
		GND					AA3									
		GND					AA4									
		GND					AA6									
		GND					AA8									
		GND					AB1									
		GND					AB2									
		GND					AB7									
		GND					AC3									
		GND					AC4									
		GND					AC8									
		GND					AD1									
		GND					AD2									
		GND					AD5									
		GND					AD7									
		GND					AE3									
		GND					AE4									
		GND					AE5									
		GND					AE8									
		GND					AF1									
		GND					AF2									
		GND					AP9									
		GND					AG3									
		GND					AG4									
		GND					AG5									
		GND					AG6									
		GND					AG7									
		GND					AG8									
		GND					AH1									
		GND					AH2									
		GND					AH5									
		GND					AL3									
		GND					AL4									
		GND					AK1									
		GND					AK2									
		GND					AK5									
		GND					AL3									
		GND					AL4									
		GND					AM1									
		GND					AM2									
		GND					AM5									
		GND					AN3									
		GND					AN4									
		GND					AP1									
		GND					AP2									
		GND					AP5									
		GND					AR3									
		GND					AR4									
		GND					AT1									
		GND					AT2									
		GND					AT5									
		GND					AT3									
		GND					AU4									
		GND					AV1									
		GND					AV2									
		GND					N3									
		GND					N4									
		GND					P1									
		GND					P2									
		GND					PS									
		GND					R3									
		GND					R4									
		GND					RS									
		GND					T1									
		GND					T2									
		GND					TS									
		GND					U3									
		GND					U4									
		GND					U5									
		GND					U6									
		GND					V1									
		GND					V2									
		GND					V7									
		GND					W3									
		GND					W4									
		GND					W8									
		GND					Y1									
		GND					Y2									
		GND					Y8									
		GND					Y7									
		VCCP					AB21									
		VCCP					AB25									
		VCCP					AB15									
		VCCP					U10									
		VCCP					U16									
		VCCP					V25									
		VCCP					V27									
		VCCP					W10									
		VCCP					V27									
		VCCA_FP1L					AC30									
		VCCA_FP1L					AD9									
		VCCA_FP1L					Y30									
		VCCA_FP1L					AA8									
		VCCA_FP1L					V31									
		VCCP_HPS					U8									
		VCCP_HPS					R33									
		VCC_AUX					AB14									
		VCC_AUX					AB8									
		VCC_AUX					U28									
		VCC_AUX_SHARED					U15									
		VCCD_FP1L					AB1									
		VCCD_FP1L					AB9									
		VCCD_FP1L					W30									
		VCCD_FP1L					W9									
		VCCD_FP1L					T31									
		VCCA_GXBLO					AF33									
		VCCA_GXBRO					AE7									
		VCCA_GXB1					AB33									
		VCCA_GXB1					AB7									
		VCCA_GXB2					V33									
		VCCD_GXBLO					AD33									
		VCCD_GXBRO					AE7									
		VCCD_GXB1					Y33									
		VCCD_GXB1					W7									
		VCCD_GXB2					T33									
		VCCD_GXBLO					AD34									
		VCCD_GXBLO					AD35									
		VCCD_GXBRO					AE5									
		VCCD_GXBRO					AE6									
		VCCD_GXB1					Y34									
		VCCD_GXB1					Y35									
		VCCD_GXB1					W5									
		VCCD_GXB1					W6									
		VCCD_GXB2					T34									
		VCCD_GXB2					T35									
		VCCD_GXB1					U34									
		VCCD_GXB1					W34									
		VCCD_GXB1					AA34									
		VCCD_GXB1					AB35									





Bank Number	VREF	PinName/Function (2), (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F15T (4)	DQS for X8/X9	DQS for X16/X18	DQS for X32/X36	HMC pin assignment for DQS3 (5)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		VCCIOBA					G33									
		VCCIOBA					K31									
		VCCIOBA					K31									
		VCCIOBA					P33									
		VCCIOBB					E38									
		VCCIOBB					E30									
		VCCIOBB					H30									
		VCCIOBB					K28									
		VCCIOBC					C25									
		VCCIOBC					D27									
		VCCIOBC					F25									
		VCCIOBC					G27									
		VCCIOBC					J26									
		VCCIOBC					M24									
		VCCIOBD					G21									
		VCCIOBD					D32									
		VCCIOBD					F21									
		VCCIOBD					G22									
		VCCIOBD					K22									
		VCCIOBD					M21									
		VCCPD3					AA27									
		VCCPD3					AA28									
		VCCPD3					AA29									
		VCCPD3					AB22									
		VCCPD3					AB23									
		VCCPD3					AB24									
		VCCPD3					AB25									
		VCCPD4A					AE10									
		VCCPD4A					AE10									
		VCCPD4B					AB12									
		VCCPD4B					AB13									
		VCCPD4B					AB16									
		VCCPD4B					AB18									
		VCCPD4B					AB19									
		VCCPD6AB_HPS					L9									
		VCCPD6AB_HPS					T10									
		VCCPD6AB_HPS					T6									
		VCCPD7A_HPS					T8									
		VCCPD7A_HPS					R12									
		VCCPD7B_HPS					T14									
		VCCPD7C_HPS					T16									
		VCCPD7D_HPS					T17									
		VCCPD7E_HPS					R18									
		VCCPD7E_HPS					U21									
		VCCPD8					R32									
		VCCPD8					T30									
		VCCPD8					U22									
		VCCPD8					U24									
		VCCPD8					U26									
		VCCPD8					U29									
		VCCPD8M					J19									
		VCCPD8M					AE29									
		VCCPD8M					L10									
		VCC_HPS					T13									
		VCC_HPS					U14									
		VCC_HPS					U9									
		VCC_HPS					V10									
	VREFB/A/TX/C/D7END_HPS	VREFB/A/TX/C/D7END_HPS					PA16									
		GND					AA11									
		GND					AA13									
		GND					AA15									
		GND					AA17									
		GND					AA19									
		GND					AA23									
		GND					AA30									
		GND					AB10									
		GND					AE11									
		GND					AF14									
		GND					AG17									
		GND					AG20									
		GND					AF23									
		GND					AG26									
		GND					AG28									
		GND					AB10									
		GND					AE30									
		GND					AE11									
		GND					AE14									
		GND					AF17									
		GND					AG20									
		GND					AF23									
		GND					AF26									
		GND					AF28									
		GND					AF30									
		GND					AG31									
		GND					AG32									
		GND					AJ11									
		GND					AJ14									
		GND					AJ17									
		GND					AJ20									
		GND					AK23									
		GND					AL26									
		GND					AJ29									
		GND					AL32									
		GND					AL38									
		GND					AM11									
		GND					AM14									
		GND					AM17									
		GND					AM20									
		GND					AM23									
		GND					AM26									
		GND					AM28									
		GND					AM30									
		GND					AR11									
		GND					AR14									
		GND					AR17									
		GND					AR20									
		GND					AR23									
		GND					AR26									
		GND					AR29									
		GND					AR32									
		GND					AR8									
		GND					AV11									
		GND					AV14									
		GND					AV17									
		GND					AV20									
		GND					AV23									
		GND					AV26									
		GND					AV29									
		GND					AV32									
		GND					AV38									
		GND					AV38									
		GND					B11									
		GND					B16									
		GND					B2									
		GND					B20									
		GND					B23									
		GND					B26									
		GND					B29									



Bank Number	VREF	PinName/Function (2), (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1517 (4)	DQS for X8/X9	DQS for X16/X18	DQS for X32/X36	HMC pin assignment for DDR3 (5)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		GND					B02									
		GND					B5									
		GND					B6									
		GND					E11									
		GND					E17									
		GND					E2									
		GND					E20									
		GND					E23									
		GND					E26									
		GND					E29									
		GND					E32									
		GND					E5									
		GND					E8									
		GND					F14									
		GND					H11									
		GND					H17									
		GND					H2									
		GND					H20									
		GND					H23									
		GND					H26									
		GND					H29									
		GND					H32									
		GND					H5									
		GND					H8									
		GND					H21									
		GND					H29									
		GND					H32									
		GND					H5									
		GND					H8									
		GND					K0									
		GND					K20									
		GND					L1									
		GND					L17									
		GND					L2									
		GND					L23									
		GND					L26									
		GND					L29									
		GND					L32									
		GND					L6									
		GND					L8									
		GND					N14									
		GND					N17									
		GND					N20									
		GND					P11									
		GND					P23									
		GND					P26									
		GND					P29									
		GND					P32									
		GND					P5									
		GND					W21									
		GND					T12									
		GND					T15									
		GND					T16									
		GND					T18									
		GND					T20									
		GND					T9									
		GND					U11									
		GND					U13									
		GND					U17									
		GND					U23									
		GND					U26									
		GND					U27									
		GND					U30									
		GND					U7									
		GND					V14									
		GND					V8									
		GND					V18									
		GND					V21									
		GND					V24									
		GND					V26									
		GND					V28									
		GND					V30									
		GND					V8									
		GND					W27									
		GND					W11									
		GND					W13									
		GND					W15									
		GND					W17									
		GND					W19									
		GND					W23									
		GND					W25									
		GND					W29									
		GND					V10									
		GND					V12									
		GND					V14									
		GND					V15									
		GND					V18									
		GND					V20									
		GND					V22									
		GND					V24									
		GND					V26									
		GND					V28									

Notes:  
 (1) For more information about pin definitions and pin connection guidelines, refer to the [Arria V Device Family Pin Connection Guidelines](#).  
 (2) GND\_AREFCLK pin is not supported in current Quartus II version, but will be supported in future Quartus II release version.  
 (3) Pins with \* contains similar name with other pins in the same column. For the selection of the "HPS Pin Mux Select x" columns.  
 (4) Pins with # are the 10 Gbps transceiver channels. For more information about the 10 Gbps transceiver channels clocking recommendation, refer to the [Transceiver Clocking in Arria V Devices chapter](#).  
 (5) RESET pin is only applicable for DDR3 device.



Pin Information for the Arria® V 5ASTFD5 Device  
Version 1.3

Version Number	Date	Changes Made
1.0	4/19/2013	Initial release.
1.1	9/30/2014	Remove corresponding bank number from VCCRSTCLK_HPS pin.
1.2	7/31/2015	Renamed the following columns: - Renamed "DDR3/DDR2 hard memory PHY" to "HMC pin assignment for DDR3". - Renamed "LPDDR2 hard memory PHY" to "HMC pin assignment for LPDDR2".
1.3	12/23/2016	-Renamed SDMMC_FB_CLK_IN to HPS_GPIO44.