













Bank Number	VREF	PinName/Function (3), (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	R896 (4)	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for DDR3 (5)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		GND					U24									
		GND					U25									
		GND					U26									
		GND					U29									
		GND					U30									
		GND					V23									
		GND					V27									
		GND					V28									
		GND					W24									
		GND					W29									
		GND					W35									
		GND					Y23									
		GND					Y25									
		GND					Y26									
		GND					Y27									
		GND					Y28									
		GND					AA1									
		GND					AA2									
		GND					AA7									
		GND					AB3									
		GND					AB4									
		GND					AB5									
		GND					AB6									
		GND					AC1									
		GND					AC2									
		GND					AC5									
		GND					AD3									
		GND					AD4									
		GND					AE1									
		GND					AE2									
		GND					AE5									
		GND					AF3									
		GND					AF4									
		GND					AG1									
		GND					AG2									
		GND					AG5									
		GND					AH3									
		GND					AH4									
		GND					AJ1									
		GND					AJ2									
		GND					TI									
		GND					T4									
		GND					L1									
		GND					L2									
		GND					L5									
		GND					L6									
		GND					V3									
		GND					V4									
		GND					V8									
		GND					W1									
		GND					W2									
		GND					W5									
		GND					W7									
		GND					Y3									
		GND					Y4									
		GND					Y6									
		GND					Y8									
		VCCP					AB10									
		VCCP					AB14									
		VCCP					AB17									
		VCCP					AB20									
		VCCP					AC19									
		VCCP					P10									
		VCCP					RI7									
		VCCP					R21									
		VCCP					T10									
		VCCA_FPLL					V9									
		VCCA_FPLL					V22									
		VCCPLL_HPS					L10									
		VCCBAT					H25									
		VCC_AUX					AB11									
		VCC_AUX					AB18									
		VCC_AUX					R20									
		VCC_AUX_SHARED					R13									
		VCCD_FPLL					V9									
		VCCD_FPLL					Y22									
		VCCA_GXBR0					W6									
		VCCA_GXBL1					W20									
		VCCD_GXBR0					V7									
		VCCD_GXBL1					V24									
		VCCD_GXBR0					V5									
		VCCD_GXBR0					V6									
		VCCD_GXBL1					V25									
		VCCD_GXBL1					V26									
		VCCR_GXBL					AA25									
		VCCR_GXBL					AA26									
		VCCR_GXBR					AA5									
		VCCR_GXBR					AA6									
		VCCD_GXBR0					V5									
		VCCD_GXBR0					V7									
		VCCD_GXBL1					W25									
		VCCD_GXBL1					V24									
		VCC					AA10									
		VCC					AA13									
		VCC					AA14									
		VCC					AA16									
		VCC					AA18									
		VCC					AA19									
		VCC					AA20									
		VCC					T17									
		VCC					T19									
		VCC					T21									
		VCC					T22									
		VCC					U16									
		VCC					U18									
		VCC					U20									
		VCC					V15									
		VCC					V17									
		VCC					V19									
		VCC					V21									
		VCC					W12									
		VCC					W14									
		VCC					W18									
		VCC					W20									
		VCC					Y11									
		VCC					Y13									
		VCC					Y15									



Bank Number	VREF	PinName/Function (3), (2)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	R896 (4)	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for DDR3 (5)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		VCC					Y16									
		VCC					Y17									
		VCC					Y19									
		VCC					Y21									
		VCC					W16									
		VCC_HPS					R12									
		VCC_HPS					T11									
		VCC_HPS					T13									
		VCC_HPS					U12									
		VCC_HPS					U13									
		VCC_HPS					U14									
		VCC_HPS					V11									
		VCC_HPS					V13									
		VCCD0A					AE19									
		VCCD0A					AE22									
		VCCD0A					AF26									
		VCCD0A					AH19									
		VCCD0A					AH22									
		VCCD0A					AH26									
		VCCD0B					AE13									
		VCCD0B					AE16									
		VCCD0B					AH15									
		VCCD0B					AE11									
		VCCD0B					AD19									
		VCCD0A					AD5									
		VCCD0A					AE7									
		VCCD0A					AP5									
		VCCD0A					AM5									
		VCCD0A					AH7									
		VCCD0A_HPS					C2									
		VCCD0A_HPS					C5									
		VCCD0A_HPS					C8									
		VCCD0A_HPS					F2									
		VCCD0A_HPS					F4									
		VCCD0A_HPS					F6									
		VCCD0A_HPS					H1									
		VCCD0A_HPS					J5									
		VCCD0B_HPS					L4									
		VCCD0B_HPS					M4									
		VCCD0B_HPS					N1									
		VCCD0B_HPS					N6									
		VCCD0B_HPS					T2									
		VCCD0B_HPS					T5									
		VCCD0A_HPS					B14									
		VCCD0A_HPS					B17									
		VCCD0A_HPS					G10									
		VCCD0A_HPS					M10									
		VCCD0B_HPS					R20									
		VCCD0B_HPS					E12									
		VCCD0C_HPS					E14									
		VCCD0D_HPS					E18									
		VCCD0D_HPS					J14									
		VCCD0E_HPS					G15									
		VCCD0A					F29									
		VCCD0A					J27									
		VCCD0A					J29									
		VCCD0A					M29									
		VCCD0A					N24									
		VCCD0A					N27									
		VCCD0B					E27									
		VCCD0B					F25									
		VCCD0B					K23									
		VCCD0C					D25									
		VCCD0C					F23									
		VCCD0C					J11									
		VCCD0C					L19									
		VCCD0D					E21									
		VCCD0D					K17									
		VCCP03					AB21									
		VCCP03					AC18									
		VCCP03					AC24									
		VCCP04					AB7									
		VCCP06A6B_HPS					AB8									
		VCCP06A6B_HPS					AB9									
		VCCP06A6B_HPS					AB									
		VCCP06A6B_HPS					UB									
		VCCP07A_HPS					N11									
		VCCP07B_HPS					L12									
		VCCP07C_HPS					M13									
		VCCP07D_HPS					M16									
		VCCP07E_HPS					J15									
		VCCP08					P18									
		VCCP08					P22									
		VCCD0B					R19									
		VCCP0B					R24									
		VCCP0M					F12									
		VCCP0M					AD26									
		VCCP0TCLK_HPS					C9									
		VCC_HPS					R10									
		VCC_HPS					R11									
		VCC_HPS					R14									
		VCC_HPS					R15									
		VREFB7A/B7C7D7E0_HPS		VREFB7A/B7C7D7E0_HPS			F14									
		GND					AA11									
		GND					AA13									
		GND					AA15									
		GND					AA17									
		GND					AA21									
		GND					AB19									
		GND					AB8									
		GND					AB9									
		GND					AC11									
		GND					AC14									
		GND					AC17									
		GND					AC20									
		GND					AC23									
		GND					AD8									
		GND					AF11									
		GND					AF14									
		GND					AF17									
		GND					AF20									
		GND					AF23									
		GND					AF8									
		GND					AJ14									
		GND					AJ14									
		GND					AJ17									
		GND					AJ20									



Bank Number	VREF	PinName/Function (2), (3)	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	FB96 (4)	DQS for X8/X9	DQS for X16/ X18	DQS for X32/ X36	HMC pin assignment for DDR3 (5)	HMC pin assignment for LPDDR2	HPS Pin Mux Select 3	HPS Pin Mux Select 2	HPS Pin Mux Select 1	HPS Pin Mux Select 0
		GND					A123									
		GND					A126									
		GND					A15									
		GND					A16									
		GND					B11									
		GND					B2									
		GND					B23									
		GND					B26									
		GND					B29									
		GND					B5									
		GND					B8									
		GND					E17									
		GND					E2									
		GND					E20									
		GND					E23									
		GND					E26									
		GND					E29									
		GND					E5									
		GND					E8									
		GND					G12									
		GND					G14									
		GND					H17									
		GND					H2									
		GND					H20									
		GND					H23									
		GND					H26									
		GND					H29									
		GND					H5									
		GND					H8									
		GND					K11									
		GND					K14									
		GND					L17									
		GND					L2									
		GND					L20									
		GND					L23									
		GND					L26									
		GND					L29									
		GND					L5									
		GND					L8									
		GND					N10									
		GND					N14									
		GND					P11									
		GND					P17									
		GND					P16									
		GND					P2									
		GND					P20									
		GND					P23									
		GND					P26									
		GND					P29									
		GND					P5									
		GND					P8									
		GND					R18									
		GND					T12									
		GND					T14									
		GND					T18									
		GND					T20									
		GND					U11									
		GND					U15									
		GND					U17									
		GND					U19									
		GND					U21									
		GND					U7									
		GND					V10									
		GND					V12									
		GND					V14									
		GND					V18									
		GND					V20									
		GND					V14									
		GND					W13									
		GND					W15									
		GND					W17									
		GND					W19									
		GND					W21									
		GND					X10									
		GND					Y12									
		GND					Y18									
		GND					Y20									

Notes:  
 (1) For more information about pin definitions and pin connection guidelines, refer to the [Arria V Device Family Pin Connection Guidelines](#).  
 (2) GAB, REFCLK pin is not supported in current Quartus II version, but will be supported in future Quartus II release version.  
 (3) Pins with \* contains similar name with other pins in the same column. For the selection of the HPS pins, refer to the "HPS Pin Mux Select x" columns.  
 (4) Pins with ~ are the 10 Gbps transceiver channels. For more information about the 10 Gbps transceiver channels clocking recommendation, refer to the [Transceiver Clocking in Arria V Devices chapter](#).  
 (5) RESET pin is only applicable for DDR3 device.





**Pin Information for the Arria® V 5ASTMD5 Device  
Version 1.3**

<b>Version Number</b>	<b>Date</b>	<b>Changes Made</b>
1.0	4/19/2013	Initial release.
1.1	9/30/2014	Remove corresponding bank number from VCCRSTCLK_HPS pin.
1.2	7/31/2015	Renamed the following columns: - Renamed "DDR3/DDR2 hard memory PHY" to "HMC pin assignment for DDR3". - Renamed "LPDDR2 hard memory PHY" to "HMC pin assignment for LPDDR2".
1.3	12/23/2016	-Renamed SDMMC_FB_CLK_IN to HPS_GPIO44.