Bank Number	VREFB Group	Pin Name / Function *(2)*	Optional Function(s) *(2)*	Configuration Function	F484	DQS for X8/X9 in F484	DQS for X16/X18 in F484	DQS for X32/X36 in F484
QL0		GXB_TX3p			F2			
QL0		GXB_TX3n			F1			
QL0		GXB_RX3p			H2			
QL0		GXB_RX3n			H1			
QL0		GXB_TX2p			K2			
QL0		GXB_TX2n			K1			
QL0		GXB_RX2p			M2			
QL0		GXB_RX2n			M1			
QL0		GXB_TX1p			P2			
QL0		GXB_TX1n			P1			
QL0		GXB_RX1p			T2			
QL0		GXB_RX1n			T1			
QL0		GXB_TX0p			V2			
QL0		GXB_TX0n			V1			
QL0		GXB_RX0p			Y2			
QL0		GXB_RX0n			Y1			
B3		MSEL3		MSEL3	P4			
B3		MSEL2		MSEL2	R5			
B3		MSEL1		MSEL1	P5			
B3		MSEL0		MSEL0	T6			
B3		CONF_DONE		CONF_DONE	U5			
B3		nSTATUS		nSTATUS	R8			
B3B	VREFB3N2	REFCLK0p	DIFFCLK_0p,CLKIO20		M7			
B3B	VREFB3N2	REFCLK0n	DIFFCLK_0n		N7			
B3B	VREFB3N2	REFCLK1p	DIFFCLK_1p,CLKIO22		M8			
B3B	VREFB3N2	REFCLK1n	DIFFCLK_1n		N8			
B3	VREFB3N2	IO	PLL1_CLKOUTp		T7			
B3	VREFB3N2	IO	PLL1_CLKOUTn		T8			
B3	VREFB3N2	IO	PLL5_CLKOUTp		U6			
B3	VREFB3N2	IO	PLL5_CLKOUTn		V6			
B3	VREFB3N2	IO	PLL6_CLKOUTp		U7			
B3	VREFB3N2	IO	PLL6_CLKOUTn		V7			
B3	VREFB3N2	IO		INIT_DONE	W8			
B3	VREFB3N2	IO	DIFFIO_B1p	DATA5	W4			
B3	VREFB3N2	IO	DIFFIO_B1n	DATA6	Y4			
B3	VREFB3N2	IO	DIFFIO_B2p	DATA7	R9			
B3	VREFB3N2	IO	DIFFIO_B2n		T9			
B3	VREFB3N2	IO	DIFFIO_B3p	CRC_ERROR	AA4			
B3	VREFB3N2	IO	DIFFIO_B3n	NCEO	AB3			
B3	VREFB3N2	IO	DIFFIO_B4p		P10			
B3	VREFB3N2	IO	DIFFIO_B4n		R10			
B3	VREFB3N2	IO	DIFFIO_B5p		W5	DM3B/BWS#3B	DM3B/BWS#3B	DM5B/BWS#5B
B3	VREFB3N2	IO	DIFFIO_B5n		Y5	DQ3B	DQ3B	DQ5B
B3	VREFB3N2	IO	VREFB3N2		V9			
B3	VREFB3N2	IO	DIFFIO_B6p		R11	DQS1B/CQ1B#, DPCLK0	DQS1B/CQ1B#, DPCLK0	DQS1B/CQ1B#, DPCLK0
B3	VREFB3N2	IO	DIFFIO_B6n		T11	DQ3B	DQ3B	DQ5B
B3	VREFB3N2	IO	DIFFIO_B7p		W6	DQ3B	DQ3B	DQ5B
B3	VREFB3N2	IO	DIFFIO_B7n		Y6	DQ3B	DQ3B	DQ5B
B3	VREFB3N2	IO	DIFFIO_B8p		W7	DQ3B	DQ3B	DQ5B
B3	VREFB3N2	IO	DIFFIO_B8n		Y7	DQ3B	DQ3B	DQ5B
B3	VREFB3N1	IO	DIFFIO_B9p		AB4	DQ3B	DQ3B	DQ5B

Bank Number	VREFB Group	Pin Name / Function *(2)*	Optional Function(s) *(2)*	Configuration Function	F484	DQS for X8/X9 in F484	DQS for X16/X18 in F484	DQS for X32/X36 in F484
B3	VREFB3N1	IO	DIFFIO_B9n		AB5	DQ3B	DQ3B	DQ5B
B3	VREFB3N1	IO	DIFFIO_B10p		AA6	DQ3B	DQ3B	DQ5B
B3	VREFB3N1	IO	DIFFIO_B10n		AB6	DM5B/BWS#5B	DM3B/BWS#3B	DM5B/BWS#5B
B3	VREFB3N1	IO	DIFFIO_B11p		AA7			
B3	VREFB3N1	IO	DIFFIO_B11n		AB7			
B3	VREFB3N1	IO	VREFB3N1		W10			
B3	VREFB3N1	IO	DIFFIO_B12p		W9	DQ5B	DQ3B	DQ5B
B3	VREFB3N1	IO	DIFFIO_B12n		Y8	DQS3B/CQ3B#, DPCLK1	DQS3B/CQ3B#, DPCLK1	DQS3B/CQ3B#, DPCLK1
B3	VREFB3N1	IO	DIFFIO_B13p		Y9	DQ5B	DQ3B	DQ5B
B3	VREFB3N1	IO	DIFFIO_B13n		AA9	DQ5B	DQ3B	DQ5B
B3	VREFB3N1	IO	DIFFIO_B14p		AB8	DQ5B	DQ3B	DQ5B
B3	VREFB3N1	IO	DIFFIO_B14n		AB9			
B3	VREFB3N0	IO	DIFFIO_B15p		W11	DQ5B	DQ3B	DQ5B
B3	VREFB3N0	IO	DIFFIO_B15n		Y11	DQ5B	DQ3B	DQ5B
B3	VREFB3N0	IO	DIFFIO_B16p		Y10	DQS5B/CQ5B#, DPCLK2	DQS5B/CQ5B#, DPCLK2	DQS5B/CQ5B#, DPCLK2
B3	VREFB3N0	IO	DIFFIO_B16n		AA10	DQ5B	DQ3B	DQ5B
B3	VREFB3N0	IO	VREFB3N0		U12			
B3	VREFB3N0	IO	DIFFIO_B17p		W12	DQ5B	DQ3B	DQ5B
B3	VREFB3N0	IO	DIFFIO_B17n		Y12	DQ5B	DQ3B	DQ5B
B3	VREFB3N0	IO	DIFFIO_B18p		AB10	DM4B	DM5B/BWS#5B	DM5B/BWS#5B
B3	VREFB3N0	IO	DIFFIO_B18n		AB11		DQ5B	DQ5B
B3A	VREFB3N0	CLKIO12	DIFFCLK_7p,REFCLK2p		M11			
B3A	VREFB3N0	CLKIO13	DIFFCLK_7n,REFCLK2n		N11			
B4	VREFB4N2	CLKIO14	DIFFCLK_6p		AA12			
B4	VREFB4N2	CLKIO15	DIFFCLK_6n		AB12			
B4	VREFB4N2	IO	DIFFIO_B19p		R13	DQ4B	DQ5B	DQ5B
B4	VREFB4N2	IO	DIFFIO_B19n		T13	DQS4B/CQ5B, DPCLK3	DQS4B/CQ5B, DPCLK3	DQS4B/CQ5B, DPCLK3
B4	VREFB4N2	IO	DIFFIO_B20p		W13	DQ4B	DQ5B	DQ5B
B4	VREFB4N2	IO	DIFFIO_B20n		Y13	DQ4B	DQ5B	DQ5B
B4	VREFB4N2	IO	DIFFIO_B21p		AA13			
B4	VREFB4N2	IO	DIFFIO_B21n		AB13			
B4	VREFB4N2	IO	VREFB4N2		V13			
B4	VREFB4N2	IO	DIFFIO_B22p		AB14	DQ4B	DQ5B	DQ5B
B4	VREFB4N2	IO	DIFFIO_B22n		AB15	DQ4B	DQ5B	DQ5B
B4	VREFB4N2	IO	DIFFIO_B23p		W14	DQ4B	DQ5B	DQ5B
B4	VREFB4N2	IO	DIFFIO_B23n		Y14	DQ4B	DQ5B	DQ5B
B4	VREFB4N2	IO	DIFFIO_B24p		R14			
B4	VREFB4N2	IO	DIFFIO_B24n		T14			
B4	VREFB4N1	IO	DIFFIO_B25p		W15	DQ4B	DQ5B	DQ5B
B4	VREFB4N1	IO	DIFFIO_B25n		Y15	DM2B	DM5B/BWS#5B	DM5B/BWS#5B
B4	VREFB4N1	IO	DIFFIO_B26p		U14			
B4	VREFB4N1	IO	DIFFIO_B26n		U15	DQ2B	DQ5B	DQ5B
B4	VREFB4N1	IO	VREFB4N1		W16			
B4	VREFB4N1	IO	DIFFIO_B27p		AA15	DQS2B/CQ3B, DPCLK4	DQS2B/CQ3B, DPCLK4	DQS2B/CQ3B, DPCLK4
B4	VREFB4N1	IO	DIFFIO_B27n		AB16			
B4	VREFB4N1	IO	DIFFIO_B28p		Y16	DQ2B	DQ5B	DQ5B
B4	VREFB4N1	IO	DIFFIO_B28n		AA16	DQ2B	DQ5B	DQ5B
B4	VREFB4N1	IO	DIFFIO_B29p		AB17			
B4	VREFB4N1	IO	DIFFIO_B29n		AB18	DQ2B	DQ5B	DQ5B
B4	VREFB4N1	IO	DIFFIO_B30p		W17	DQ2B	DQ5B	DQ5B
B4	VREFB4N1	IO	DIFFIO_B30n		Y17			

Bank Number	VREFB Group	Pin Name / Function *(2)*	Optional Function(s) *(2)*	Configuration Function	F484	DQS for X8/X9 in F484	DQS for X16/X18 in F484	DQS for X32/X36 in F484
B4	VREFB4N1	IO	DIFFIO_B31p		Y18	DQ2B	DQ5B	DQ5B
B4	VREFB4N1	IO	DIFFIO_B31n		AA18	DQ2B	DQ5B	DQ5B
B4	VREFB4N0	IO	DIFFIO_B32p		R15			
B4	VREFB4N0	IO	DIFFIO_B32n		T15			
B4	VREFB4N0	IO	DIFFIO_B33p		AA19			
B4	VREFB4N0	IO	DIFFIO_B33n		AB19			
B4	VREFB4N0	IO	VREFB4N0		T16			
B4	VREFB4N0	IO	DIFFIO_B34p		AA20			
B4	VREFB4N0	IO	DIFFIO_B34n		AB20	DQS0B/CQ1B, DPCLK5	DQS0B/CQ1B, DPCLK5	DQS0B/CQ1B, DPCLK5
B4	VREFB4N0	IO	DIFFIO_B35p		AA21			
B4	VREFB4N0	IO	DIFFIO_B35n		AB21		DQ5B	DQ5B
B4	VREFB4N0	IO	DIFFIO_B36p		W18			
B4	VREFB4N0	IO	DIFFIO_B36n		Y19	DQ2B	DQ5B	DQ5B
B4	VREFB4N0	IO	PLL3_CLKOUTp		AA22			
B4	VREFB4N0	IO	PLL3_CLKOUTn		AB22			
B4	VREFB4N0	IO	RUP2		W19			
B4	VREFB4N0	IO	RDN2		Y20			
B5	VREFB5N2	IO	RUP3		T17			
B5	VREFB5N2	IO	RDN3		T18			
B5	VREFB5N2	IO	DIFFIO_R49n		R17	DM3R/BWS#3R	DM3R/BWS#3R	DM1R/BWS#1R
B5	VREFB5N2	IO	DIFFIO_R49p		R16	DQS5R/CQ5R#, DPCLK6	DQS5R/CQ5R#, DPCLK6	DQS5R/CQ5R#, DPCLK6
B5	VREFB5N2	IO	VREFB5N2		U18			
B5	VREFB5N2	IO	DIFFIO_R47n		W22	DQ3R	DQ3R	DQ1R
B5	VREFB5N2	IO	DIFFIO_R47p		Y22	DQ3R	DQ3R	DQ1R
B5	VREFB5N2	IO	DIFFIO_R46n		N15			
B5	VREFB5N2	IO	DIFFIO_R46p		P15			
B5	VREFB5N2	IO	DIFFIO_R45n		W21	DQ3R	DQ3R	DQ1R
B5	VREFB5N2	IO	DIFFIO_R45p		W20	DQ3R	DQ3R	DQ1R
B5	VREFB5N2	IO	DIFFIO_R44n	DEV_OE	P14			
B5	VREFB5N2	IO	DIFFIO_R44p	DEV_CLRn	P13			
B5	VREFB5N2	IO	DIFFIO_R43n		V21	DQ3R	DQ3R	DQ1R
B5	VREFB5N2	IO	DIFFIO_R43p		V20	DQ3R	DQ3R	DQ1R
B5	VREFB5N1	IO	DIFFIO_R42n		U20	DQ3R	DQ3R	DQ1R
B5	VREFB5N1	IO	DIFFIO_R42p		T19			
B5	VREFB5N1	IO	DIFFIO_R41n		T20	DQ3R	DQ3R	DQ1R
B5	VREFB5N1	IO	DIFFIO_R41p		R19	DQ3R	DQ3R	DQ1R
B5	VREFB5N1	IO	DIFFIO_R40n		U22			
B5	VREFB5N1	IO	DIFFIO_R40p		V22	DQS3R/CQ3R#, DPCLK7	DQS3R/CQ3R#, DPCLK7	DQS3R/CQ3R#, DPCLK7
B5	VREFB5N1	IO	DIFFIO_R39n		R21			
B5	VREFB5N1	IO	DIFFIO_R39p		R20	DM1R/BWS#1R	DM3R/BWS#3R	DM1R/BWS#1R
B5	VREFB5N1	IO	DIFFIO_R38n		T22			
B5	VREFB5N1	IO	DIFFIO_R38p		T21	DQ1R	DQ3R	DQ1R
B5	VREFB5N1	IO	VREFB5N1		P20			
B5	VREFB5N1	IO	DIFFIO_R36n		M15			
B5	VREFB5N1	IO	DIFFIO_R36p		N14			
B5	VREFB5N1	IO	DIFFIO_R35n		M14			
B5	VREFB5N1	IO	DIFFIO_R35p		N13			
B5	VREFB5N1	IO	DIFFIO_R34n		L15	DQ1R	DQ3R	DQ1R
B5	VREFB5N1	IO	DIFFIO_R34p		L14			
B5	VREFB5N0	IO	DIFFIO_R33n		P22	DQ1R	DQ3R	DQ1R
B5	VREFB5N0	IO	DIFFIO_R33p		R22			

Bank Number	VREFB Group	Pin Name / Function *(2)*	Optional Function(s) *(2)*	Configuration Function	F484	DQS for X8/X9 in F484	DQS for X16/X18 in F484	DQS for X32/X36 in F484
B5	VREFB5N0	IO	DIFFIO_R32n		M17			
B5	VREFB5N0	IO	DIFFIO_R32p		N17	DQ1R	DQ3R	DQ1R
B5	VREFB5N0	IO	DIFFIO_R31n		L13			
B5	VREFB5N0	IO	DIFFIO_R31p		M13	DQ1R	DQ3R	DQ1R
B5	VREFB5N0	IO	DIFFIO_R30n		N20			
B5	VREFB5N0	IO	DIFFIO_R30p		N19	DQS1R/CQ1R#, DPCLK8	DQS1R/CQ1R#, DPCLK8	DQS1R/CQ1R#, DPCLK8
B5	VREFB5N0	IO	DIFFIO_R29n		N22	DQ1R	DQ3R	DQ1R
B5	VREFB5N0	IO	DIFFIO_R29p		N21	DQ1R	DQ3R	DQ1R
B5	VREFB5N0	IO	VREFB5N0		M20			
B5	VREFB5N0	IO	DIFFIO_R27n		L16			
B5	VREFB5N0	IO	DIFFIO_R27p		M16			
B5	VREFB5N0	IO	DIFFIO_R26n		M19	DQ1R	DQ3R	DQ1R
B5	VREFB5N0	IO	DIFFIO_R26p		M18	DQ1R	DQ3R	DQ1R
B5	VREFB5N0	CLKIO4	DIFFCLK_2n		M22			
B5	VREFB5N0	CLKIO5	DIFFCLK_2p		M21			
B6	VREFB6N2	CLKIO6	DIFFCLK_3n		L22			
B6	VREFB6N2	CLKIO7	DIFFCLK_3p		L21			
B6	VREFB6N2	IO	DIFFIO_R25n		L20	DM0R	DM1R/BWS#1R	DM1R/BWS#1R
B6	VREFB6N2	IO	DIFFIO_R25p		L19	DQ0R	DQ1R	DQ1R
B6	VREFB6N2	IO	VREFB6N2		J15			
B6	VREFB6N2	IO	DIFFIO_R23n		J20	DQ0R	DQ1R	DQ1R
B6	VREFB6N2	IO	DIFFIO_R23p		J19	DQ0R	DQ1R	DQ1R
B6	VREFB6N2	IO	DIFFIO_R22n		H22	DQS0R/CQ1R, DPCLK9	DQS0R/CQ1R, DPCLK9	DQS0R/CQ1R, DPCLK9
B6	VREFB6N2	IO	DIFFIO_R22p		J21			
B6	VREFB6N2	IO	DIFFIO_R21n		J22			
B6	VREFB6N2	IO	DIFFIO_R21p		K22	DQ0R	DQ1R	DQ1R
B6	VREFB6N2	IO	DIFFIO_R20n		K20			
B6	VREFB6N2	IO	DIFFIO_R20p		K19	DQ0R	DQ1R	DQ1R
B6	VREFB6N2	IO	DIFFIO_R19n		H21			
B6	VREFB6N2	IO	DIFFIO_R19p		H20	DQ0R	DQ1R	DQ1R
B6	VREFB6N2	IO	DIFFIO_R18n		G21			
B6	VREFB6N2	IO	DIFFIO_R18p		G20	DQ0R	DQ1R	DQ1R
B6	VREFB6N1	IO	DIFFIO_R17n		E20			
B6	VREFB6N1	IO	DIFFIO_R17p		F20			
B6	VREFB6N1	IO	DIFFIO_R16n		F22	DQ0R	DQ1R	DQ1R
B6	VREFB6N1	IO	DIFFIO_R16p		G22			
B6	VREFB6N1	IO	DIFFIO_R15n		E22			
B6	VREFB6N1	IO	DIFFIO_R15p		E21		DQ1R	DQ1R
B6	VREFB6N1	IO	DIFFIO_R14n		D22			
B6	VREFB6N1	IO	DIFFIO_R14p		D21	DM2R	DM1R/BWS#1R	DM1R/BWS#1R
B6	VREFB6N1	IO	VREFB6N1		H17			
B6	VREFB6N1	IO	DIFFIO_R12n		B22			
B6	VREFB6N1	IO	DIFFIO_R12p		C22		DQ1R	DQ1R
B6	VREFB6N1	IO	DIFFIO_R11n		A22			
B6	VREFB6N1	IO	DIFFIO_R11p		A21	DQ2R	DQ1R	DQ1R
B6	VREFB6N1	IO	DIFFIO_R10n		D20			
B6	VREFB6N1	IO	DIFFIO_R10p		D19	DQ2R	DQ1R	DQ1R
B6	VREFB6N1	IO	DIFFIO_R9n		B21	DQS2R/CQ3R, DPCLK10	DQS2R/CQ3R, DPCLK10	DQS2R/CQ3R, DPCLK10
B6	VREFB6N1	IO	DIFFIO_R9p		B20	DQ2R	DQ1R	DQ1R
B6	VREFB6N1	IO	DIFFIO_R8n		C20			
B6	VREFB6N1	IO	DIFFIO_R8p		C19	DQ2R	DQ1R	DQ1R

Bank Number	VREFB Group	Pin Name / Function *(2)*	Optional Function(s) *(2)*	Configuration Function	F484	DQS for X8/X9 in F484	DQS for X16/X18 in F484	DQS for X32/X36 in F484
B6	VREFB6N1	IO	DIFFIO_R7n		A20			
B6	VREFB6N1	IO	DIFFIO_R7p		B19	DQ2R	DQ1R	DQ1R
B6	VREFB6N0	IO	DIFFIO_R6n		K17			
B6	VREFB6N0	IO	DIFFIO_R6p		J16			
B6	VREFB6N0	IO	VREFB6N0		G18			
B6	VREFB6N0	IO	DIFFIO_R4n		K14			
B6	VREFB6N0	IO	DIFFIO_R4p		K13			
B6	VREFB6N0	IO	DIFFIO_R3n		H16			
B6	VREFB6N0	IO	DIFFIO_R3p		H15			
B6	VREFB6N0	IO	DIFFIO_R2n		G17	DQ2R	DQ1R	DQ1R
B6	VREFB6N0	IO	DIFFIO_R2p		G16	DQS4R/CQ5R, DPCLK11	DQS4R/CQ5R, DPCLK11	DQS4R/CQ5R, DPCLK11
B6	VREFB6N0	IO	DIFFIO_R1n		G19	DQ2R	DQ1R	DQ1R
B6	VREFB6N0	IO	DIFFIO_R1p		F18	DQ2R	DQ1R	DQ1R
B7	VREFB7N0	IO	RUP4		F16			
B7	VREFB7N0	IO	RDN4		F17			
B7	VREFB7N0	IO	PLL4_CLKOUTn		C17			
B7	VREFB7N0	IO	PLL4_CLKOUTp		C18			
B7	VREFB7N0	IO			B18			
B7	VREFB7N0	IO	DIFFIO_T37n		A18	DQ2T	DQ5T	DQ5T
B7	VREFB7N0	IO	DIFFIO_T37p		A19	DQ2T	DQ5T	DQ5T
B7	VREFB7N0	IO	DIFFIO_T36n		D17			
B7	VREFB7N0	IO	DIFFIO_T36p		E17			
B7	VREFB7N0	IO	VREFB7N0		D16			
B7	VREFB7N0	IO	DIFFIO_T35n		B16	DQS0T/CQ1T, DPCLK12	DQS0T/CQ1T, DPCLK12	DQS0T/CQ1T, DPCLK12
B7	VREFB7N0	IO	DIFFIO_T35p		C16	DQ2T	DQ5T	DQ5T
B7	VREFB7N0	IO	DIFFIO_T34n		A16	DQ2T	DQ5T	DQ5T
B7	VREFB7N0	IO	DIFFIO_T34p		A17			
B7	VREFB7N0	IO	DIFFIO_T33n		C15	DQ2T	DQ5T	DQ5T
B7	VREFB7N0	IO	DIFFIO_T33p		D15			
B7	VREFB7N1	IO	DIFFIO_T32n		A15	DQ2T	DQ5T	DQ5T
B7	VREFB7N1	IO	DIFFIO_T32p		B15	DQ2T	DQ5T	DQ5T
B7	VREFB7N1	IO	DIFFIO_T31n		C14			
B7	VREFB7N1	IO	DIFFIO_T31p		D14	DQ2T	DQ5T	DQ5T
B7	VREFB7N1	IO	DIFFIO_T30n		A13			
B7	VREFB7N1	IO	DIFFIO_T30p		A14		DQ5T	DQ5T
B7	VREFB7N1	IO	VREFB7N1		D13			
B7	VREFB7N1	IO	DIFFIO_T29n		C12	DM2T	DM5T/BWS#5T	DM5T/BWS#5T
B7	VREFB7N1	IO	DIFFIO_T29p		C13			
B7	VREFB7N1	IO	DIFFIO_T28n		B12	DQ4T	DQ5T	DQ5T
B7	VREFB7N1	IO	DIFFIO_T28p		B13	DQ4T	DQ5T	DQ5T
B7	VREFB7N1	IO	DIFFIO_T27n		G14			
B7	VREFB7N1	IO	DIFFIO_T27p		G15	DQS2T/CQ3T, DPCLK13	DQS2T/CQ3T, DPCLK13	DQS2T/CQ3T, DPCLK13
B7	VREFB7N1	IO	DIFFIO_T26n		H14			
B7	VREFB7N1	IO	DIFFIO_T26p		J14	DQ4T	DQ5T	DQ5T
B7	VREFB7N2	IO	DIFFIO_T25n		J12			
B7	VREFB7N2	IO	DIFFIO_T25p		K12			
B7	VREFB7N2	IO	DIFFIO_T24n		C10	DQ4T	DQ5T	DQ5T
B7	VREFB7N2	IO	DIFFIO_T24p		C11			
B7	VREFB7N2	IO	VREFB7N2		F12			
B7	VREFB7N2	IO	DIFFIO_T23n		H13	DQ4T	DQ5T	DQ5T
B7	VREFB7N2	IO	DIFFIO_T23p		J13	DQ4T	DQ5T	DQ5T

Bank Number	VREFB Group	Pin Name / Function *(2)*	Optional Function(s) *(2)*	Configuration Function	F484	DQS for X8/X9 in F484	DQS for X16/X18 in F484	DQS for X32/X36 in F484
B7	VREFB7N2	IO	DIFFIO_T22n		A11	DQ4T	DQ5T	DQ5T
B7	VREFB7N2	IO	DIFFIO_T22p		A12			
B7	VREFB7N2	IO	DIFFIO_T21n		A10	DQ4T	DQ5T	DQ5T
B7	VREFB7N2	IO	DIFFIO_T21p		B10	DQS4T/CQ5T, DPCLK14	DQS4T/CQ5T, DPCLK14	DQS4T/CQ5T, DPCLK14
B7	VREFB7N2	IO	DIFFIO_T20n		G12		DQ5T	DQ5T
B7	VREFB7N2	IO	DIFFIO_T20p		H12	DM4T	DM5T/BWS#5T	DM5T/BWS#5T
B7	VREFB7N2	CLKIO8	DIFFCLK_5n		A9			
B7	VREFB7N2	CLKIO9	DIFFCLK_5p		B9			
B8A	VREFB8N0	CLKIO10	DIFFCLK_4n,REFCLK3n		J10			
B8A	VREFB8N0	CLKIO11	DIFFCLK_4p,REFCLK3p		K10			
B8	VREFB8N0	IO	DIFFIO_T19n		A8	DQS5T/CQ5T#, DPCLK15	DQS5T/CQ5T#, DPCLK15	DQS5T/CQ5T#, DPCLK15
B8	VREFB8N0	IO	DIFFIO_T19p		B7	DQ5T	DQ3T	DQ5T
B8	VREFB8N0	IO	DIFFIO_T18n		A6			
B8	VREFB8N0	IO	DIFFIO_T18p		A7	DQ5T	DQ3T	DQ5T
B8	VREFB8N0	IO	DIFFIO_T17n		A4	DQ5T	DQ3T	DQ5T
B8	VREFB8N0	IO	DIFFIO_T17p		A5			
B8	VREFB8N0	IO	VREFB8N0		D12			
B8	VREFB8N0	IO	DIFFIO_T16n		A2	DQ5T	DQ3T	DQ5T
B8	VREFB8N0	IO	DIFFIO_T16p		A3	DQ5T	DQ3T	DQ5T
B8	VREFB8N0	IO	DIFFIO_T15n		B3	DQ5T	DQ3T	DQ5T
B8	VREFB8N0	IO	DIFFIO_T15p		B4			
B8	VREFB8N0	IO	DIFFIO_T14n		B6	DQ5T	DQ3T	DQ5T
B8	VREFB8N0	IO	DIFFIO_T14p		C6	DQ5T	DQ3T	DQ5T
B8	VREFB8N1	IO	DIFFIO_T13n		A1			
B8	VREFB8N1	IO	DIFFIO_T13p		B1	DQ5T	DQ3T	DQ5T
B8	VREFB8N1	IO	DIFFIO_T12n		C8			
B8	VREFB8N1	IO	DIFFIO_T12p		D8			
B8	VREFB8N1	IO	VREFB8N1		D11			
B8	VREFB8N1	IO	DIFFIO_T11n		C1	DM5T/BWS#5T	DM3T/BWS#3T	DM5T/BWS#5T
B8	VREFB8N1	IO	DIFFIO_T11p		C2			
B8	VREFB8N1	IO	DIFFIO_T10n		C7	DQS3T/CQ3T#, DPCLK16	DQS3T/CQ3T#, DPCLK16	DQS3T/CQ3T#, DPCLK16
B8	VREFB8N1	IO	DIFFIO_T10p		D7	DQ3T	DQ3T	DQ5T
B8	VREFB8N1	IO	DIFFIO_T9n		C3			
B8	VREFB8N1	IO	DIFFIO_T9p		C4	DQ3T	DQ3T	DQ5T
B8	VREFB8N1	IO	DIFFIO_T8n		E8	DQ3T	DQ3T	DQ5T
B8	VREFB8N1	IO	DIFFIO_T8p		F8			
B8	VREFB8N2	IO	DIFFIO_T7n		C5	DQ3T	DQ3T	DQ5T
B8	VREFB8N2	IO	DIFFIO_T7p		D4			
B8	VREFB8N2	IO	DIFFIO_T6n		D5	DQ3T	DQ3T	DQ5T
B8	VREFB8N2	IO	DIFFIO_T6p		E5	DQS1T/CQ1T#, DPCLK17	DQS1T/CQ1T#, DPCLK17	DQS1T/CQ1T#, DPCLK17
B8	VREFB8N2	IO	VREFB8N2		D10			
B8	VREFB8N2	IO	DIFFIO_T5n		C9	DQ3T	DQ3T	DQ5T
B8	VREFB8N2	IO	DIFFIO_T5p		D9	DQ3T	DQ3T	DQ5T
B8	VREFB8N2	IO	DIFFIO_T4n		D6	DQ3T	DQ3T	DQ5T
B8	VREFB8N2	IO	DIFFIO_T4p		E6	DQ3T	DQ3T	DQ5T
B8	VREFB8N2	IO	DIFFIO_T3n		G7			
B8	VREFB8N2	IO	DIFFIO_T3p		H7			
B8	VREFB8N2	IO	DIFFIO_T2n	DATA4	F6	DM3T/BWS#3T	DM3T/BWS#3T	DM5T/BWS#5T
B8	VREFB8N2	IO	DIFFIO_T2p	DATA3	G6			
B8	VREFB8N2	IO	DIFFIO_T1n	DATA2	G8			
B8	VREFB8N2	IO	DIFFIO_T1p		H8			

Bank Number	VREFB Group	Pin Name / Function *(2)*	Optional Function(s) *(2)*	Configuration Function	F484	DQS for X8/X9 in F484	DQS for X16/X18 in F484	DQS for X32/X36 in F484
B8	VREFB8N2	IO	PLL2_CLKOUTn		G10			
B8	VREFB8N2	IO	PLL2_CLKOUTp		H9			
B8	VREFB8N2	IO		CLKUSR	G11			
B9	VREFB8N2	IO		DATA0	K4			
B9	VREFB8N2	IO		DATA1, ASDO	D1			
B9	VREFB8N2	IO		NCSO	J4			
B9		DCLK		DCLK	D3			
B9		nCONFIG		nCONFIG	H4			
B9		nCE		nCE	D2			
B9		TDI		TDI	F5			
B9		TCK		TCK	E4			
B9		TMS		TMS	G5			
B9		TDO		TDO	E3			
		GND			F3			
		GND			M3			
		GND			T4			
		GND			U3			
		GND			V19			
		GND			E19			
		GND			H5			
		GND			AA11			
		GND			AA14			
		GND			AA17			
		GND			AA5			
		GND			AA8			
		GND			B11			
		GND			B14			
		GND			B17			
		GND			B2			
		GND			B5			
		GND			B8			
		GND			C21			
		GND			D18			
		GND			E7			
		GND			F11			
		GND			F13			
		GND			F15			
		GND			F21			
		GND			F9			
		GND			H11			
		GND			H18			
		GND			J6			
		GND			J8			
		GND			K11			
		GND			K15			
		GND			K21			
		GND			K5			
		GND			K7			
		GND			K9			
		GND			L10			
		GND			L12			

Bank Number	VREFB Group	Pin Name / Function *(2)*	Optional Function(s) *(2)*	Configuration Function	F484	DQS for X8/X9 in F484	DQS for X16/X18 in F484	DQS for X32/X36 in F484
		GND			L18			
		GND			L6			
		GND			L8			
		GND			M5			
		GND			M9			
		GND			N10			
		GND			N4			
		GND			N6			
		GND			P11			
		GND			P16			
		GND			P18			
		GND			P21			
		GND			P9			
		GND			R12			
		GND			R6			
		GND			U10			
		GND			U17			
		GND			U21			
		GND			V11			
		GND			V14			
		GND			V5			
		GND			V8			
		GND			Y21			
		GND			AA1			
		GND			AA2			
		GND			AB2			
		GND			E1			
		GND			E2			
		GND			G1			
		GND			G2			
		GND			J1			
		GND			J2			
		GND			L1			
		GND			L2			
		GND			N1			
		GND			N2			
		GND			R1			
		GND			R2			
		GND			U1			
		GND			U2			
		GND			W1			
		GND			W2			
		VCC_CLKIN3A			N12			
		VCC_CLKIN3B			P7			
		VCC_CLKIN8A			H10			
		VCCD_PLL			G3			
		VCCD_PLL			M4			
		VCCD_PLL			R4			
		VCCD_PLL			U4			
		VCCD_PLL			V18			
		VCCD_PLL			E18			

Bank Number	VREFB Group	Pin Name / Function *(2)*	Optional Function(s) *(2)*	Configuration Function	F484	DQS for X8/X9 in F484	DQS for X16/X18 in F484	DQS for X32/X36 in F484
		VCCINT			J5			
		VCCINT			F7			
		VCCINT			G13			
		VCCINT			G9			
		VCCINT			H6			
		VCCINT			J11			
		VCCINT			J17			
		VCCINT			J7			
		VCCINT			J9			
		VCCINT			K16			
		VCCINT			K6			
		VCCINT			K8			
		VCCINT			L11			
		VCCINT			L17			
		VCCINT			L5			
		VCCINT			L7			
		VCCINT			L9			
		VCCINT			M10			
		VCCINT			M12			
		VCCINT			M6			
		VCCINT			N16			
		VCCINT			N5			
		VCCINT			N9			
		VCCINT			P12			
		VCCINT			P17			
		VCCINT			P6			
		VCCINT			P8			
		VCCINT			R7			
		VCCINT			T10			
		VCCINT			T12			
		VCCINT			U16			
		VCCIO3			U11			
		VCCIO3			U8			
		VCCIO3			U9			
		VCCIO3			V10			
		VCCIO3			V12			
		VCCIO4			U13			
		VCCIO4			V15			
		VCCIO4			V16			
		VCCIO4			V17			
		VCCIO5			N18			
		VCCIO5			P19			
		VCCIO5			R18			
		VCCIO6			H19			
		VCCIO6			J18			
		VCCIO6			K18			
		VCCIO7			E13			
		VCCIO7			E14			
		VCCIO7			E15			
		VCCIO7			E16			
		VCCIO7			F14			

Bank Number	VREFB Group	Pin Name / Function *(2)*	Optional Function(s) *(2)*	Configuration Function	F484	DQS for X8/X9 in F484	DQS for X16/X18 in F484	DQS for X32/X36 in F484
		VCCIO8			E10			
		VCCIO8			E11			
		VCCIO8			E12			
		VCCIO8			E9			
		VCCIO8			F10			
		VCCIO9			G4			
		VCCA			F4			
		VCCA			L4			
		VCCA			T5			
		VCCA			V4			
		VCCA			U19			
		VCCA			F19			
		NC			Y3			
		NC			AA3			
		VCCL_GXB			V3			
		VCCL_GXB			K3			
		VCCL_GXB			L3			
		VCCL_GXB			N3			
		VCCL_GXB			T3			
		VCCH_GXB			H3			
		VCCH_GXB			P3			
		RREF0			AB1			
		VCCA_GXB			W3			
		VCCA_GXB			J3			
		VCCA_GXB			R3			

Notes:

(1) For DQS pins that do not have the associated DQ pins, the particular DQS is not supported.

(2) For implementation of transceiver applications that run at ≥2.97Gbps data rate, you must refer to the Cyclone IV Device Family Pin Connection Guidelines.

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
	Clock and PLL Pins	
CLK[5, 7, 9, 11, 12,14], DIFFCLK_[2..7]p	Clock, Input	Dedicated global clock input pins that can also be used for the positive terminal inputs for differential global clock input or user input pins.
CLK[4, 6, 8, 10, 13, 15], DIFFCLK_[2..7]n	Clock, Input	Dedicated global clock input pins that can also be used for the negative terminal inputs for differential global clock input or user input pins.
DIFFCLK_[0, 1, 8, 9]p, CLKIO[17, 19, 20, 22]	Clock, Input	Optional positive terminal inputs for differential global clock input or single-ended clock input.
DIFFCLK_[0, 1, 8, 9]n	Clock, Input	Optional negative terminal inputs for differential global clock input.
PLL[1..8]_CLKOUTp	I/O, Output	Optional positive terminal for external clock outputs from PLL [1..8]. These pins can be assigned to single-ended or differential I/O standards if it is being fed by a PLL output.
PLL[1..8]_CLKOUTn	I/O, Output	Optional negative terminal for external clock outputs from PLL [1..8]. These pins can be assigned to single-ended or differential I/O standards if it is being fed by a PLL output.
	Configuration/JTAG Pins	
MSEL[0..3]	Input	Configuration input pins that set the Cyclone IV GX device configuration scheme. The smaller devices like EP4CGX15, EP4CGX22, and EP4CGX30 do not have the MSEL3 pin.
nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled.
nCONFIG	Input	Dedicated configuration control input. Pulling this pin low during user-mode will cause the FPGA to lose its configuration data, enter a reset state, and tri-state all I/O pins. Returning this pin to a logic high level will initiate reconfiguration.
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration status pin. As a status output, the CONF_DONE pin drives low before and during configuration. Once all configuration data is received without error and the initialization cycle starts, CONF_DONE is released. As a status input, CONF_DONE goes high after all data is received. Then the device initializes and enters user mode. It is not available as a user I/O pin.
NCEO	I/O, Output	Output that drives low when device configuration is complete. This pin can be used as a regular I/O if not used for device configuration.
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin. The FPGA drives nSTATUS low immediately after power-up and releases it after POR time. As a status output, the nSTATUS is pulled low if an error occurs during configuration. As a status input, the device enters an error state when nSTATUS is driven low by an external source during configuration or initialization. It is not available as an user I/O pin.
TCK	Input	Dedicated JTAG test clock input pin.
TMS	Input	Dedicated JTAG test mode select input pin.
TDI	Input	Dedicated JTAG test data input pin.
TDO	Output	Dedicated JTAG test data output pin.
NCSO	I/O, Output	Dedicated output control signal from the FPGA to the serial configuration device in AS mode that enables the configuration device.

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
ASDO, DATA1	Input (PS, FPP) Output (AS)	This pin functions as DATA1 in PS and FPP modes, and as ASDO in AS mode. DATA1: Data input in non-AS mode. Byte-wide configuration data is presented to the target device on DATA[0..7]. In PS configuration scheme, DATA1 functions as user I/O pin during configuration, which means it is tri-stated. After FPP configuration, DATA1 is available as a user I/O pin and the state of this pin depends on the Dual- Purpose Pin settings. ASDO: Control signal from the FPGA to the serial configuration device in AS mode used to read out configuration data.
DATA0	I/O, Input	Dual-purpose configuration data input pin. The DATA0 pin can be used for bit-wide configuration or as an I/O pin after configuration is complete.
DATA[2..7]	Input (FPP)	Data inputs. Byte-wide configuration data is presented to the target device on DATA [0..7]. In AS or PS configuration scheme, they function as user I/O pins during configuration, which means they are tri-stated. After FPP configuration, DATA [2..7] are available as user I/O pins and the state of these pins depends on the Dual-Purpose Pin settings.
DCLK	Input (PS) Output (AS)	Dedicated configuration clock pin. In PS configuration, DCLK is used to clock configuration data from an external source into the FPGA. In AS mode, DCLK is an output from the FPGA that provides timing for the configuration interface.
CRC_ERROR	I/O, Output	Active high signal that indicates that the error detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error detection circuit is enabled. This pin can be used as regular I/O if not used for CRC error detection.
DEV_CLRn	I/O (when option off), Input (when option on)	Optional pin that allows designers to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as programmed. This pin is enabled by turning on the Enable device-wide reset (DEV_CLRn) option in the Quartus II software.
DEV_OE	I/O (when option off), Input (when option on)	Optional pin that allows designers to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design. This pin is enabled by turning on the Enable device-wide output enable (DEV_OE) option in the Quartus II software.
INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high at the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration. This pin is enabled by turning on the Enable INIT_DONE output option in the Quartus II software.
CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. If this pin is not enabled for use as a user-supplied configuration clock, it can be used as a user I/O pin. This pin is enabled by turning on the Enable user-supplied start-up clock (CLKUSR) option in the Quartus II software.
Differential I/O Pins		

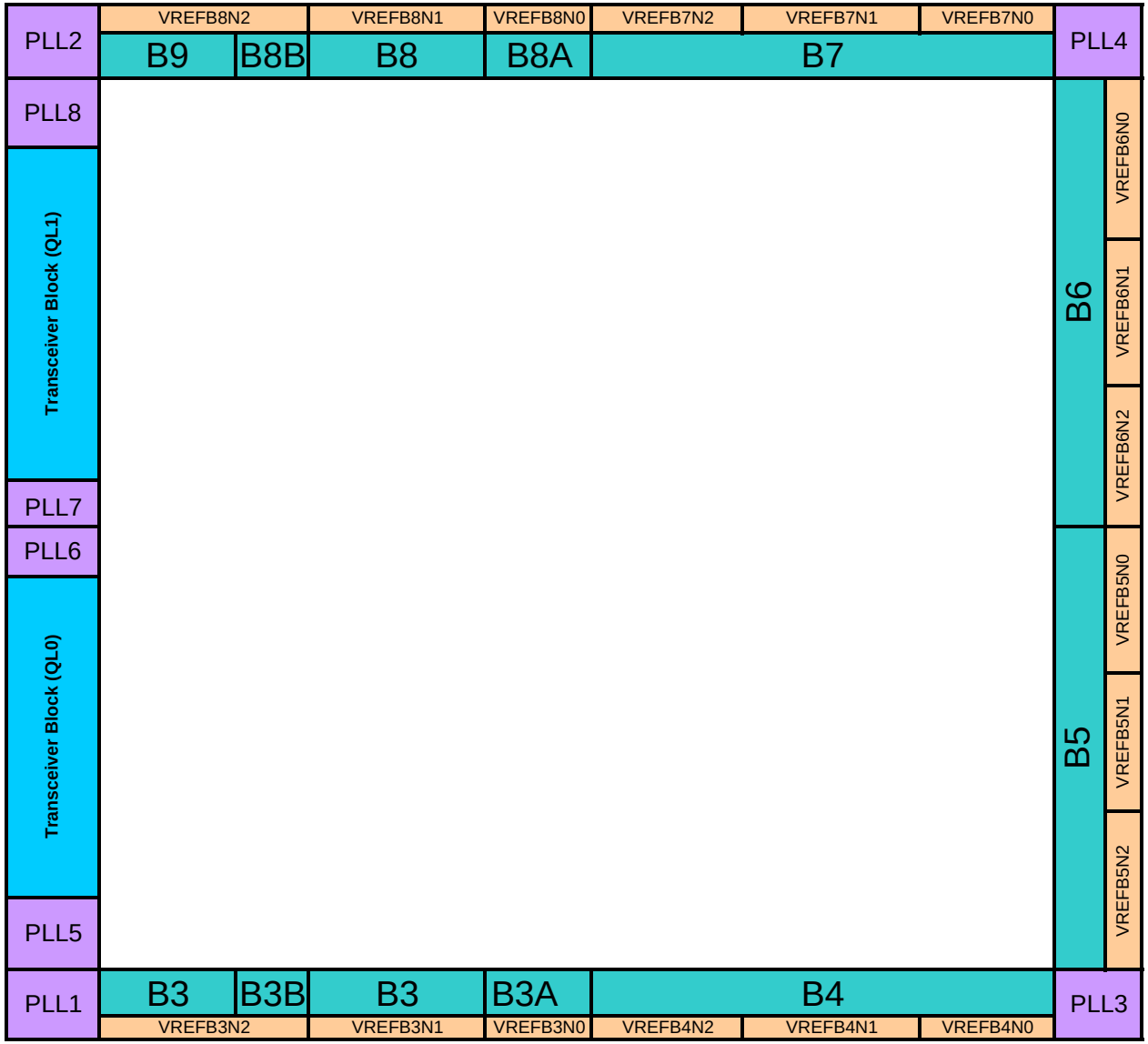
Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
DIFFIO_[R,T,B]0..72][n,p]	I/O, TX/RX channel	Dual-purpose differential transmitter/receiver channels. These channels can be used for transmitting/receiving LVDS compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
External Memory Interface Pins		
DQS[0..5][R,T,B]/CQ[0,1,3,5][R,T,B][#],DPCLK[0..17]	I/O, DQS/CQ, DPCLK	Dual-purpose DPCLK/DQS pins can connect to the global clock network for high-fanout control signals such as clocks, asynchronous clears, presets and clock enables. It can also be used as optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry, which allows fine tune of the phase shift for input clocks or strobes to properly align clock edges needed to capture data.
DQ[0..5][R,T,B]	I/O, DQ	Optional data signal for use in external memory interface.
DM[0..5][R,B,T]/BWS#[0..5][R,T,B]	I/O, DM/BWS#	The data mask pins are only required when writing to DDR SDRAM and DDR2 SDRAM devices. QDR II SRAM devices use the BWS signal to select the byte to be written into memory. A low signal on the DM/BWS# pin indicates that the write is valid. Driving the DM/BWS# pin high results in the memory masking the DQ signals.
Reference Pins		
RUP[2..4]	I/O, Input	Reference pins for on-chip termination (OCT) block in I/O banks 4, 5, and 7. The external precision resistor RUP must be connected to the designated RUP pin within the same bank when used. If the RUP pin is not used, this pin can function as a regular I/O pin.
RDN[2..4]	I/O, Input	Reference pins for on-chip termination (OCT) block in I/O banks 4, 5, and 7. The external precision resistor RDN must be connected to the designated RDN pin within the same bank when used. If the RDN pin is not used, this pin can function as a regular I/O pin.
NC	No Connect	Do not drive signals into these pins.
Supply Pins		
VCCINT	Power	These are internal logic array voltage supply pins.
VCCD_PLL	Power	Digital power for PLLs. The designer must power up these pins, even if the PLL is not used.
VCCA	Power	Analog power for PLLs. All VCCA pins must be powered and all VCCA pins must be powered up and powered down at the same time even if not all the PLLs are used. Designer is advised to keep VCCA isolated from other VCC for better jitter performance.
VCCIO[3..9]	Power	These are I/O supply voltage pins for banks 3 through 9. Each bank can support a different voltage level. VCCIO supplies power to the input and output buffers for all I/O standards.
VCC_CLKIN[3,8]A	Power	CLLKIN power in bank 3A and bank 8A.
VREFB[3..8]N[0..2]	I/O	Input reference voltage for each I/O bank. If a bank uses a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for the bank. If voltage reference I/O standards are not used in the bank, the VREF pins are available as user I/O pins.
GND	Ground	Device ground pins. All GND pins should be connected to GND plane on the board.
Transceiver Pins		
VCCL_GXB	Power	Supplies power to the transceiver PMA TX, PMA RX, and clocking.

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
VCCH_GXB	Power	Supplies power to the transceiver PMA output (TX) buffer.
VCCA_GXB	Power	Supplies power to the transceiver PMA regulator.
GXB_RX[0..7]p	Input	High speed positive differential receiver channels.
GXB_RX[0..7]n	Input	High speed negative differential receiver channels.
GXB_TX[0..7]p	Output	High speed positive differential transmitter channels.
GXB_TX[0..7]n	Output	High speed negative differential transmitter channels.
REFCLK[0..5]p *(2)*	Input	High speed differential reference clock positive.
REFCLK[0..5]n *(2)*	Input	High speed differential reference clock complement.
RREF0	Input	Reference resistor for transceiver.

Notes:

(1) The pin definitions are prepared based on the device with the largest density, EP4CGX150. For the availability of pins in each density, refer to the pin list.

(2) For implementation of transceiver applications that run at ≥2.97Gbps data rate, you must refer to the Cyclone IV Device Family Pin Connection Guidelines.



Notes:

1. This is a top view of the silicon die.
2. This is only a pictorial representation to provide an idea of placement on the device. For exact locations, refer to the pin list and the Quartus® II software.

Version Number	Date	Changes Made
1.0	6/23/2010	Initial release.
1.1	11/8/2010	Added new note in Pin List and Pin Definitions.