Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode (2)	DQ Group for DQS X32/X36 Mode *(2)*
		TDI		TDI			G34				
		TMS		TMS			F34				
		TRST		TRST			C37				
		TCK		TCK			D36				
		TDO		TDO			F35				
1A	VREFB1AN0	PLL_L1_CLKn	PLL_L1_CLKn				C39				
1A	VREFB1AN0	PLL_L1_CLKp	PLL_L1_CLKp				C38				
1A	VREFB1AN0	IO	PLL_L1_CLKOUT0n		DIFFIO_TX_L1n	DIFFOUT_L1n	J33				
1A	VREFB1AN0	IO	PLL_L1_FB_CLKOUT0p		DIFFIO_TX_L1p	DIFFOUT_L1p	K32				
1A	VREFB1AN0	IO	RDN1A		DIFFIO_RX_L1n	DIFFOUT_L2n	G35				
1A	VREFB1AN0	IO	RUP1A		DIFFIO_RX_L1p	DIFFOUT_L2p	H34				
1A	VREFB1AN0	IO			DIFFIO_TX_L2n	DIFFOUT_L3n	J35	DQ1L	DQ1L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_TX_L2p	DIFFOUT_L3p	J34	DQ1L	DQ1L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_RX_L2n	DIFFOUT_L4n	E37	DQSn1L	DQ1L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_RX_L2p	DIFFOUT_L4p	E36	DQS1L	DQ1L/CQn1L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_TX_L3n	DIFFOUT_L5n	K35	DQ1L	DQ1L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_TX_L3p	DIFFOUT_L5p	K34	DQ1L	DQ1L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_RX_L3n	DIFFOUT_L6n	D38	DQSn2L	DQSn1L/DQ1L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_RX_L3p	DIFFOUT_L6p	D37	DQS2L	DQS1L/CQ1L	DQ1L/CQn1L	
1A	VREFB1AN0	IO			DIFFIO_TX_L4n	DIFFOUT_L7n	L34	DQ2L	DQ1L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_TX_L4p	DIFFOUT_L7p	L33	DQ2L	DQ1L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_RX_L4n	DIFFOUT_L8n	F36	DQ2L	DQ1L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_RX_L4p	DIFFOUT_L8p	G36	DQ2L	DQ1L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_TX_L5n	DIFFOUT_L9n	M34	DQ3L	DQ2L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_TX_L5p	DIFFOUT_L9p	M33	DQ3L	DQ2L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_RX_L5n	DIFFOUT_L10n	D39	DQSn3L	DQ2L	DQSn1L/DQ1L	
1A	VREFB1AN0	IO			DIFFIO_RX_L5p	DIFFOUT_L10p	E39	DQS3L	DQ2L/CQn2L	DQS1L/CQ1L	
1A	VREFB1AN0	IO			DIFFIO_TX_L6n	DIFFOUT_L11n	M32	DQ3L	DQ2L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_TX_L6p	DIFFOUT_L11p	N31	DQ3L	DQ2L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_RX_L6n	DIFFOUT_L12n	F39	DQSn4L	DQSn2L/DQ2L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_RX_L6p	DIFFOUT_L12p	F38	DQS4L	DQS2L/CQ2L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_TX_L7n	DIFFOUT_L13n	J37	DQ4L	DQ2L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_TX_L7p	DIFFOUT_L13p	J36	DQ4L	DQ2L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_RX_L7n	DIFFOUT_L14n	H37	DQ4L	DQ2L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_RX_L7p	DIFFOUT_L14p	H36	DQ4L	DQ2L	DQ1L	
1A	VREFB1AN0	IO			DIFFIO_TX_L8n	DIFFOUT_L15n	M29	DQ5L	DQ3L		
1A	VREFB1AN0	IO			DIFFIO_TX_L8p	DIFFOUT_L15p	M28	DQ5L	DQ3L		
1A	VREFB1AN0	IO			DIFFIO_RX_L8n	DIFFOUT_L16n	G38	DQSn5L	DQ3L		
1A	VREFB1AN0	IO			DIFFIO_RX_L8p	DIFFOUT_L16p	G37	DQS5L	DQ3L/CQn3L		
1A	VREFB1AN0	IO			DIFFIO_TX_L9n	DIFFOUT_L17n	N30	DQ5L	DQ3L		
1A	VREFB1AN0	IO			DIFFIO_TX_L9p	DIFFOUT_L17p	N29	DQ5L	DQ3L		
1A	VREFB1AN0	IO			DIFFIO_RX_L9n	DIFFOUT_L18n	G39	DQSn6L	DQSn3L/DQ3L		
1A	VREFB1AN0	IO			DIFFIO_RX_L9p	DIFFOUT_L18p	H39	DQS6L	DQS3L/CQ3L		
1A	VREFB1AN0	IO			DIFFIO_TX_L10n	DIFFOUT_L19n	L37	DQ6L	DQ3L		
1A	VREFB1AN0	IO			DIFFIO_TX_L10p	DIFFOUT_L19p	L36	DQ6L	DQ3L		
1A	VREFB1AN0	IO			DIFFIO_RX_L10n	DIFFOUT_L20n	J39	DQ6L	DQ3L		
1A	VREFB1AN0	IO			DIFFIO_RX_L10p	DIFFOUT_L20p	J38	DQ6L	DQ3L		
1A	VREFB1AN0	IO			DIFFIO_TX_L11n	DIFFOUT_L21n	P28	DQ7L			
1A	VREFB1AN0	IO			DIFFIO_TX_L11p	DIFFOUT_L21p	N27	DQ7L			
1A	VREFB1AN0	IO			DIFFIO_RX_L11n	DIFFOUT_L22n	K38	DQSn7L			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode (2)	DQ Group for DQS X32/X36 Mode *(2)*
1A	VREFB1AN0	IO			DIFFIO_RX_L11p	DIFFOUT_L22p	K37	DQS7L			
1A	VREFB1AN0	IO			DIFFIO_TX_L12n	DIFFOUT_L23n	R27	DQ7L			
1A	VREFB1AN0	IO			DIFFIO_TX_L12p	DIFFOUT_L23p	R26	DQ7L			
1A	VREFB1AN0	IO			DIFFIO_RX_L12n	DIFFOUT_L24n	K39				
1A	VREFB1AN0	IO			DIFFIO_RX_L12p	DIFFOUT_L24p	L39				
1C	VREFB1CN0	IO			DIFFIO_TX_L13n	DIFFOUT_L25n	R36	DQ8L	DQ8L	DQ8L	
1C	VREFB1CN0	IO			DIFFIO_TX_L13p	DIFFOUT_L25p	R35	DQ8L	DQ8L	DQ8L	
1C	VREFB1CN0	IO			DIFFIO_RX_L13n	DIFFOUT_L26n	T36	DQSn8L	DQ8L	DQ8L	
1C	VREFB1CN0	IO			DIFFIO_RX_L13p	DIFFOUT_L26p	T35	DQS8L	DQ8L/CQn8L	DQ8L	
1C	VREFB1CN0	IO			DIFFIO_TX_L14n	DIFFOUT_L27n	T33	DQ8L	DQ8L	DQ8L	
1C	VREFB1CN0	IO			DIFFIO_TX_L14p	DIFFOUT_L27p	T32	DQ8L	DQ8L	DQ8L	
1C	VREFB1CN0	IO			DIFFIO_RX_L14n	DIFFOUT_L28n	P37	DQSn9L	DQSn8L/DQ8L	DQ8L	
1C	VREFB1CN0	IO			DIFFIO_RX_L14p	DIFFOUT_L28p	P36	DQS9L	DQS8L/CQ8L	DQ8L/CQn8L	
1C	VREFB1CN0	IO			DIFFIO_TX_L15n	DIFFOUT_L29n	R34	DQ9L	DQ8L	DQ8L	
1C	VREFB1CN0	IO			DIFFIO_TX_L15p	DIFFOUT_L29p	T34	DQ9L	DQ8L	DQ8L	
1C	VREFB1CN0	IO			DIFFIO_RX_L15n	DIFFOUT_L30n	R38	DQ9L	DQ8L	DQ8L	
1C	VREFB1CN0	IO			DIFFIO_RX_L15p	DIFFOUT_L30p	R37	DQ9L	DQ8L	DQ8L	
1C	VREFB1CN0	IO			DIFFIO_TX_L16n	DIFFOUT_L31n	U31	DQ10L	DQ9L	DQ8L	
1C	VREFB1CN0	IO			DIFFIO_TX_L16p	DIFFOUT_L31p	U30	DQ10L	DQ9L	DQ8L	
1C	VREFB1CN0	IO			DIFFIO_RX_L16n	DIFFOUT_L32n	P39	DQSn10L	DQ9L	DQSn8L/DQ8L	
1C	VREFB1CN0	IO			DIFFIO_RX_L16p	DIFFOUT_L32p	R39	DQS10L	DQ9L/CQn9L	DQS8L/CQ8L	
1C	VREFB1CN0	IO			DIFFIO_TX_L17n	DIFFOUT_L33n	V29	DQ10L	DQ9L	DQ8L	
1C	VREFB1CN0	IO			DIFFIO_TX_L17p	DIFFOUT_L33p	V28	DQ10L	DQ9L	DQ8L	
1C	VREFB1CN0	IO			DIFFIO_RX_L17n	DIFFOUT_L34n	T39	DQSn11L	DQSn9L/DQ9L	DQ8L	
1C	VREFB1CN0	IO			DIFFIO_RX_L17p	DIFFOUT_L34p	T38	DQS11L	DQS9L/CQ9L	DQ8L	
1C	VREFB1CN0	IO			DIFFIO_TX_L18n	DIFFOUT_L35n	U34	DQ11L	DQ9L	DQ8L	
1C	VREFB1CN0	IO			DIFFIO_TX_L18p	DIFFOUT_L35p	U33	DQ11L	DQ9L	DQ8L	
1C	VREFB1CN0	IO			DIFFIO_RX_L18n	DIFFOUT_L36n	U37	DQ11L	DQ9L	DQ8L	
1C	VREFB1CN0	IO			DIFFIO_RX_L18p	DIFFOUT_L36p	U36	DQ11L	DQ9L	DQ8L	
1C	VREFB1CN0	IO		DATA0	DIFFIO_TX_L19n	DIFFOUT_L37n	W29	DQ12L	DQ10L		
1C	VREFB1CN0	IO			DIFFIO_TX_L19p	DIFFOUT_L37p	W28	DQ12L	DQ10L		
1C	VREFB1CN0	IO			DIFFIO_RX_L19n	DIFFOUT_L38n	U39	DQSn12L	DQ10L		
1C	VREFB1CN0	IO			DIFFIO_RX_L19p	DIFFOUT_L38p	V39	DQS12L	DQ10L/CQn10L		
1C	VREFB1CN0	IO			DIFFIO_TX_L20n	DIFFOUT_L39n	V31	DQ12L	DQ10L		
1C	VREFB1CN0	IO			DIFFIO_TX_L20p	DIFFOUT_L39p	W30	DQ12L	DQ10L		
1C	VREFB1CN0	IO			DIFFIO_RX_L20n	DIFFOUT_L40n	V38	DQSn13L	DQSn10L/DQ10L		
1C	VREFB1CN0	IO			DIFFIO_RX_L20p	DIFFOUT_L40p	V37	DQS13L	DQS10L/CQ10L		
1C	VREFB1CN0	IO		INIT_DONE	DIFFIO_TX_L21n	DIFFOUT_L41n	V33	DQ13L	DQ10L		
1C	VREFB1CN0	IO			DIFFIO_TX_L21p	DIFFOUT_L41p	W33	DQ13L	DQ10L		
1C	VREFB1CN0	IO		DEV_OE	DIFFIO_RX_L21n	DIFFOUT_L42n	V36	DQ13L	DQ10L		
1C	VREFB1CN0	IO		DEV_CLRn	DIFFIO_RX_L21p	DIFFOUT_L42p	V35	DQ13L	DQ10L		
1C	VREFB1CN0	IO	PLL_L2_CLKOUT0n		DIFFIO_TX_L22n	DIFFOUT_L43n	W35				
1C	VREFB1CN0	IO	PLL_L2_FB_CLKOUT0p		DIFFIO_TX_L22p	DIFFOUT_L43p	W34				
1C	VREFB1CN0	IO	CLK0n		DIFFIO_RX_L22n	DIFFOUT_L44n	W37				
1C	VREFB1CN0	IO	CLK0p		DIFFIO_RX_L22p	DIFFOUT_L44p	W36				
1C	VREFB1CN0	CLK1n	CLK1n				W39				
1C	VREFB1CN0	CLK1p	CLK1p				W38				
2C	VREFB2CN0	CLK3p	CLK3p				AA38				
2C	VREFB2CN0	CLK3n	CLK3n				AA39				
2C	VREFB2CN0	IO	CLK2p		DIFFIO_RX_L23p	DIFFOUT_L45p	Y36				

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode (2)	DQ Group for DQS X32/X36 Mode *(2)*
2C	VREFB2CN0	IO	CLK2n		DIFFIO_RX_L23n	DIFFOUT_L45n	Y37				
2C	VREFB2CN0	IO	PLL_L3_FB_CLKOUT0p		DIFFIO_TX_L23p	DIFFOUT_L46p	AA34				
2C	VREFB2CN0	IO	PLL_L3_CLKOUT0n		DIFFIO_TX_L23n	DIFFOUT_L46n	AA35				
2C	VREFB2CN0	IO			DIFFIO_RX_L24p	DIFFOUT_L47p	AA36	DQ14L	DQ17L		
2C	VREFB2CN0	IO			DIFFIO_RX_L24n	DIFFOUT_L47n	AA37	DQ14L	DQ17L		
2C	VREFB2CN0	IO			DIFFIO_TX_L24p	DIFFOUT_L48p	AB34	DQ14L	DQ17L		
2C	VREFB2CN0	IO			DIFFIO_TX_L24n	DIFFOUT_L48n	AB35	DQ14L	DQ17L		
2C	VREFB2CN0	IO			DIFFIO_RX_L25p	DIFFOUT_L49p	AB38	DQS14L	DQS17L/CQ17L		
2C	VREFB2CN0	IO			DIFFIO_RX_L25n	DIFFOUT_L49n	AB39	DQSn14L	DQSn17L/DQ17L		
2C	VREFB2CN0	IO			DIFFIO_TX_L25p	DIFFOUT_L50p	AB32	DQ15L	DQ17L		
2C	VREFB2CN0	IO			DIFFIO_TX_L25n	DIFFOUT_L50n	AA33	DQ15L	DQ17L		
2C	VREFB2CN0	IO			DIFFIO_RX_L26p	DIFFOUT_L51p	AB36	DQS15L	DQ17L/CQn17L		
2C	VREFB2CN0	IO			DIFFIO_RX_L26n	DIFFOUT_L51n	AB37	DQSn15L	DQ17L		
2C	VREFB2CN0	IO			DIFFIO_TX_L26p	DIFFOUT_L52p	AC33	DQ15L	DQ17L		
2C	VREFB2CN0	IO			DIFFIO_TX_L26n	DIFFOUT_L52n	AC34	DQ15L	DQ17L		
2C	VREFB2CN0	IO			DIFFIO_RX_L27p	DIFFOUT_L53p	AC39	DQ16L	DQ18L	DQ19L	
2C	VREFB2CN0	IO			DIFFIO_RX_L27n	DIFFOUT_L53n	AD39	DQ16L	DQ18L	DQ19L	
2C	VREFB2CN0	IO			DIFFIO_TX_L27p	DIFFOUT_L54p	Y30	DQ16L	DQ18L	DQ19L	
2C	VREFB2CN0	IO			DIFFIO_TX_L27n	DIFFOUT_L54n	Y31	DQ16L	DQ18L	DQ19L	
2C	VREFB2CN0	IO			DIFFIO_RX_L28p	DIFFOUT_L55p	AC36	DQS16L	DQS18L/CQ18L	DQ19L	
2C	VREFB2CN0	IO			DIFFIO_RX_L28n	DIFFOUT_L55n	AC37	DQSn16L	DQSn18L/DQ18L	DQ19L	
2C	VREFB2CN0	IO			DIFFIO_TX_L28p	DIFFOUT_L56p	AA30	DQ17L	DQ18L	DQ19L	
2C	VREFB2CN0	IO			DIFFIO_TX_L28n	DIFFOUT_L56n	AB31	DQ17L	DQ18L	DQ19L	
2C	VREFB2CN0	IO			DIFFIO_RX_L29p	DIFFOUT_L57p	AF39	DQS17L	DQ18L/CQn18L	DQS19L/CQ19L	
2C	VREFB2CN0	IO			DIFFIO_RX_L29n	DIFFOUT_L57n	AE39	DQSn17L	DQ18L	DQSn19L/DQ19L	
2C	VREFB2CN0	IO			DIFFIO_TX_L29p	DIFFOUT_L58p	AA28	DQ17L	DQ18L	DQ19L	
2C	VREFB2CN0	IO			DIFFIO_TX_L29n	DIFFOUT_L58n	Y28	DQ17L	DQ18L	DQ19L	
2C	VREFB2CN0	IO			DIFFIO_RX_L30p	DIFFOUT_L59p	AD38	DQ18L	DQ19L	DQ19L	
2C	VREFB2CN0	IO			DIFFIO_RX_L30n	DIFFOUT_L59n	AE38	DQ18L	DQ19L	DQ19L	
2C	VREFB2CN0	IO			DIFFIO_TX_L30p	DIFFOUT_L60p	AB29	DQ18L	DQ19L	DQ19L	
2C	VREFB2CN0	IO			DIFFIO_TX_L30n	DIFFOUT_L60n	AA29	DQ18L	DQ19L	DQ19L	
2C	VREFB2CN0	IO			DIFFIO_RX_L31p	DIFFOUT_L61p	AE36	DQS18L	DQS19L/CQ19L	DQ19L/CQn19L	
2C	VREFB2CN0	IO			DIFFIO_RX_L31n	DIFFOUT_L61n	AE37	DQSn18L	DQSn19L/DQ19L	DQ19L	
2C	VREFB2CN0	IO			DIFFIO_TX_L31p	DIFFOUT_L62p	AC30	DQ19L	DQ19L	DQ19L	
2C	VREFB2CN0	IO			DIFFIO_TX_L31n	DIFFOUT_L62n	AC31	DQ19L	DQ19L	DQ19L	
2C	VREFB2CN0	IO			DIFFIO_RX_L32p	DIFFOUT_L63p	AD35	DQS19L	DQ19L/CQn19L	DQ19L	
2C	VREFB2CN0	IO			DIFFIO_RX_L32n	DIFFOUT_L63n	AD36	DQSn19L	DQ19L	DQ19L	
2C	VREFB2CN0	IO			DIFFIO_TX_L32p	DIFFOUT_L64p	AD33	DQ19L	DQ19L	DQ19L	
2C	VREFB2CN0	IO			DIFFIO_TX_L32n	DIFFOUT_L64n	AD34	DQ19L	DQ19L	DQ19L	
2A	VREFB2AN0	IO			DIFFIO_RX_L33p	DIFFOUT_L65p	AK39				
2A	VREFB2AN0	IO			DIFFIO_RX_L33n	DIFFOUT_L65n	AJ39				
2A	VREFB2AN0	IO			DIFFIO_TX_L33p	DIFFOUT_L66p	AE27	DQ20L			
2A	VREFB2AN0	IO			DIFFIO_TX_L33n	DIFFOUT_L66n	AE28	DQ20L			
2A	VREFB2AN0	IO			DIFFIO_RX_L34p	DIFFOUT_L67p	AJ36	DQS20L			
2A	VREFB2AN0	IO			DIFFIO_RX_L34n	DIFFOUT_L67n	AJ37	DQSn20L			
2A	VREFB2AN0	IO			DIFFIO_TX_L34p	DIFFOUT_L68p	AH35	DQ20L			
2A	VREFB2AN0	IO			DIFFIO_TX_L34n	DIFFOUT_L68n	AH36	DQ20L			
2A	VREFB2AN0	IO			DIFFIO_RX_L35p	DIFFOUT_L69p	AL38	DQ21L	DQ24L		
2A	VREFB2AN0	IO			DIFFIO_RX_L35n	DIFFOUT_L69n	AL39	DQ21L	DQ24L		
2A	VREFB2AN0	IO			DIFFIO_TX_L35p	DIFFOUT_L70p	AH33	DQ21L	DQ24L		

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode (2)	DQ Group for DQS X32/X36 Mode *(2)*
2A	VREFB2AN0	IO			DIFFIO_TX_L35n	DIFFOUT_L70n	AG34	DQ21L	DQ24L		
2A	VREFB2AN0	IO			DIFFIO_RX_L36p	DIFFOUT_L71p	AN39	DQS21L	DQS24L/CQ24L		
2A	VREFB2AN0	IO			DIFFIO_RX_L36n	DIFFOUT_L71n	AM39	DQSn21L	DQSn24L/DQ24L		
2A	VREFB2AN0	IO			DIFFIO_TX_L36p	DIFFOUT_L72p	AG32	DQ22L	DQ24L		
2A	VREFB2AN0	IO			DIFFIO_TX_L36n	DIFFOUT_L72n	AG33	DQ22L	DQ24L		
2A	VREFB2AN0	IO			DIFFIO_RX_L37p	DIFFOUT_L73p	AL37	DQS22L	DQ24L/CQn24L		
2A	VREFB2AN0	IO			DIFFIO_RX_L37n	DIFFOUT_L73n	AK38	DQSn22L	DQ24L		
2A	VREFB2AN0	IO			DIFFIO_TX_L37p	DIFFOUT_L74p	AF30	DQ22L	DQ24L		
2A	VREFB2AN0	IO			DIFFIO_TX_L37n	DIFFOUT_L74n	AF31	DQ22L	DQ24L		
2A	VREFB2AN0	IO			DIFFIO_RX_L38p	DIFFOUT_L75p	AP38	DQ23L	DQ25L	DQ26L	
2A	VREFB2AN0	IO			DIFFIO_RX_L38n	DIFFOUT_L75n	AN38	DQ23L	DQ25L	DQ26L	
2A	VREFB2AN0	IO			DIFFIO_TX_L38p	DIFFOUT_L76p	AF28	DQ23L	DQ25L	DQ26L	
2A	VREFB2AN0	IO			DIFFIO_TX_L38n	DIFFOUT_L76n	AG29	DQ23L	DQ25L	DQ26L	
2A	VREFB2AN0	IO			DIFFIO_RX_L39p	DIFFOUT_L77p	AM36	DQS23L	DQS25L/CQ25L	DQ26L	
2A	VREFB2AN0	IO			DIFFIO_RX_L39n	DIFFOUT_L77n	AM37	DQSn23L	DQSn25L/DQ25L	DQ26L	
2A	VREFB2AN0	IO			DIFFIO_TX_L39p	DIFFOUT_L78p	AG30	DQ24L	DQ25L	DQ26L	
2A	VREFB2AN0	IO			DIFFIO_TX_L39n	DIFFOUT_L78n	AG31	DQ24L	DQ25L	DQ26L	
2A	VREFB2AN0	IO			DIFFIO_RX_L40p	DIFFOUT_L79p	AL35	DQS24L	DQ25L/CQn25L	DQS26L/CQ26L	
2A	VREFB2AN0	IO			DIFFIO_RX_L40n	DIFFOUT_L79n	AL36	DQSn24L	DQ25L	DQSn26L/DQ26L	
2A	VREFB2AN0	IO			DIFFIO_TX_L40p	DIFFOUT_L80p	AH31	DQ24L	DQ25L	DQ26L	
2A	VREFB2AN0	IO			DIFFIO_TX_L40n	DIFFOUT_L80n	AH32	DQ24L	DQ25L	DQ26L	
2A	VREFB2AN0	IO			DIFFIO_RX_L41p	DIFFOUT_L81p	AN36	DQ25L	DQ26L	DQ26L	
2A	VREFB2AN0	IO			DIFFIO_RX_L41n	DIFFOUT_L81n	AN37	DQ25L	DQ26L	DQ26L	
2A	VREFB2AN0	IO			DIFFIO_TX_L41p	DIFFOUT_L82p	AK35	DQ25L	DQ26L	DQ26L	
2A	VREFB2AN0	IO			DIFFIO_TX_L41n	DIFFOUT_L82n	AK36	DQ25L	DQ26L	DQ26L	
2A	VREFB2AN0	IO			DIFFIO_RX_L42p	DIFFOUT_L83p	AR39	DQS25L	DQS26L/CQ26L	DQ26L/CQn26L	
2A	VREFB2AN0	IO			DIFFIO_RX_L42n	DIFFOUT_L83n	AP39	DQSn25L	DQSn26L/DQ26L	DQ26L	
2A	VREFB2AN0	IO			DIFFIO_TX_L42p	DIFFOUT_L84p	AK33	DQ26L	DQ26L	DQ26L	
2A	VREFB2AN0	IO			DIFFIO_TX_L42n	DIFFOUT_L84n	AK34	DQ26L	DQ26L	DQ26L	
2A	VREFB2AN0	IO			DIFFIO_RX_L43p	DIFFOUT_L85p	AT38	DQS26L	DQ26L/CQn26L	DQ26L	
2A	VREFB2AN0	IO			DIFFIO_RX_L43n	DIFFOUT_L85n	AT39	DQSn26L	DQ26L	DQ26L	
2A	VREFB2AN0	IO			DIFFIO_TX_L43p	DIFFOUT_L86p	AJ33	DQ26L	DQ26L	DQ26L	
2A	VREFB2AN0	IO			DIFFIO_TX_L43n	DIFFOUT_L86n	AJ34	DQ26L	DQ26L	DQ26L	
2A	VREFB2AN0	IO	RUP2A		DIFFIO_RX_L44p	DIFFOUT_L87p	AP36				
2A	VREFB2AN0	IO	RDN2A		DIFFIO_RX_L44n	DIFFOUT_L87n	AR37				
2A	VREFB2AN0	IO	PLL_L4_FB_CLKOUT0p		DIFFIO_TX_L44p	DIFFOUT_L88p	AL33				
2A	VREFB2AN0	IO	PLL_L4_CLKOUT0n		DIFFIO_TX_L44n	DIFFOUT_L88n	AL34				
2A	VREFB2AN0	PLL_L4_CLKp	PLL_L4_CLKp				AU38				
2A	VREFB2AN0	PLL_L4_CLKn	PLL_L4_CLKn				AU39				
		nCONFIG		nCONFIG			AG28				
		nSTATUS		nSTATUS			AN35				
		CONF_DONE		CONF_DONE			AT37				
		PORSEL		PORSEL			AM34				
		nCE		nCE			AH29				
3A	VREFB3AN0	IO				DIFFOUT_B1n	AM30	DQ1B	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B1p	AM31	DQ1B	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO	RDN3A		DIFFIO_RX_B1n	DIFFOUT_B2n	AN30	DQSn1B	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO	RUP3A		DIFFIO_RX_B1p	DIFFOUT_B2p	AN29	DQS1B	DQ1B/CQn1B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B3n	AN31	DQ1B	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B3p	AL31	DQ1B	DQ1B	DQ1B	DQ1B

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode (2)	DQ Group for DQS X32/X36 Mode *(2)*
3A	VREFB3AN0	IO			DIFFIO_RX_B2n	DIFFOUT_B4n	AP33	DQSn2B	DQSn1B/DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B2p	DIFFOUT_B4p	AN33	DQS2B	DQS1B/CQ1B	DQ1B/CQn1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B5n	AP32	DQ2B	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B5p	AN32	DQ2B	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B3n	DIFFOUT_B6n	AR33	DQ2B	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B3p	DIFFOUT_B6p	AP34	DQ2B	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B7n	AL29	DQ3B	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B7p	AL28	DQ3B	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B4n	DIFFOUT_B8n	AK30	DQSn3B	DQ2B	DQSn1B/DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B4p	DIFFOUT_B8p	AK29	DQS3B	DQ2B/CQn2B	DQS1B/CQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B9n	AK28	DQ3B	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B9p	AJ28	DQ3B	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B5n	DIFFOUT_B10n	AT36	DQSn4B	DQSn2B/DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B5p	DIFFOUT_B10p	AR36	DQS4B	DQS2B/CQ2B	DQ1B	DQ1B/CQn1B
3A	VREFB3AN0	IO				DIFFOUT_B11n	AR34	DQ4B	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B11p	AT34	DQ4B	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B6n	DIFFOUT_B12n	AU35	DQ4B	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B6p	DIFFOUT_B12p	AT35	DQ4B	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B13n	AW37	DQ5B	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B13p	AV36	DQ5B	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B7n	DIFFOUT_B14n	AV37	DQSn5B	DQ3B	DQ2B	DQSn1B/DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B7p	DIFFOUT_B14p	AU37	DQS5B	DQ3B/CQn3B	DQ2B	DQS1B/CQ1B
3A	VREFB3AN0	IO				DIFFOUT_B15n	AW36	DQ5B	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B15p	AW38	DQ5B	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B8n	DIFFOUT_B16n	AU32	DQSn6B	DQSn3B/DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B8p	DIFFOUT_B16p	AT32	DQS6B	DQS3B/CQ3B	DQ2B/CQn2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B17n	AR31	DQ6B	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B17p	AT31	DQ6B	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B9n	DIFFOUT_B18n	AU33	DQ6B	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B9p	DIFFOUT_B18p	AT33	DQ6B	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B19n	AK27	DQ7B	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B19p	AJ27	DQ7B	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B10n	DIFFOUT_B20n	AH27	DQSn7B	DQ4B	DQSn2B/DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B10p	DIFFOUT_B20p	AG27	DQS7B	DQ4B/CQn4B	DQS2B/CQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B21n	AH26	DQ7B	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B21p	AH25	DQ7B	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B11n	DIFFOUT_B22n	AV34	DQSn8B	DQSn4B/DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B11p	DIFFOUT_B22p	AU34	DQS8B	DQS4B/CQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B23n	AV33	DQ8B	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B23p	AW33	DQ8B	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B12n	DIFFOUT_B24n	AW35	DQ8B	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B12p	DIFFOUT_B24p	AW34	DQ8B	DQ4B	DQ2B	DQ1B
3B	VREFB3BN0	IO				DIFFOUT_B25n	AN28	DQ9B	DQ9B	DQ9B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B25p	AM28	DQ9B	DQ9B	DQ9B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B13n	DIFFOUT_B26n	AR27	DQSn9B	DQ9B	DQ9B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B13p	DIFFOUT_B26p	AP27	DQS9B	DQ9B/CQn9B	DQ9B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B27n	AP29	DQ9B	DQ9B	DQ9B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B27p	AP28	DQ9B	DQ9B	DQ9B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B14n	DIFFOUT_B28n	AT28	DQSn10B	DQSn9B/DQ9B	DQ9B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B14p	DIFFOUT_B28p	AR28	DQS10B	DQS9B/CQ9B	DQ9B/CQn9B	DQ9B

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode (2)	DQ Group for DQS X32/X36 Mode *(2)*
3B	VREFB3BN0	IO				DIFFOUT_B29n	AR30	DQ10B	DQ9B	DQ9B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B29p	AT30	DQ10B	DQ9B	DQ9B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B15n	DIFFOUT_B30n	AU29	DQ10B	DQ9B	DQ9B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B15p	DIFFOUT_B30p	AT29	DQ10B	DQ9B	DQ9B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B31n	AL26	DQ11B	DQ10B	DQ9B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B31p	AK26	DQ11B	DQ10B	DQ9B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B16n	DIFFOUT_B32n	AM27	DQSn11B	DQ10B	DQSn9B/DQ9B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B16p	DIFFOUT_B32p	AL27	DQS11B	DQ10B/CQn10B	DQS9B/CQ9B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B33n	AM25	DQ11B	DQ10B	DQ9B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B33p	AL25	DQ11B	DQ10B	DQ9B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B17n	DIFFOUT_B34n	AV31	DQSn12B	DQSn10B/DQ10B	DQ9B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B17p	DIFFOUT_B34p	AU30	DQS12B	DQS10B/CQ10B	DQ9B	DQ9B/CQn9B
3B	VREFB3BN0	IO				DIFFOUT_B35n	AW32	DQ12B	DQ10B	DQ9B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B35p	AW31	DQ12B	DQ10B	DQ9B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B18n	DIFFOUT_B36n	AW30	DQ12B	DQ10B	DQ9B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B18p	DIFFOUT_B36p	AV30	DQ12B	DQ10B	DQ9B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B37n	AH24	DQ13B	DQ11B	DQ10B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B37p	AH23	DQ13B	DQ11B	DQ10B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B19n	DIFFOUT_B38n	AJ25	DQSn13B	DQ11B	DQ10B	DQSn9B/DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B19p	DIFFOUT_B38p	AJ24	DQS13B	DQ11B/CQn11B	DQ10B	DQS9B/CQ9B
3B	VREFB3BN0	IO				DIFFOUT_B39n	AK24	DQ13B	DQ11B	DQ10B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B39p	AL24	DQ13B	DQ11B	DQ10B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B20n	DIFFOUT_B40n	AR25	DQSn14B	DQSn11B/DQ11B	DQ10B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B20p	DIFFOUT_B40p	AP25	DQS14B	DQS11B/CQ11B	DQ10B/CQn10B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B41n	AN26	DQ14B	DQ11B	DQ10B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B41p	AP26	DQ14B	DQ11B	DQ10B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B21n	DIFFOUT_B42n	AP24	DQ14B	DQ11B	DQ10B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B21p	DIFFOUT_B42p	AN25	DQ14B	DQ11B	DQ10B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B43n	AT26	DQ15B	DQ12B	DQ10B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B43p	AU26	DQ15B	DQ12B	DQ10B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B22n	DIFFOUT_B44n	AU27	DQSn15B	DQ12B	DQSn10B/DQ10B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B22p	DIFFOUT_B44p	AT27	DQS15B	DQ12B/CQn12B	DQS10B/CQ10B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B45n	AT25	DQ15B	DQ12B	DQ10B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B45p	AU25	DQ15B	DQ12B	DQ10B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B23n	DIFFOUT_B46n	AW29	DQSn16B	DQSn12B/DQ12B	DQ10B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B23p	DIFFOUT_B46p	AW28	DQS16B	DQS12B/CQ12B	DQ10B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B47n	AV27	DQ16B	DQ12B	DQ10B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B47p	AV28	DQ16B	DQ12B	DQ10B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B24n	DIFFOUT_B48n	AW27	DQ16B	DQ12B	DQ10B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B24p	DIFFOUT_B48p	AW26	DQ16B	DQ12B	DQ10B	DQ9B
3C	VREFB3CN0	IO				DIFFOUT_B49n	AP22	DQ17B	DQ17B		
3C	VREFB3CN0	IO				DIFFOUT_B49p	AN23	DQ17B	DQ17B		
3C	VREFB3CN0	IO			DIFFIO_RX_B25n	DIFFOUT_B50n	AR24	DQSn17B	DQ17B		
3C	VREFB3CN0	IO			DIFFIO_RX_B25p	DIFFOUT_B50p	AP23	DQS17B	DQ17B/CQn17B		
3C	VREFB3CN0	IO				DIFFOUT_B51n	AM22	DQ17B	DQ17B		
3C	VREFB3CN0	IO				DIFFOUT_B51p	AN22	DQ17B	DQ17B		
3C	VREFB3CN0	IO			DIFFIO_RX_B26n	DIFFOUT_B52n	AU24	DQSn18B	DQSn17B/DQ17B		
3C	VREFB3CN0	IO			DIFFIO_RX_B26p	DIFFOUT_B52p	AT23	DQS18B	DQS17B/CQ17B		
3C	VREFB3CN0	IO				DIFFOUT_B53n	AV25	DQ18B	DQ17B		
3C	VREFB3CN0	IO				DIFFOUT_B53p	AW25	DQ18B	DQ17B		

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode (2)	DQ Group for DQS X32/X36 Mode *(2)*
3C	VREFB3CN0	IO			DIFFIO_RX_B27n	DIFFOUT_B54n	AW24	DQ18B	DQ17B		
3C	VREFB3CN0	IO			DIFFIO_RX_B27p	DIFFOUT_B54p	AV24	DQ18B	DQ17B		
3C	VREFB3CN0	IO				DIFFOUT_B55n	AU22	DQ19B			
3C	VREFB3CN0	IO				DIFFOUT_B55p	AW23	DQ19B			
3C	VREFB3CN0	IO			DIFFIO_RX_B28n	DIFFOUT_B56n	AU23	DQSn19B			
3C	VREFB3CN0	IO			DIFFIO_RX_B28p	DIFFOUT_B56p	AT22	DQS19B			
3C	VREFB3CN0	IO				DIFFOUT_B57n	AV22	DQ19B			
3C	VREFB3CN0	IO				DIFFOUT_B57p	AW22	DQ19B			
3C	VREFB3CN0	IO			DIFFIO_RX_B29n	DIFFOUT_B58n	AR22				
3C	VREFB3CN0	IO			DIFFIO_RX_B29p	DIFFOUT_B58p	AR21				
3C	VREFB3CN0	IO	PLL_B1_CLKOUT4			DIFFOUT_B59n	AK22				
3C	VREFB3CN0	IO	PLL_B1_CLKOUT3			DIFFOUT_B59p	AJ22				
3C	VREFB3CN0	IO			DIFFIO_RX_B30n	DIFFOUT_B60n	AL23				
3C	VREFB3CN0	IO			DIFFIO_RX_B30p	DIFFOUT_B60p	AK23				
3C	VREFB3CN0	IO	PLL_B1_CLKOUT0n			DIFFOUT_B61n	AH22				
3C	VREFB3CN0	IO	PLL_B1_CLKOUT0p			DIFFOUT_B61p	AH21				
3C	VREFB3CN0	IO	PLL_B1_FBn/CLKOUT2		DIFFIO_RX_B31n	DIFFOUT_B62n	AN21				
3C	VREFB3CN0	IO	PLL_B1_FBp/CLKOUT1		DIFFIO_RX_B31p	DIFFOUT_B62p	AM21				
3C	VREFB3CN0	IO	CLK5n			DIFFOUT_B63n	AW21				
3C	VREFB3CN0	IO	CLK5p			DIFFOUT_B63p	AV21				
3C	VREFB3CN0	IO	CLK4n		DIFFIO_RX_B32n	DIFFOUT_B64n	AU21				
3C	VREFB3CN0	IO	CLK4p		DIFFIO_RX_B32p	DIFFOUT_B64p	AT21				
4C	VREFB4CN0	IO	CLK6p		DIFFIO_RX_B33p	DIFFOUT_B65p	AT20				
4C	VREFB4CN0	IO	CLK6n		DIFFIO_RX_B33n	DIFFOUT_B65n	AU20				
4C	VREFB4CN0	IO	CLK7p			DIFFOUT_B66p	AV19				
4C	VREFB4CN0	IO	CLK7n			DIFFOUT_B66n	AW19				
4C	VREFB4CN0	IO	PLL_B2_FBp/CLKOUT1		DIFFIO_RX_B34p	DIFFOUT_B67p	AM19				
4C	VREFB4CN0	IO	PLL_B2_FBn/CLKOUT2		DIFFIO_RX_B34n	DIFFOUT_B67n	AN19				
4C	VREFB4CN0	IO	PLL_B2_CLKOUT0p			DIFFOUT_B68p	AH19				
4C	VREFB4CN0	IO	PLL_B2_CLKOUT0n			DIFFOUT_B68n	AH20				
4C	VREFB4CN0	IO			DIFFIO_RX_B35p	DIFFOUT_B69p	AL18				
4C	VREFB4CN0	IO			DIFFIO_RX_B35n	DIFFOUT_B69n	AM18				
4C	VREFB4CN0	IO	PLL_B2_CLKOUT3			DIFFOUT_B70p	AK18				
4C	VREFB4CN0	IO	PLL_B2_CLKOUT4			DIFFOUT_B70n	AJ19				
4C	VREFB4CN0	IO			DIFFIO_RX_B36p	DIFFOUT_B71p	AP17				
4C	VREFB4CN0	IO			DIFFIO_RX_B36n	DIFFOUT_B71n	AR18				
4C	VREFB4CN0	IO				DIFFOUT_B72p	AP20	DQ20B			
4C	VREFB4CN0	IO				DIFFOUT_B72n	AR19	DQ20B			
4C	VREFB4CN0	IO			DIFFIO_RX_B37p	DIFFOUT_B73p	AT19	DQS20B			
4C	VREFB4CN0	IO			DIFFIO_RX_B37n	DIFFOUT_B73n	AU19	DQSn20B			
4C	VREFB4CN0	IO				DIFFOUT_B74p	AP18	DQ20B			
4C	VREFB4CN0	IO				DIFFOUT_B74n	AP19	DQ20B			
4C	VREFB4CN0	IO			DIFFIO_RX_B38p	DIFFOUT_B75p	AT18	DQ21B	DQ22B		
4C	VREFB4CN0	IO			DIFFIO_RX_B38n	DIFFOUT_B75n	AU18	DQ21B	DQ22B		
4C	VREFB4CN0	IO				DIFFOUT_B76p	AT17	DQ21B	DQ22B		
4C	VREFB4CN0	IO				DIFFOUT_B76n	AU17	DQ21B	DQ22B		
4C	VREFB4CN0	IO			DIFFIO_RX_B39p	DIFFOUT_B77p	AR16	DQS21B	DQS22B/CQ22B		
4C	VREFB4CN0	IO			DIFFIO_RX_B39n	DIFFOUT_B77n	AT16	DQSn21B	DQSn22B/DQ22B		
4C	VREFB4CN0	IO				DIFFOUT_B78p	AW18	DQ22B	DQ22B		
4C	VREFB4CN0	IO				DIFFOUT_B78n	AV18	DQ22B	DQ22B		

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode (2)	DQ Group for DQS X32/X36 Mode *(2)*
4C	VREFB4CN0	IO			DIFFIO_RX_B40p	DIFFOUT_B79p	AV16	DQS22B	DQ22B/CQn22B		
4C	VREFB4CN0	IO			DIFFIO_RX_B40n	DIFFOUT_B79n	AW17	DQSn22B	DQ22B		
4C	VREFB4CN0	IO				DIFFOUT_B80p	AW15	DQ22B	DQ22B		
4C	VREFB4CN0	IO				DIFFOUT_B80n	AW16	DQ22B	DQ22B		
4B	VREFB4BN0	IO			DIFFIO_RX_B41p	DIFFOUT_B81p	AV15	DQ23B	DQ27B	DQ29B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B41n	DIFFOUT_B81n	AW14	DQ23B	DQ27B	DQ29B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B82p	AT15	DQ23B	DQ27B	DQ29B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B82n	AU15	DQ23B	DQ27B	DQ29B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B42p	DIFFOUT_B83p	AV13	DQS23B	DQS27B/CQ27B	DQ29B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B42n	DIFFOUT_B83n	AW13	DQSn23B	DQSn27B/DQ27B	DQ29B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B84p	AK17	DQ24B	DQ27B	DQ29B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B84n	AL17	DQ24B	DQ27B	DQ29B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B43p	DIFFOUT_B85p	AH17	DQS24B	DQ27B/CQn27B	DQS29B/CQ29B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B43n	DIFFOUT_B85n	AJ16	DQSn24B	DQ27B	DQSn29B/DQ29B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B86p	AH18	DQ24B	DQ27B	DQ29B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B86n	AJ18	DQ24B	DQ27B	DQ29B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B44p	DIFFOUT_B87p	AP16	DQ25B	DQ28B	DQ29B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B44n	DIFFOUT_B87n	AR15	DQ25B	DQ28B	DQ29B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B88p	AN14	DQ25B	DQ28B	DQ29B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B88n	AP14	DQ25B	DQ28B	DQ29B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B45p	DIFFOUT_B89p	AN15	DQS25B	DQS28B/CQ28B	DQ29B/CQn29B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B45n	DIFFOUT_B89n	AP15	DQSn25B	DQSn28B/DQ28B	DQ29B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B90p	AU14	DQ26B	DQ28B	DQ29B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B90n	AT14	DQ26B	DQ28B	DQ29B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B46p	DIFFOUT_B91p	AR12	DQS26B	DQ28B/CQn28B	DQ29B	DQS30B/CQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B46n	DIFFOUT_B91n	AT12	DQSn26B	DQ28B	DQ29B	DQSn30B/DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B92p	AR13	DQ26B	DQ28B	DQ29B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B92n	AT13	DQ26B	DQ28B	DQ29B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B47p	DIFFOUT_B93p	AW11	DQ27B	DQ29B	DQ30B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B47n	DIFFOUT_B93n	AW12	DQ27B	DQ29B	DQ30B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B94p	AV12	DQ27B	DQ29B	DQ30B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B94n	AU12	DQ27B	DQ29B	DQ30B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B48p	DIFFOUT_B95p	AT11	DQS27B	DQS29B/CQ29B	DQ30B	DQ30B/CQn30B
4B	VREFB4BN0	IO			DIFFIO_RX_B48n	DIFFOUT_B95n	AU11	DQSn27B	DQSn29B/DQ29B	DQ30B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B96p	AK15	DQ28B	DQ29B	DQ30B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B96n	AL16	DQ28B	DQ29B	DQ30B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B49p	DIFFOUT_B97p	AL15	DQS28B	DQ29B/CQn29B	DQS30B/CQ30B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B49n	DIFFOUT_B97n	AM15	DQSn28B	DQ29B	DQSn30B/DQ30B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B98p	AL14	DQ28B	DQ29B	DQ30B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B98n	AK14	DQ28B	DQ29B	DQ30B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B50p	DIFFOUT_B99p	AV10	DQ29B	DQ30B	DQ30B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B50n	DIFFOUT_B99n	AW10	DQ29B	DQ30B	DQ30B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B100p	AV9	DQ29B	DQ30B	DQ30B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B100n	AW9	DQ29B	DQ30B	DQ30B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B51p	DIFFOUT_B101p	AT10	DQS29B	DQS30B/CQ30B	DQ30B/CQn30B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B51n	DIFFOUT_B101n	AU9	DQSn29B	DQSn30B/DQ30B	DQ30B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B102p	AM13	DQ30B	DQ30B	DQ30B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B102n	AN13	DQ30B	DQ30B	DQ30B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B52p	DIFFOUT_B103p	AN12	DQS30B	DQ30B/CQn30B	DQ30B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B52n	DIFFOUT_B103n	AP12	DQSn30B	DQ30B	DQ30B	DQ30B

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode (2)	DQ Group for DQS X32/X36 Mode *(2)*
4B	VREFB4BN0	IO				DIFFOUT_B104p	AP11	DQ30B	DQ30B	DQ30B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B104n	AR10	DQ30B	DQ30B	DQ30B	DQ30B
4A	VREFB4AN0	IO			DIFFIO_RX_B53p	DIFFOUT_B105p	AR9	DQ31B	DQ35B	DQ37B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B53n	DIFFOUT_B105n	AT9	DQ31B	DQ35B	DQ37B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B106p	AN11	DQ31B	DQ35B	DQ37B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B106n	AP10	DQ31B	DQ35B	DQ37B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B54p	DIFFOUT_B107p	AT7	DQS31B	DQS35B/CQ35B	DQ37B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B54n	DIFFOUT_B107n	AT8	DQSn31B	DQSn35B/DQ35B	DQ37B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B108p	AG15	DQ32B	DQ35B	DQ37B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B108n	AH16	DQ32B	DQ35B	DQ37B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B55p	DIFFOUT_B109p	AG14	DQS32B	DQ35B/CQn35B	DQS37B/CQ37B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B55n	DIFFOUT_B109n	AH14	DQSn32B	DQ35B	DQSn37B/DQ37B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B110p	AH15	DQ32B	DQ35B	DQ37B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B110n	AJ15	DQ32B	DQ35B	DQ37B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B56p	DIFFOUT_B111p	AU8	DQ33B	DQ36B	DQ37B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B56n	DIFFOUT_B111n	AV7	DQ33B	DQ36B	DQ37B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B112p	AW8	DQ33B	DQ36B	DQ37B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B112n	AW7	DQ33B	DQ36B	DQ37B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B57p	DIFFOUT_B113p	AV6	DQS33B	DQS36B/CQ36B	DQ37B/CQn37B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B57n	DIFFOUT_B113n	AW6	DQSn33B	DQSn36B/DQ36B	DQ37B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B114p	AW4	DQ34B	DQ36B	DQ37B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B114n	AW5	DQ34B	DQ36B	DQ37B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B58p	DIFFOUT_B115p	AV3	DQS34B	DQ36B/CQn36B	DQ37B	DQS38B/CQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B58n	DIFFOUT_B115n	AV4	DQSn34B	DQ36B	DQ37B	DQSn38B/DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B116p	AW2	DQ34B	DQ36B	DQ37B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B116n	AW3	DQ34B	DQ36B	DQ37B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B59p	DIFFOUT_B117p	AT6	DQ35B	DQ37B	DQ38B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B59n	DIFFOUT_B117n	AU6	DQ35B	DQ37B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B118p	AR6	DQ35B	DQ37B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B118n	AR7	DQ35B	DQ37B	DQ38B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B60p	DIFFOUT_B119p	AT5	DQS35B	DQS37B/CQ37B	DQ38B	DQ38B/CQn38B
4A	VREFB4AN0	IO			DIFFIO_RX_B60n	DIFFOUT_B119n	AU5	DQSn35B	DQSn37B/DQ37B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B120p	AK13	DQ36B	DQ37B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B120n	AL13	DQ36B	DQ37B	DQ38B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B61p	DIFFOUT_B121p	AH13	DQS36B	DQ37B/CQn37B	DQS38B/CQ38B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B61n	DIFFOUT_B121n	AJ13	DQSn36B	DQ37B	DQSn38B/DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B122p	AJ12	DQ36B	DQ37B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B122n	AK12	DQ36B	DQ37B	DQ38B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B62p	DIFFOUT_B123p	AN9	DQ37B	DQ38B	DQ38B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B62n	DIFFOUT_B123n	AP9	DQ37B	DQ38B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B124p	AN7	DQ37B	DQ38B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B124n	AP7	DQ37B	DQ38B	DQ38B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B63p	DIFFOUT_B125p	AN8	DQS37B	DQS38B/CQ38B	DQ38B/CQn38B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B63n	DIFFOUT_B125n	AP8	DQSn37B	DQSn38B/DQ38B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B126p	AL9	DQ38B	DQ38B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B126n	AM9	DQ38B	DQ38B	DQ38B	DQ38B
4A	VREFB4AN0	IO	RUP4A		DIFFIO_RX_B64p	DIFFOUT_B127p	AL10	DQS38B	DQ38B/CQn38B	DQ38B	DQ38B
4A	VREFB4AN0	IO	RDN4A		DIFFIO_RX_B64n	DIFFOUT_B127n	AM10	DQSn38B	DQ38B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B128p	AK11	DQ38B	DQ38B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B128n	AL11	DQ38B	DQ38B	DQ38B	DQ38B

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode (2)	DQ Group for DQS X32/X36 Mode *(2)*
		nIO_PULLUP		nIO_PULLUP			AP6				
		nCEO		nCEO			AU3				
		DCLK		DCLK			AP5				
		nCSO		nCSO			AM7				
		ASDO		ASDO			AT4				
5A	VREFB5AN0	PLL_R4_CLKn	PLL_R4_CLKn				AU1				
5A	VREFB5AN0	PLL_R4_CLKp	PLL_R4_CLKp				AU2				
5A	VREFB5AN0	IO	PLL_R4_CLKOUT0n		DIFFIO_TX_R1n	DIFFOUT_R1n	AL7				
5A	VREFB5AN0	IO	PLL_R4_FB_CLKOUT0p		DIFFIO_TX_R1p	DIFFOUT_R1p	AK8				
5A	VREFB5AN0	IO	RDN5A		DIFFIO_RX_R1n	DIFFOUT_R2n	AN5				
5A	VREFB5AN0	IO	RUP5A		DIFFIO_RX_R1p	DIFFOUT_R2p	AM6				
5A	VREFB5AN0	IO			DIFFIO_TX_R2n	DIFFOUT_R3n	AL5	DQ1R	DQ1R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_TX_R2p	DIFFOUT_R3p	AL6	DQ1R	DQ1R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R2n	DIFFOUT_R4n	AR3	DQSn1R	DQ1R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R2p	DIFFOUT_R4p	AR4	DQS1R	DQ1R/CQn1R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_TX_R3n	DIFFOUT_R5n	AK5	DQ1R	DQ1R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_TX_R3p	DIFFOUT_R5p	AK6	DQ1R	DQ1R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R3n	DIFFOUT_R6n	AT2	DQSn2R	DQSn1R/DQ1R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R3p	DIFFOUT_R6p	AT3	DQS2R	DQS1R/CQ1R	DQ1R/CQn1R	
5A	VREFB5AN0	IO			DIFFIO_TX_R4n	DIFFOUT_R7n	AJ6	DQ2R	DQ1R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_TX_R4p	DIFFOUT_R7p	AJ7	DQ2R	DQ1R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R4n	DIFFOUT_R8n	AP4	DQ2R	DQ1R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R4p	DIFFOUT_R8p	AN4	DQ2R	DQ1R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_TX_R5n	DIFFOUT_R9n	AH6	DQ3R	DQ2R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_TX_R5p	DIFFOUT_R9p	AH7	DQ3R	DQ2R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R5n	DIFFOUT_R10n	AT1	DQSn3R	DQ2R	DQSn1R/DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R5p	DIFFOUT_R10p	AR1	DQS3R	DQ2R/CQn2R	DQS1R/CQ1R	
5A	VREFB5AN0	IO			DIFFIO_TX_R6n	DIFFOUT_R11n	AH8	DQ3R	DQ2R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_TX_R6p	DIFFOUT_R11p	AG9	DQ3R	DQ2R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R6n	DIFFOUT_R12n	AP1	DQSn4R	DQSn2R/DQ2R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R6p	DIFFOUT_R12p	AP2	DQS4R	DQS2R/CQ2R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_TX_R7n	DIFFOUT_R13n	AL3	DQ4R	DQ2R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_TX_R7p	DIFFOUT_R13p	AL4	DQ4R	DQ2R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R7n	DIFFOUT_R14n	AM3	DQ4R	DQ2R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_RX_R7p	DIFFOUT_R14p	AM4	DQ4R	DQ2R	DQ1R	
5A	VREFB5AN0	IO			DIFFIO_TX_R8n	DIFFOUT_R15n	AH11	DQ5R	DQ3R		
5A	VREFB5AN0	IO			DIFFIO_TX_R8p	DIFFOUT_R15p	AH12	DQ5R	DQ3R		
5A	VREFB5AN0	IO			DIFFIO_RX_R8n	DIFFOUT_R16n	AN2	DQSn5R	DQ3R		
5A	VREFB5AN0	IO			DIFFIO_RX_R8p	DIFFOUT_R16p	AN3	DQS5R	DQ3R/CQn3R		
5A	VREFB5AN0	IO			DIFFIO_TX_R9n	DIFFOUT_R17n	AG10	DQ5R	DQ3R		
5A	VREFB5AN0	IO			DIFFIO_TX_R9p	DIFFOUT_R17p	AG11	DQ5R	DQ3R		
5A	VREFB5AN0	IO			DIFFIO_RX_R9n	DIFFOUT_R18n	AN1	DQSn6R	DQSn3R/DQ3R		
5A	VREFB5AN0	IO			DIFFIO_RX_R9p	DIFFOUT_R18p	AM1	DQS6R	DQS3R/CQ3R		
5A	VREFB5AN0	IO			DIFFIO_TX_R10n	DIFFOUT_R19n	AJ3	DQ6R	DQ3R		
5A	VREFB5AN0	IO			DIFFIO_TX_R10p	DIFFOUT_R19p	AJ4	DQ6R	DQ3R		
5A	VREFB5AN0	IO			DIFFIO_RX_R10n	DIFFOUT_R20n	AL1	DQ6R	DQ3R		
5A	VREFB5AN0	IO			DIFFIO_RX_R10p	DIFFOUT_R20p	AL2	DQ6R	DQ3R		
5A	VREFB5AN0	IO			DIFFIO_TX_R11n	DIFFOUT_R21n	AF12	DQ7R			
5A	VREFB5AN0	IO			DIFFIO_TX_R11p	DIFFOUT_R21p	AG13	DQ7R			
5A	VREFB5AN0	IO			DIFFIO_RX_R11n	DIFFOUT_R22n	AK2	DQSn7R			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode (2)	DQ Group for DQS X32/X36 Mode *(2)*
5A	VREFB5AN0	IO			DIFFIO_RX_R11p	DIFFOUT_R22p	AK3	DQS7R			
5A	VREFB5AN0	IO			DIFFIO_TX_R12n	DIFFOUT_R23n	AE13	DQ7R			
5A	VREFB5AN0	IO			DIFFIO_TX_R12p	DIFFOUT_R23p	AE14	DQ7R			
5A	VREFB5AN0	IO			DIFFIO_RX_R12n	DIFFOUT_R24n	AK1				
5A	VREFB5AN0	IO			DIFFIO_RX_R12p	DIFFOUT_R24p	AJ1				
5C	VREFB5CN0	IO			DIFFIO_TX_R13n	DIFFOUT_R25n	AE4	DQ8R	DQ8R	DQ8R	
5C	VREFB5CN0	IO			DIFFIO_TX_R13p	DIFFOUT_R25p	AE5	DQ8R	DQ8R	DQ8R	
5C	VREFB5CN0	IO			DIFFIO_RX_R13n	DIFFOUT_R26n	AD4	DQSn8R	DQ8R	DQ8R	
5C	VREFB5CN0	IO			DIFFIO_RX_R13p	DIFFOUT_R26p	AD5	DQS8R	DQ8R/CQn8R	DQ8R	
5C	VREFB5CN0	IO			DIFFIO_TX_R14n	DIFFOUT_R27n	AD7	DQ8R	DQ8R	DQ8R	
5C	VREFB5CN0	IO			DIFFIO_TX_R14p	DIFFOUT_R27p	AD8	DQ8R	DQ8R	DQ8R	
5C	VREFB5CN0	IO			DIFFIO_RX_R14n	DIFFOUT_R28n	AF3	DQSn9R	DQSn8R/DQ8R	DQ8R	
5C	VREFB5CN0	IO			DIFFIO_RX_R14p	DIFFOUT_R28p	AF4	DQS9R	DQS8R/CQ8R	DQ8R/CQn8R	
5C	VREFB5CN0	IO			DIFFIO_TX_R15n	DIFFOUT_R29n	AE6	DQ9R	DQ8R	DQ8R	
5C	VREFB5CN0	IO			DIFFIO_TX_R15p	DIFFOUT_R29p	AD6	DQ9R	DQ8R	DQ8R	
5C	VREFB5CN0	IO			DIFFIO_RX_R15n	DIFFOUT_R30n	AE2	DQ9R	DQ8R	DQ8R	
5C	VREFB5CN0	IO			DIFFIO_RX_R15p	DIFFOUT_R30p	AE3	DQ9R	DQ8R	DQ8R	
5C	VREFB5CN0	IO			DIFFIO_TX_R16n	DIFFOUT_R31n	AC9	DQ10R	DQ9R	DQ8R	
5C	VREFB5CN0	IO			DIFFIO_TX_R16p	DIFFOUT_R31p	AC10	DQ10R	DQ9R	DQ8R	
5C	VREFB5CN0	IO			DIFFIO_RX_R16n	DIFFOUT_R32n	AF1	DQSn10R	DQ9R	DQSn8R/DQ8R	
5C	VREFB5CN0	IO			DIFFIO_RX_R16p	DIFFOUT_R32p	AE1	DQS10R	DQ9R/CQn9R	DQS8R/CQ8R	
5C	VREFB5CN0	IO			DIFFIO_TX_R17n	DIFFOUT_R33n	AB11	DQ10R	DQ9R	DQ8R	
5C	VREFB5CN0	IO			DIFFIO_TX_R17p	DIFFOUT_R33p	AB12	DQ10R	DQ9R	DQ8R	
5C	VREFB5CN0	IO			DIFFIO_RX_R17n	DIFFOUT_R34n	AD1	DQSn11R	DQSn9R/DQ9R	DQ8R	
5C	VREFB5CN0	IO			DIFFIO_RX_R17p	DIFFOUT_R34p	AD2	DQS11R	DQS9R/CQ9R	DQ8R	
5C	VREFB5CN0	IO			DIFFIO_TX_R18n	DIFFOUT_R35n	AC6	DQ11R	DQ9R	DQ8R	
5C	VREFB5CN0	IO			DIFFIO_TX_R18p	DIFFOUT_R35p	AC7	DQ11R	DQ9R	DQ8R	
5C	VREFB5CN0	IO			DIFFIO_RX_R18n	DIFFOUT_R36n	AC3	DQ11R	DQ9R	DQ8R	
5C	VREFB5CN0	IO			DIFFIO_RX_R18p	DIFFOUT_R36p	AC4	DQ11R	DQ9R	DQ8R	
5C	VREFB5CN0	IO			DIFFIO_TX_R19n	DIFFOUT_R37n	AA11	DQ12R	DQ10R		
5C	VREFB5CN0	IO			DIFFIO_TX_R19p	DIFFOUT_R37p	AA12	DQ12R	DQ10R		
5C	VREFB5CN0	IO			DIFFIO_RX_R19n	DIFFOUT_R38n	AC1	DQSn12R	DQ10R		
5C	VREFB5CN0	IO			DIFFIO_RX_R19p	DIFFOUT_R38p	AB1	DQS12R	DQ10R/CQn10R		
5C	VREFB5CN0	IO			DIFFIO_TX_R20n	DIFFOUT_R39n	AB9	DQ12R	DQ10R		
5C	VREFB5CN0	IO			DIFFIO_TX_R20p	DIFFOUT_R39p	AA10	DQ12R	DQ10R		
5C	VREFB5CN0	IO			DIFFIO_RX_R20n	DIFFOUT_R40n	AB2	DQSn13R	DQSn10R/DQ10R		
5C	VREFB5CN0	IO			DIFFIO_RX_R20p	DIFFOUT_R40p	AB3	DQS13R	DQS10R/CQ10R		
5C	VREFB5CN0	IO			DIFFIO_TX_R21n	DIFFOUT_R41n	AA7	DQ13R	DQ10R		
5C	VREFB5CN0	IO			DIFFIO_TX_R21p	DIFFOUT_R41p	AB7	DQ13R	DQ10R		
5C	VREFB5CN0	IO			DIFFIO_RX_R21n	DIFFOUT_R42n	AB4	DQ13R	DQ10R		
5C	VREFB5CN0	IO			DIFFIO_RX_R21p	DIFFOUT_R42p	AB5	DQ13R	DQ10R		
5C	VREFB5CN0	IO	PLL_R3_CLKOUT0n		DIFFIO_TX_R22n	DIFFOUT_R43n	AA5				
5C	VREFB5CN0	IO	PLL_R3_FB_CLKOUT0p		DIFFIO_TX_R22p	DIFFOUT_R43p	AA6				
5C	VREFB5CN0	IO	CLK9n		DIFFIO_RX_R22n	DIFFOUT_R44n	AA3				
5C	VREFB5CN0	IO	CLK9p		DIFFIO_RX_R22p	DIFFOUT_R44p	AA4				
5C	VREFB5CN0	CLK8n	CLK8n				AA1				
5C	VREFB5CN0	CLK8p	CLK8p				AA2				
6C	VREFB6CN0	CLK10p	CLK10p				W2				
6C	VREFB6CN0	CLK10n	CLK10n				W1				
6C	VREFB6CN0	IO	CLK11p		DIFFIO_RX_R23p	DIFFOUT_R45p	Y4				

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode (2)	DQ Group for DQS X32/X36 Mode *(2)*
6C	VREFB6CN0	IO	CLK11n		DIFFIO_RX_R23n	DIFFOUT_R45n	Y3				
6C	VREFB6CN0	IO	PLL_R2_FB_CLKOUT0p		DIFFIO_TX_R23p	DIFFOUT_R46p	W6				
6C	VREFB6CN0	IO	PLL_R2_CLKOUT0n		DIFFIO_TX_R23n	DIFFOUT_R46n	W5				
6C	VREFB6CN0	IO			DIFFIO_RX_R24p	DIFFOUT_R47p	W4	DQ14R	DQ17R		
6C	VREFB6CN0	IO			DIFFIO_RX_R24n	DIFFOUT_R47n	W3	DQ14R	DQ17R		
6C	VREFB6CN0	IO			DIFFIO_TX_R24p	DIFFOUT_R48p	V6	DQ14R	DQ17R		
6C	VREFB6CN0	IO			DIFFIO_TX_R24n	DIFFOUT_R48n	V5	DQ14R	DQ17R		
6C	VREFB6CN0	IO			DIFFIO_RX_R25p	DIFFOUT_R49p	V2	DQS14R	DQS17R/CQ17R		
6C	VREFB6CN0	IO			DIFFIO_RX_R25n	DIFFOUT_R49n	V1	DQSn14R	DQSn17R/DQ17R		
6C	VREFB6CN0	IO			DIFFIO_TX_R25p	DIFFOUT_R50p	V8	DQ15R	DQ17R		
6C	VREFB6CN0	IO			DIFFIO_TX_R25n	DIFFOUT_R50n	W7	DQ15R	DQ17R		
6C	VREFB6CN0	IO			DIFFIO_RX_R26p	DIFFOUT_R51p	V4	DQS15R	DQ17R/CQn17R		
6C	VREFB6CN0	IO			DIFFIO_RX_R26n	DIFFOUT_R51n	V3	DQSn15R	DQ17R		
6C	VREFB6CN0	IO			DIFFIO_TX_R26p	DIFFOUT_R52p	U7	DQ15R	DQ17R		
6C	VREFB6CN0	IO			DIFFIO_TX_R26n	DIFFOUT_R52n	U6	DQ15R	DQ17R		
6C	VREFB6CN0	IO			DIFFIO_RX_R27p	DIFFOUT_R53p	T1	DQ16R	DQ18R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_RX_R27n	DIFFOUT_R53n	U1	DQ16R	DQ18R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_TX_R27p	DIFFOUT_R54p	Y10	DQ16R	DQ18R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_TX_R27n	DIFFOUT_R54n	Y9	DQ16R	DQ18R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_RX_R28p	DIFFOUT_R55p	U4	DQS16R	DQS18R/CQ18R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_RX_R28n	DIFFOUT_R55n	U3	DQSn16R	DQSn18R/DQ18R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_TX_R28p	DIFFOUT_R56p	W10	DQ17R	DQ18R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_TX_R28n	DIFFOUT_R56n	V9	DQ17R	DQ18R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_RX_R29p	DIFFOUT_R57p	P1	DQS17R	DQ18R/CQn18R	DQS19R/CQ19R	
6C	VREFB6CN0	IO			DIFFIO_RX_R29n	DIFFOUT_R57n	R1	DQSn17R	DQ18R	DQSn19R/DQ19R	
6C	VREFB6CN0	IO			DIFFIO_TX_R29p	DIFFOUT_R58p	W12	DQ17R	DQ18R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_TX_R29n	DIFFOUT_R58n	Y12	DQ17R	DQ18R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_RX_R30p	DIFFOUT_R59p	R2	DQ18R	DQ19R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_RX_R30n	DIFFOUT_R59n	T2	DQ18R	DQ19R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_TX_R30p	DIFFOUT_R60p	V11	DQ18R	DQ19R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_TX_R30n	DIFFOUT_R60n	W11	DQ18R	DQ19R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_RX_R31p	DIFFOUT_R61p	R4	DQS18R	DQS19R/CQ19R	DQ19R/CQn19R	
6C	VREFB6CN0	IO			DIFFIO_RX_R31n	DIFFOUT_R61n	R3	DQSn18R	DQSn19R/DQ19R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_TX_R31p	DIFFOUT_R62p	U10	DQ19R	DQ19R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_TX_R31n	DIFFOUT_R62n	U9	DQ19R	DQ19R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_RX_R32p	DIFFOUT_R63p	T5	DQS19R	DQ19R/CQn19R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_RX_R32n	DIFFOUT_R63n	T4	DQSn19R	DQ19R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_TX_R32p	DIFFOUT_R64p	T7	DQ19R	DQ19R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_TX_R32n	DIFFOUT_R64n	T6	DQ19R	DQ19R	DQ19R	
6A	VREFB6AN0	IO			DIFFIO_RX_R33p	DIFFOUT_R65p	K1				
6A	VREFB6AN0	IO			DIFFIO_RX_R33n	DIFFOUT_R65n	L1				
6A	VREFB6AN0	IO			DIFFIO_TX_R33p	DIFFOUT_R66p	R13	DQ20R			
6A	VREFB6AN0	IO			DIFFIO_TX_R33n	DIFFOUT_R66n	R12	DQ20R			
6A	VREFB6AN0	IO			DIFFIO_RX_R34p	DIFFOUT_R67p	L4	DQS20R			
6A	VREFB6AN0	IO			DIFFIO_RX_R34n	DIFFOUT_R67n	L3	DQSn20R			
6A	VREFB6AN0	IO			DIFFIO_TX_R34p	DIFFOUT_R68p	M5	DQ20R			
6A	VREFB6AN0	IO			DIFFIO_TX_R34n	DIFFOUT_R68n	M4	DQ20R			
6A	VREFB6AN0	IO			DIFFIO_RX_R35p	DIFFOUT_R69p	J2	DQ21R	DQ24R		
6A	VREFB6AN0	IO			DIFFIO_RX_R35n	DIFFOUT_R69n	J1	DQ21R	DQ24R		
6A	VREFB6AN0	IO			DIFFIO_TX_R35p	DIFFOUT_R70p	M7	DQ21R	DQ24R		

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode (2)	DQ Group for DQS X32/X36 Mode *(2)*
6A	VREFB6AN0	IO			DIFFIO_TX_R35n	DIFFOUT_R70n	N6	DQ21R	DQ24R		
6A	VREFB6AN0	IO			DIFFIO_RX_R36p	DIFFOUT_R71p	G1	DQS21R	DQS24R/CQ24R		
6A	VREFB6AN0	IO			DIFFIO_RX_R36n	DIFFOUT_R71n	H1	DQSn21R	DQSn24R/DQ24R		
6A	VREFB6AN0	IO			DIFFIO_TX_R36p	DIFFOUT_R72p	N8	DQ22R	DQ24R		
6A	VREFB6AN0	IO			DIFFIO_TX_R36n	DIFFOUT_R72n	N7	DQ22R	DQ24R		
6A	VREFB6AN0	IO			DIFFIO_RX_R37p	DIFFOUT_R73p	J3	DQS22R	DQ24R/CQn24R		
6A	VREFB6AN0	IO			DIFFIO_RX_R37n	DIFFOUT_R73n	K2	DQSn22R	DQ24R		
6A	VREFB6AN0	IO			DIFFIO_TX_R37p	DIFFOUT_R74p	P10	DQ22R	DQ24R		
6A	VREFB6AN0	IO			DIFFIO_TX_R37n	DIFFOUT_R74n	P9	DQ22R	DQ24R		
6A	VREFB6AN0	IO			DIFFIO_RX_R38p	DIFFOUT_R75p	G2	DQ23R	DQ25R	DQ26R	
6A	VREFB6AN0	IO			DIFFIO_RX_R38n	DIFFOUT_R75n	F2	DQ23R	DQ25R	DQ26R	
6A	VREFB6AN0	IO			DIFFIO_TX_R38p	DIFFOUT_R76p	N11	DQ23R	DQ25R	DQ26R	
6A	VREFB6AN0	IO			DIFFIO_TX_R38n	DIFFOUT_R76n	P12	DQ23R	DQ25R	DQ26R	
6A	VREFB6AN0	IO			DIFFIO_RX_R39p	DIFFOUT_R77p	H4	DQS23R	DQS25R/CQ25R	DQ26R	
6A	VREFB6AN0	IO			DIFFIO_RX_R39n	DIFFOUT_R77n	H3	DQSn23R	DQSn25R/DQ25R	DQ26R	
6A	VREFB6AN0	IO			DIFFIO_TX_R39p	DIFFOUT_R78p	N10	DQ24R	DQ25R	DQ26R	
6A	VREFB6AN0	IO			DIFFIO_TX_R39n	DIFFOUT_R78n	N9	DQ24R	DQ25R	DQ26R	
6A	VREFB6AN0	IO			DIFFIO_RX_R40p	DIFFOUT_R79p	J5	DQS24R	DQ25R/CQn25R	DQS26R/CQ26R	
6A	VREFB6AN0	IO			DIFFIO_RX_R40n	DIFFOUT_R79n	J4	DQSn24R	DQ25R	DQSn26R/DQ26R	
6A	VREFB6AN0	IO			DIFFIO_TX_R40p	DIFFOUT_R80p	M9	DQ24R	DQ25R	DQ26R	
6A	VREFB6AN0	IO			DIFFIO_TX_R40n	DIFFOUT_R80n	M8	DQ24R	DQ25R	DQ26R	
6A	VREFB6AN0	IO			DIFFIO_RX_R41p	DIFFOUT_R81p	G4	DQ25R	DQ26R	DQ26R	
6A	VREFB6AN0	IO			DIFFIO_RX_R41n	DIFFOUT_R81n	G3	DQ25R	DQ26R	DQ26R	
6A	VREFB6AN0	IO			DIFFIO_TX_R41p	DIFFOUT_R82p	K5	DQ25R	DQ26R	DQ26R	
6A	VREFB6AN0	IO			DIFFIO_TX_R41n	DIFFOUT_R82n	K4	DQ25R	DQ26R	DQ26R	
6A	VREFB6AN0	IO			DIFFIO_RX_R42p	DIFFOUT_R83p	E1	DQS25R	DQS26R/CQ26R	DQ26R/CQn26R	
6A	VREFB6AN0	IO			DIFFIO_RX_R42n	DIFFOUT_R83n	F1	DQSn25R	DQSn26R/DQ26R	DQ26R	
6A	VREFB6AN0	IO			DIFFIO_TX_R42p	DIFFOUT_R84p	K7	DQ26R	DQ26R	DQ26R	
6A	VREFB6AN0	IO			DIFFIO_TX_R42n	DIFFOUT_R84n	K6	DQ26R	DQ26R	DQ26R	
6A	VREFB6AN0	IO			DIFFIO_RX_R43p	DIFFOUT_R85p	D2	DQS26R	DQ26R/CQn26R	DQ26R	
6A	VREFB6AN0	IO			DIFFIO_RX_R43n	DIFFOUT_R85n	D1	DQSn26R	DQ26R	DQ26R	
6A	VREFB6AN0	IO			DIFFIO_TX_R43p	DIFFOUT_R86p	L7	DQ26R	DQ26R	DQ26R	
6A	VREFB6AN0	IO			DIFFIO_TX_R43n	DIFFOUT_R86n	L6	DQ26R	DQ26R	DQ26R	
6A	VREFB6AN0	IO	RUP6A		DIFFIO_RX_R44p	DIFFOUT_R87p	F4				
6A	VREFB6AN0	IO	RDN6A		DIFFIO_RX_R44n	DIFFOUT_R87n	E3				
6A	VREFB6AN0	IO	PLL_R1_FB_CLKOUT0p		DIFFIO_TX_R44p	DIFFOUT_R88p	J7				
6A	VREFB6AN0	IO	PLL_R1_CLKOUT0n		DIFFIO_TX_R44n	DIFFOUT_R88n	J6				
6A	VREFB6AN0	PLL_R1_CLKp	PLL_R1_CLKp				C2				
6A	VREFB6AN0	PLL_R1_CLKn	PLL_R1_CLKn				C1				
7A	VREFB7AN0	IO				DIFFOUT_T1n	H9	DQ1T	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T1p	H10	DQ1T	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO	RDN7A		DIFFIO_RX_T1n	DIFFOUT_T2n	G10	DQSn1T	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO	RUP7A		DIFFIO_RX_T1p	DIFFOUT_T2p	G11	DQS1T	DQ1T/CQn1T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T3n	J9	DQ1T	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T3p	G9	DQ1T	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T2n	DIFFOUT_T4n	F7	DQSn2T	DQSn1T/DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T2p	DIFFOUT_T4p	G7	DQS2T	DQS1T/CQ1T	DQ1T/CQn1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T5n	G8	DQ2T	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T5p	F8	DQ2T	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T3n	DIFFOUT_T6n	E7	DQ2T	DQ1T	DQ1T	DQ1T

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode (2)	DQ Group for DQS X32/X36 Mode *(2)*
7A	VREFB7AN0	IO			DIFFIO_RX_T3p	DIFFOUT_T6p	F6	DQ2T	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T7n	J12	DQ3T	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T7p	J11	DQ3T	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T4n	DIFFOUT_T8n	K10	DQSn3T	DQ2T	DQSn1T/DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T4p	DIFFOUT_T8p	K11	DQS3T	DQ2T/CQn2T	DQS1T/CQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T9n	L12	DQ3T	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T9p	K12	DQ3T	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T5n	DIFFOUT_T10n	D4	DQSn4T	DQSn2T/DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T5p	DIFFOUT_T10p	E4	DQS4T	DQS2T/CQ2T	DQ1T	DQ1T/CQn1T
7A	VREFB7AN0	IO				DIFFOUT_T11n	D6	DQ4T	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T11p	E6	DQ4T	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T6n	DIFFOUT_T12n	C5	DQ4T	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T6p	DIFFOUT_T12p	D5	DQ4T	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T13n	B4	DQ5T	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T13p	A3	DQ5T	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T7n	DIFFOUT_T14n	B3	DQSn5T	DQ3T	DQ2T	DQSn1T/DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T7p	DIFFOUT_T14p	C3	DQS5T	DQ3T/CQn3T	DQ2T	DQS1T/CQ1T
7A	VREFB7AN0	IO				DIFFOUT_T15n	A2	DQ5T	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T15p	A4	DQ5T	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T8n	DIFFOUT_T16n	C8	DQSn6T	DQSn3T/DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T8p	DIFFOUT_T16p	D8	DQS6T	DQS3T/CQ3T	DQ2T/CQn2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T17n	D9	DQ6T	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T17p	E9	DQ6T	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T9n	DIFFOUT_T18n	C7	DQ6T	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T9p	DIFFOUT_T18p	D7	DQ6T	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T19n	L13	DQ7T	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T19p	K13	DQ7T	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T10n	DIFFOUT_T20n	M14	DQSn7T	DQ4T	DQSn2T/DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T10p	DIFFOUT_T20p	M15	DQS7T	DQ4T/CQn4T	DQS2T/CQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T21n	N13	DQ7T	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T21p	M13	DQ7T	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T11n	DIFFOUT_T22n	B6	DQSn8T	DQSn4T/DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T11p	DIFFOUT_T22p	C6	DQS8T	DQS4T/CQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T23n	A7	DQ8T	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T23p	B7	DQ8T	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T12n	DIFFOUT_T24n	A5	DQ8T	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T12p	DIFFOUT_T24p	A6	DQ8T	DQ4T	DQ2T	DQ1T
7B	VREFB7BN0	IO				DIFFOUT_T25n	H12	DQ9T	DQ9T	DQ9T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T25p	G12	DQ9T	DQ9T	DQ9T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T13n	DIFFOUT_T26n	E13	DQSn9T	DQ9T	DQ9T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T13p	DIFFOUT_T26p	F13	DQS9T	DQ9T/CQn9T	DQ9T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T27n	F12	DQ9T	DQ9T	DQ9T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T27p	F11	DQ9T	DQ9T	DQ9T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T14n	DIFFOUT_T28n	D12	DQSn10T	DQSn9T/DQ9T	DQ9T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T14p	DIFFOUT_T28p	E12	DQS10T	DQS9T/CQ9T	DQ9T/CQn9T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T29n	D10	DQ10T	DQ9T	DQ9T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T29p	E10	DQ10T	DQ9T	DQ9T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T15n	DIFFOUT_T30n	C11	DQ10T	DQ9T	DQ9T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T15p	DIFFOUT_T30p	D11	DQ10T	DQ9T	DQ9T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T31n	J13	DQ11T	DQ10T	DQ9T	DQ9T

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode (2)	DQ Group for DQS X32/X36 Mode *(2)*
7B	VREFB7BN0	IO				DIFFOUT_T31p	H13	DQ11T	DQ10T	DQ9T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T16n	DIFFOUT_T32n	J14	DQSn11T	DQ10T	DQSn9T/DQ9T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T16p	DIFFOUT_T32p	K14	DQS11T	DQ10T/CQn10T	DQS9T/CQ9T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T33n	J15	DQ11T	DQ10T	DQ9T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T33p	H15	DQ11T	DQ10T	DQ9T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T17n	DIFFOUT_T34n	B9	DQSn12T	DQSn10T/DQ10T	DQ9T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T17p	DIFFOUT_T34p	C10	DQS12T	DQS10T/CQ10T	DQ9T	DQ9T/CQn9T
7B	VREFB7BN0	IO				DIFFOUT_T35n	A9	DQ12T	DQ10T	DQ9T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T35p	A8	DQ12T	DQ10T	DQ9T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T18n	DIFFOUT_T36n	A10	DQ12T	DQ10T	DQ9T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T18p	DIFFOUT_T36p	B10	DQ12T	DQ10T	DQ9T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T37n	L16	DQ13T	DQ11T	DQ10T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T37p	L15	DQ13T	DQ11T	DQ10T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T19n	DIFFOUT_T38n	M16	DQSn13T	DQ11T	DQ10T	DQSn9T/DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T19p	DIFFOUT_T38p	M17	DQS13T	DQ11T/CQn11T	DQ10T	DQS9T/CQ9T
7B	VREFB7BN0	IO				DIFFOUT_T39n	J16	DQ13T	DQ11T	DQ10T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T39p	K16	DQ13T	DQ11T	DQ10T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T20n	DIFFOUT_T40n	E15	DQSn14T	DQSn11T/DQ11T	DQ10T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T20p	DIFFOUT_T40p	F15	DQS14T	DQS11T/CQ11T	DQ10T/CQn10T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T41n	F14	DQ14T	DQ11T	DQ10T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T41p	G14	DQ14T	DQ11T	DQ10T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T21n	DIFFOUT_T42n	F16	DQ14T	DQ11T	DQ10T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T21p	DIFFOUT_T42p	G15	DQ14T	DQ11T	DQ10T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T43n	D14	DQ15T	DQ12T	DQ10T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T43p	C14	DQ15T	DQ12T	DQ10T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T22n	DIFFOUT_T44n	C13	DQSn15T	DQ12T	DQSn10T/DQ10T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T22p	DIFFOUT_T44p	D13	DQS15T	DQ12T/CQn12T	DQS10T/CQ10T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T45n	C15	DQ15T	DQ12T	DQ10T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T45p	D15	DQ15T	DQ12T	DQ10T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T23n	DIFFOUT_T46n	A11	DQSn16T	DQSn12T/DQ12T	DQ10T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T23p	DIFFOUT_T46p	A12	DQS16T	DQS12T/CQ12T	DQ10T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T47n	B12	DQ16T	DQ12T	DQ10T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T47p	B13	DQ16T	DQ12T	DQ10T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T24n	DIFFOUT_T48n	A13	DQ16T	DQ12T	DQ10T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T24p	DIFFOUT_T48p	A14	DQ16T	DQ12T	DQ10T	DQ9T
7C	VREFB7CN0	IO				DIFFOUT_T49n	G18	DQ17T	DQ17T		
7C	VREFB7CN0	IO				DIFFOUT_T49p	F18	DQ17T	DQ17T		
7C	VREFB7CN0	IO			DIFFIO_RX_T25n	DIFFOUT_T50n	E16	DQSn17T	DQ17T		
7C	VREFB7CN0	IO			DIFFIO_RX_T25p	DIFFOUT_T50p	F17	DQS17T	DQ17T/CQn17T		
7C	VREFB7CN0	IO				DIFFOUT_T51n	H18	DQ17T	DQ17T		
7C	VREFB7CN0	IO				DIFFOUT_T51p	G17	DQ17T	DQ17T		
7C	VREFB7CN0	IO			DIFFIO_RX_T26n	DIFFOUT_T52n	C16	DQSn18T	DQSn17T/DQ17T		
7C	VREFB7CN0	IO			DIFFIO_RX_T26p	DIFFOUT_T52p	D17	DQS18T	DQS17T/CQ17T		
7C	VREFB7CN0	IO				DIFFOUT_T53n	A15	DQ18T	DQ17T		
7C	VREFB7CN0	IO				DIFFOUT_T53p	B15	DQ18T	DQ17T		
7C	VREFB7CN0	IO			DIFFIO_RX_T27n	DIFFOUT_T54n	A16	DQ18T	DQ17T		
7C	VREFB7CN0	IO			DIFFIO_RX_T27p	DIFFOUT_T54p	B16	DQ18T	DQ17T		
7C	VREFB7CN0	IO				DIFFOUT_T55n	A17	DQ19T			
7C	VREFB7CN0	IO				DIFFOUT_T55p	C18	DQ19T			
7C	VREFB7CN0	IO			DIFFIO_RX_T28n	DIFFOUT_T56n	C17	DQSn19T			

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode (2)	DQ Group for DQS X32/X36 Mode *(2)*
7C	VREFB7CN0	IO			DIFFIO_RX_T28p	DIFFOUT_T56p	D18	DQS19T			
7C	VREFB7CN0	IO				DIFFOUT_T57n	A18	DQ19T			
7C	VREFB7CN0	IO				DIFFOUT_T57p	B18	DQ19T			
7C	VREFB7CN0	IO			DIFFIO_RX_T29n	DIFFOUT_T58n	E18				
7C	VREFB7CN0	IO			DIFFIO_RX_T29p	DIFFOUT_T58p	E19				
7C	VREFB7CN0	IO	PLL_T2_CLKOUT4			DIFFOUT_T59n	M19				
7C	VREFB7CN0	IO	PLL_T2_CLKOUT3			DIFFOUT_T59p	M18				
7C	VREFB7CN0	IO			DIFFIO_RX_T30n	DIFFOUT_T60n	J17				
7C	VREFB7CN0	IO			DIFFIO_RX_T30p	DIFFOUT_T60p	K17				
7C	VREFB7CN0	IO	PLL_T2_CLKOUT0n			DIFFOUT_T61n	K18				
7C	VREFB7CN0	IO	PLL_T2_CLKOUT0p			DIFFOUT_T61p	L18				
7C	VREFB7CN0	IO	PLL_T2_FBn/CLKOUT2		DIFFIO_RX_T31n	DIFFOUT_T62n	G19				
7C	VREFB7CN0	IO	PLL_T2_FBp/CLKOUT1		DIFFIO_RX_T31p	DIFFOUT_T62p	H19				
7C	VREFB7CN0	IO	CLK13n			DIFFOUT_T63n	A19				
7C	VREFB7CN0	IO	CLK13p			DIFFOUT_T63p	B19				
7C	VREFB7CN0	IO	CLK12n		DIFFIO_RX_T32n	DIFFOUT_T64n	C19				
7C	VREFB7CN0	IO	CLK12p		DIFFIO_RX_T32p	DIFFOUT_T64p	D19				
8C	VREFB8CN0	IO	CLK14p		DIFFIO_RX_T33p	DIFFOUT_T65p	D20				
8C	VREFB8CN0	IO	CLK14n		DIFFIO_RX_T33n	DIFFOUT_T65n	C20				
8C	VREFB8CN0	IO	CLK15p			DIFFOUT_T66p	B21				
8C	VREFB8CN0	IO	CLK15n			DIFFOUT_T66n	A21				
8C	VREFB8CN0	IO	PLL_T1_FBp/CLKOUT1		DIFFIO_RX_T34p	DIFFOUT_T67p	H21				
8C	VREFB8CN0	IO	PLL_T1_FBn/CLKOUT2		DIFFIO_RX_T34n	DIFFOUT_T67n	G21				
8C	VREFB8CN0	IO	PLL_T1_CLKOUT0p			DIFFOUT_T68p	M21				
8C	VREFB8CN0	IO	PLL_T1_CLKOUT0n			DIFFOUT_T68n	M20				
8C	VREFB8CN0	IO			DIFFIO_RX_T35p	DIFFOUT_T69p	J22				
8C	VREFB8CN0	IO			DIFFIO_RX_T35n	DIFFOUT_T69n	H22				
8C	VREFB8CN0	IO	PLL_T1_CLKOUT3			DIFFOUT_T70p	L21				
8C	VREFB8CN0	IO	PLL_T1_CLKOUT4			DIFFOUT_T70n	K22				
8C	VREFB8CN0	IO			DIFFIO_RX_T36p	DIFFOUT_T71p	F21				
8C	VREFB8CN0	IO			DIFFIO_RX_T36n	DIFFOUT_T71n	F20				
8C	VREFB8CN0	IO				DIFFOUT_T72p	E22	DQ20T			
8C	VREFB8CN0	IO				DIFFOUT_T72n	E21	DQ20T			
8C	VREFB8CN0	IO			DIFFIO_RX_T37p	DIFFOUT_T73p	D21	DQS20T			
8C	VREFB8CN0	IO			DIFFIO_RX_T37n	DIFFOUT_T73n	C21	DQSn20T			
8C	VREFB8CN0	IO				DIFFOUT_T74p	F22	DQ20T			
8C	VREFB8CN0	IO				DIFFOUT_T74n	F23	DQ20T			
8C	VREFB8CN0	IO			DIFFIO_RX_T38p	DIFFOUT_T75p	D22	DQ21T	DQ22T		
8C	VREFB8CN0	IO			DIFFIO_RX_T38n	DIFFOUT_T75n	C22	DQ21T	DQ22T		
8C	VREFB8CN0	IO				DIFFOUT_T76p	C23	DQ21T	DQ22T		
8C	VREFB8CN0	IO				DIFFOUT_T76n	D23	DQ21T	DQ22T		
8C	VREFB8CN0	IO			DIFFIO_RX_T39p	DIFFOUT_T77p	E24	DQS21T	DQS22T/CQ22T		
8C	VREFB8CN0	IO			DIFFIO_RX_T39n	DIFFOUT_T77n	D24	DQSn21T	DQSn22T/DQ22T		
8C	VREFB8CN0	IO				DIFFOUT_T78p	B22	DQ22T	DQ22T		
8C	VREFB8CN0	IO				DIFFOUT_T78n	A22	DQ22T	DQ22T		
8C	VREFB8CN0	IO			DIFFIO_RX_T40p	DIFFOUT_T79p	B24	DQS22T	DQ22T/CQn22T		
8C	VREFB8CN0	IO			DIFFIO_RX_T40n	DIFFOUT_T79n	A23	DQSn22T	DQ22T		
8C	VREFB8CN0	IO				DIFFOUT_T80p	A24	DQ22T	DQ22T		
8C	VREFB8CN0	IO				DIFFOUT_T80n	A25	DQ22T	DQ22T		
8B	VREFB8BN0	IO			DIFFIO_RX_T41p	DIFFOUT_T81p	B25	DQ23T	DQ27T	DQ29T	DQ30T

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode (2)	DQ Group for DQS X32/X36 Mode *(2)*
8B	VREFB8BN0	IO			DIFFIO_RX_T41n	DIFFOUT_T81n	A26	DQ23T	DQ27T	DQ29T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T82p	C25	DQ23T	DQ27T	DQ29T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T82n	D25	DQ23T	DQ27T	DQ29T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T42p	DIFFOUT_T83p	B27	DQS23T	DQS27T/CQ27T	DQ29T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T42n	DIFFOUT_T83n	A27	DQSn23T	DQSn27T/DQ27T	DQ29T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T84p	J23	DQ24T	DQ27T	DQ29T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T84n	K23	DQ24T	DQ27T	DQ29T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T43p	DIFFOUT_T85p	M23	DQS24T	DQ27T/CQn27T	DQS29T/CQ29T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T43n	DIFFOUT_T85n	L24	DQSn24T	DQ27T	DQSn29T/DQ29T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T86p	L22	DQ24T	DQ27T	DQ29T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T86n	M22	DQ24T	DQ27T	DQ29T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T44p	DIFFOUT_T87p	F24	DQ25T	DQ28T	DQ29T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T44n	DIFFOUT_T87n	E25	DQ25T	DQ28T	DQ29T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T88p	F26	DQ25T	DQ28T	DQ29T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T88n	G26	DQ25T	DQ28T	DQ29T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T45p	DIFFOUT_T89p	G25	DQS25T	DQS28T/CQ28T	DQ29T/CQn29T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T45n	DIFFOUT_T89n	F25	DQSn25T	DQSn28T/DQ28T	DQ29T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T90p	D26	DQ26T	DQ28T	DQ29T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T90n	C26	DQ26T	DQ28T	DQ29T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T46p	DIFFOUT_T91p	E28	DQS26T	DQ28T/CQn28T	DQ29T	DQS30T/CQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T46n	DIFFOUT_T91n	D28	DQSn26T	DQ28T	DQ29T	DQSn30T/DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T92p	D27	DQ26T	DQ28T	DQ29T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T92n	E27	DQ26T	DQ28T	DQ29T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T47p	DIFFOUT_T93p	A29	DQ27T	DQ29T	DQ30T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T47n	DIFFOUT_T93n	A28	DQ27T	DQ29T	DQ30T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T94p	C28	DQ27T	DQ29T	DQ30T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T94n	B28	DQ27T	DQ29T	DQ30T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T48p	DIFFOUT_T95p	D29	DQS27T	DQS29T/CQ29T	DQ30T	DQ30T/CQn30T
8B	VREFB8BN0	IO			DIFFIO_RX_T48n	DIFFOUT_T95n	C29	DQSn27T	DQSn29T/DQ29T	DQ30T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T96p	J24	DQ28T	DQ29T	DQ30T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T96n	K25	DQ28T	DQ29T	DQ30T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T49p	DIFFOUT_T97p	J25	DQS28T	DQ29T/CQn29T	DQS30T/CQ30T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T49n	DIFFOUT_T97n	H25	DQSn28T	DQ29T	DQSn30T/DQ30T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T98p	K26	DQ28T	DQ29T	DQ30T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T98n	J26	DQ28T	DQ29T	DQ30T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T50p	DIFFOUT_T99p	B30	DQ29T	DQ30T	DQ30T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T50n	DIFFOUT_T99n	A30	DQ29T	DQ30T	DQ30T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T100p	A31	DQ29T	DQ30T	DQ30T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T100n	B31	DQ29T	DQ30T	DQ30T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T51p	DIFFOUT_T101p	D30	DQS29T	DQS30T/CQ30T	DQ30T/CQn30T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T51n	DIFFOUT_T101n	C31	DQSn29T	DQSn30T/DQ30T	DQ30T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T102p	G27	DQ30T	DQ30T	DQ30T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T102n	H27	DQ30T	DQ30T	DQ30T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T52p	DIFFOUT_T103p	G28	DQS30T	DQ30T/CQn30T	DQ30T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T52n	DIFFOUT_T103n	F28	DQSn30T	DQ30T	DQ30T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T104p	F29	DQ30T	DQ30T	DQ30T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T104n	E30	DQ30T	DQ30T	DQ30T	DQ30T
8A	VREFB8AN0	IO			DIFFIO_RX_T53p	DIFFOUT_T105p	E31	DQ31T	DQ35T	DQ37T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T53n	DIFFOUT_T105n	D31	DQ31T	DQ35T	DQ37T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T106p	F30	DQ31T	DQ35T	DQ37T	DQ38T

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode (2)	DQ Group for DQS X32/X36 Mode *(2)*
8A	VREFB8AN0	IO				DIFFOUT_T106n	G29	DQ31T	DQ35T	DQ37T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T54p	DIFFOUT_T107p	D33	DQS31T	DQS35T/CQ35T	DQ37T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T54n	DIFFOUT_T107n	D32	DQSn31T	DQSn35T/DQ35T	DQ37T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T108p	M24	DQ32T	DQ35T	DQ37T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T108n	N25	DQ32T	DQ35T	DQ37T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T55p	DIFFOUT_T109p	M25	DQS32T	DQ35T/CQn35T	DQS37T/CQ37T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T55n	DIFFOUT_T109n	L25	DQSn32T	DQ35T	DQSn37T/DQ37T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T110p	M26	DQ32T	DQ35T	DQ37T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T110n	N26	DQ32T	DQ35T	DQ37T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T56p	DIFFOUT_T111p	C32	DQ33T	DQ36T	DQ37T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T56n	DIFFOUT_T111n	B33	DQ33T	DQ36T	DQ37T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T112p	A32	DQ33T	DQ36T	DQ37T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T112n	A33	DQ33T	DQ36T	DQ37T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T57p	DIFFOUT_T113p	B34	DQS33T	DQS36T/CQ36T	DQ37T/CQn37T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T57n	DIFFOUT_T113n	A34	DQSn33T	DQSn36T/DQ36T	DQ37T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T114p	A35	DQ34T	DQ36T	DQ37T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T114n	A36	DQ34T	DQ36T	DQ37T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T58p	DIFFOUT_T115p	B37	DQS34T	DQ36T/CQn36T	DQ37T	DQS38T/CQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T58n	DIFFOUT_T115n	B36	DQSn34T	DQ36T	DQ37T	DQSn38T/DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T116p	A37	DQ34T	DQ36T	DQ37T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T116n	A38	DQ34T	DQ36T	DQ37T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T59p	DIFFOUT_T117p	D34	DQ35T	DQ37T	DQ38T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T59n	DIFFOUT_T117n	C34	DQ35T	DQ37T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T118p	E33	DQ35T	DQ37T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T118n	E34	DQ35T	DQ37T	DQ38T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T60p	DIFFOUT_T119p	D35	DQS35T	DQS37T/CQ37T	DQ38T	DQ38T/CQn38T
8A	VREFB8AN0	IO			DIFFIO_RX_T60n	DIFFOUT_T119n	C35	DQSn35T	DQSn37T/DQ37T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T120p	J27	DQ36T	DQ37T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T120n	K27	DQ36T	DQ37T	DQ38T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T61p	DIFFOUT_T121p	M27	DQS36T	DQ37T/CQn37T	DQS38T/CQ38T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T61n	DIFFOUT_T121n	L27	DQSn36T	DQ37T	DQSn38T/DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T122p	K28	DQ36T	DQ37T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T122n	L28	DQ36T	DQ37T	DQ38T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T62p	DIFFOUT_T123p	G31	DQ37T	DQ38T	DQ38T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T62n	DIFFOUT_T123n	F31	DQ37T	DQ38T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T124p	F33	DQ37T	DQ38T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T124n	G33	DQ37T	DQ38T	DQ38T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T63p	DIFFOUT_T125p	G32	DQS37T	DQS38T/CQ38T	DQ38T/CQn38T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T63n	DIFFOUT_T125n	F32	DQSn37T	DQSn38T/DQ38T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T126p	J30	DQ38T	DQ38T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T126n	J31	DQ38T	DQ38T	DQ38T	DQ38T
8A	VREFB8AN0	IO	RUP8A		DIFFIO_RX_T64p	DIFFOUT_T127p	H30	DQS38T	DQ38T/CQn38T	DQ38T	DQ38T
8A	VREFB8AN0	IO	RDN8A		DIFFIO_RX_T64n	DIFFOUT_T127n	H31	DQSn38T	DQ38T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T128p	J29	DQ38T	DQ38T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T128n	K29	DQ38T	DQ38T	DQ38T	DQ38T
		GND					T24				
		GND					AN6				
		GND					Y20				
		GND					L32				
		GND					AV2				

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode (2)	DQ Group for DQS X32/X36 Mode *(2)*
		GND					AV5				
		GND					AV8				
		GND					AV11				
		GND					AV14				
		GND					AV17				
		GND					AV20				
		GND					AV23				
		GND					AV26				
		GND					AV29				
		GND					AV32				
		GND					AV35				
		GND					AV38				
		GND					AR2				
		GND					AR5				
		GND					AR8				
		GND					AR11				
		GND					AR14				
		GND					AR17				
		GND					AR20				
		GND					AR23				
		GND					AR26				
		GND					AR29				
		GND					AR32				
		GND					AR35				
		GND					AR38				
		GND					AM2				
		GND					AM5				
		GND					AM8				
		GND					AM11				
		GND					AM14				
		GND					AM17				
		GND					AM20				
		GND					AM23				
		GND					AM26				
		GND					AM29				
		GND					AM32				
		GND					AM35				
		GND					AM38				
		GND					AJ2				
		GND					AJ5				
		GND					AJ8				
		GND					AJ11				
		GND					AJ14				
		GND					AJ17				
		GND					AJ20				
		GND					AJ23				
		GND					AJ26				
		GND					AJ29				
		GND					AJ32				
		GND					AJ35				

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode (2)	DQ Group for DQS X32/X36 Mode *(2)*
		GND					AJ38				
		GND					AG17				
		GND					AG19				
		GND					AG21				
		GND					AG23				
		GND					AG25				
		GND					AF2				
		GND					AF5				
		GND					AF8				
		GND					AF11				
		GND					AF14				
		GND					AF16				
		GND					AF18				
		GND					AF20				
		GND					AF22				
		GND					AF24				
		GND					AF26				
		GND					AF29				
		GND					AF32				
		GND					AF35				
		GND					AF38				
		GND					AE15				
		GND					AE17				
		GND					AE19				
		GND					AE21				
		GND					AE23				
		GND					AE25				
		GND					AD14				
		GND					AD16				
		GND					AD18				
		GND					AD20				
		GND					AD22				
		GND					AD24				
		GND					AD26				
		GND					AC2				
		GND					AC5				
		GND					AC8				
		GND					AC11				
		GND					AC13				
		GND					AC15				
		GND					AC17				
		GND					AC19				
		GND					AC21				
		GND					AC23				
		GND					AC25				
		GND					AC29				
		GND					AC32				
		GND					AC35				
		GND					AC38				
		GND					AB14				

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode (2)	DQ Group for DQS X32/X36 Mode *(2)*
		GND					AB16				
		GND					AB18				
		GND					AB20				
		GND					AB22				
		GND					AB24				
		GND					AB26				
		GND					AA13				
		GND					AA15				
		GND					AA17				
		GND					AA19				
		GND					AA21				
		GND					AA23				
		GND					AA25				
		GND					AA27				
		GND					Y2				
		GND					Y5				
		GND					Y8				
		GND					Y11				
		GND					Y14				
		GND					Y16				
		GND					Y18				
		GND					Y22				
		GND					Y24				
		GND					Y26				
		GND					Y29				
		GND					Y32				
		GND					Y35				
		GND					Y38				
		GND					W13				
		GND					W15				
		GND					W17				
		GND					W21				
		GND					W23				
		GND					W25				
		GND					W27				
		GND					V14				
		GND					V16				
		GND					V18				
		GND					V20				
		GND					V22				
		GND					V24				
		GND					V26				
		GND					U2				
		GND					U5				
		GND					U8				
		GND					U11				
		GND					U15				
		GND					U17				
		GND					U19				
		GND					U21				

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode (2)	DQ Group for DQS X32/X36 Mode *(2)*
		GND					U23				
		GND					U25				
		GND					U27				
		GND					U29				
		GND					U32				
		GND					U35				
		GND					U38				
		GND					T14				
		GND					T16				
		GND					T18				
		GND					T20				
		GND					T22				
		GND					T26				
		GND					R15				
		GND					R17				
		GND					R19				
		GND					R21				
		GND					R23				
		GND					R25				
		GND					P2				
		GND					P5				
		GND					P8				
		GND					P11				
		GND					P14				
		GND					P16				
		GND					P18				
		GND					P20				
		GND					P22				
		GND					P24				
		GND					P26				
		GND					P29				
		GND					P32				
		GND					P35				
		GND					P38				
		GND					N15				
		GND					N17				
		GND					N19				
		GND					N21				
		GND					N23				
		GND					L2				
		GND					L5				
		GND					L8				
		GND					L11				
		GND					L14				
		GND					L17				
		GND					L20				
		GND					L23				
		GND					L26				
		GND					L29				
		GND					L35				

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode (2)	DQ Group for DQS X32/X36 Mode *(2)*
		GND					L38				
		GND					H2				
		GND					H5				
		GND					H8				
		GND					H11				
		GND					H14				
		GND					H17				
		GND					H20				
		GND					H23				
		GND					H26				
		GND					H29				
		GND					H32				
		GND					H35				
		GND					H38				
		GND					E2				
		GND					E5				
		GND					E8				
		GND					E11				
		GND					E14				
		GND					E17				
		GND					E20				
		GND					E23				
		GND					E26				
		GND					E29				
		GND					E32				
		GND					E35				
		GND					E38				
		GND					B2				
		GND					B5				
		GND					B8				
		GND					B11				
		GND					B14				
		GND					B17				
		GND					B20				
		GND					B23				
		GND					B26				
		GND					B29				
		GND					B32				
		GND					B35				
		GND					B38				
		VCCL					Y19				
		VCCL					P25				
		VCCL					AF15				
		VCCL					AE16				
		VCCL					AE18				
		VCCL					AE20				
		VCCL					AE22				
		VCCL					AE24				
		VCCL					AD15				
		VCCL					AD17				

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode (2)	DQ Group for DQS X32/X36 Mode *(2)*
		VCCL					AD19				
		VCCL					AD21				
		VCCL					AD23				
		VCCL					AD25				
		VCCL					AC16				
		VCCL					AC18				
		VCCL					AC20				
		VCCL					AC22				
		VCCL					AC24				
		VCCL					AB15				
		VCCL					AB17				
		VCCL					AB19				
		VCCL					AB21				
		VCCL					AB23				
		VCCL					AB25				
		VCCL					AA16				
		VCCL					AA18				
		VCCL					AA20				
		VCCL					AA22				
		VCCL					AA24				
		VCCL					Y15				
		VCCL					Y17				
		VCCL					Y21				
		VCCL					Y23				
		VCCL					Y25				
		VCCL					W16				
		VCCL					W18				
		VCCL					W20				
		VCCL					W22				
		VCCL					W24				
		VCCL					V15				
		VCCL					V17				
		VCCL					V19				
		VCCL					V21				
		VCCL					V23				
		VCCL					V25				
		VCCL					U16				
		VCCL					U18				
		VCCL					U20				
		VCCL					U22				
		VCCL					U24				
		VCCL					T15				
		VCCL					T17				
		VCCL					T19				
		VCCL					T21				
		VCCL					T23				
		VCCL					T25				
		VCCL					R16				
		VCCL					R18				
		VCCL					R20				

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode (2)	DQ Group for DQS X32/X36 Mode *(2)*
		VCCL					R22				
		VCCL					R24				
		VCC					P21				
		VCC					AF17				
		VCC					AF19				
		VCC					AF21				
		VCC					AF23				
		VCC					AF25				
		VCC					AE26				
		VCC					AC14				
		VCC					AC26				
		VCC					AA14				
		VCC					AA26				
		VCC					W14				
		VCC					W26				
		VCC					U14				
		VCC					U26				
		VCC					R14				
		VCC					P15				
		VCC					P17				
		VCC					P19				
		VCC					P23				
		VCCPT					J32				
		VCCPT					AL32				
		VCCPT					AL8				
		VCCPT					J8				
		DNU					W19				
		VCCPGM					AJ31				
		VCCPGM					AJ10				
		TEMPDIODEn					G5				
		TEMPDIODEp					H6				
		VCC_CLKIN3C					AL21				
		VCC_CLKIN4C					AK20				
		VCC_CLKIN7C					J19				
		VCC_CLKIN8C					K20				
		VCCA_PLL_B1					AK21				
		VCCA_PLL_B2					AL19				
		VCCA_PLL_L1					L31				
		VCCA_PLL_L2					W32				
		VCCA_PLL_L3					AA32				
		VCCA_PLL_L4					AK32				
		VCCA_PLL_R1					K9				
		VCCA_PLL_R2					W8				
		VCCA_PLL_R3					AA8				
		VCCA_PLL_R4					AJ9				
		VCCA_PLL_T1					J21				
		VCCA_PLL_T2					K19				
		VCCD_PLL_B1					AJ21				
		VCCD_PLL_B2					AK19				
		VCCD_PLL_L1					M30				

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode (2)	DQ Group for DQS X32/X36 Mode *(2)*
		VCCD_PLL_L2					W31				
		VCCD_PLL_L3					AA31				
		VCCD_PLL_L4					AK31				
		VCCD_PLL_R1					L9				
		VCCD_PLL_R2					W9				
		VCCD_PLL_R3					AA9				
		VCCD_PLL_R4					AH10				
		VCCD_PLL_T1					K21				
		VCCD_PLL_T2					L19				
		VCCIO1A					K33				
		VCCIO1A					M31				
		VCCIO1A					K36				
		VCCIO1A					F37				
		VCCIO1A					B39				
		VCCIO1C					R33				
		VCCIO1C					V30				
		VCCIO1C					V34				
		VCCIO1C					T37				
		VCCIO2A					AH34				
		VCCIO2A					AV39				
		VCCIO2A					AP37				
		VCCIO2A					AK37				
		VCCIO2A					AH30				
		VCCIO2C					AB33				
		VCCIO2C					AD37				
		VCCIO2C					AB30				
		VCCIO2C					Y39				
		VCCIO3A					AH28				
		VCCIO3A					AU36				
		VCCIO3A					AP31				
		VCCIO3A					AN34				
		VCCIO3A					AL30				
		VCCIO3B					AK25				
		VCCIO3B					AU28				
		VCCIO3B					AU31				
		VCCIO3B					AN24				
		VCCIO3B					AN27				
		VCCIO3C					AL22				
		VCCIO3C					AT24				
		VCCIO3C					AP21				
		VCCIO4A					AL12				
		VCCIO4A					AU4				
		VCCIO4A					AU7				
		VCCIO4A					AN10				
		VCCIO4A					AK10				
		VCCIO4B					AK16				
		VCCIO4B					AU10				
		VCCIO4B					AU13				
		VCCIO4B					AP13				
		VCCIO4B					AN16				

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode (2)	DQ Group for DQS X32/X36 Mode *(2)*
		VCCIO4C					AN18				
		VCCIO4C					AW20				
		VCCIO4C					AU16				
		VCCIO5A					AH9				
		VCCIO5A					AV1				
		VCCIO5A					AP3				
		VCCIO5A					AK4				
		VCCIO5A					AK7				
		VCCIO5C					AB10				
		VCCIO5C					AE7				
		VCCIO5C					AD3				
		VCCIO5C					AB6				
		VCCIO6A					M10				
		VCCIO6A					M6				
		VCCIO6A					K3				
		VCCIO6A					F3				
		VCCIO6A					B1				
		VCCIO6C					V10				
		VCCIO6C					Y1				
		VCCIO6C					V7				
		VCCIO6C					T3				
		VCCIO7A					J10				
		VCCIO7A					M12				
		VCCIO7A					G6				
		VCCIO7A					F9				
		VCCIO7A					C4				
		VCCIO7B					G16				
		VCCIO7B					K15				
		VCCIO7B					G13				
		VCCIO7B					C9				
		VCCIO7B					C12				
		VCCIO7C					D16				
		VCCIO7C					J18				
		VCCIO7C					F19				
		VCCIO8A					C36				
		VCCIO8A					K30				
		VCCIO8A					J28				
		VCCIO8A					G30				
		VCCIO8A					C33				
		VCCIO8B					F27				
		VCCIO8B					K24				
		VCCIO8B					G24				
		VCCIO8B					C27				
		VCCIO8B					C30				
		VCCIO8C					G22				
		VCCIO8C					C24				
		VCCIO8C					A20				
		VCCPD1A					P27				
		VCCPD1C					V27				
		VCCPD2A					AF27				

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode (2)	DQ Group for DQS X32/X36 Mode *(2)*
		VCCPD2C					Y27				
		VCCPD3A					AG26				
		VCCPD3B					AG24				
		VCCPD3C					AG22				
		VCCPD4A					AG16				
		VCCPD4B					AG18				
		VCCPD4C					AG20				
		VCCPD5A					AF13				
		VCCPD5C					AB13				
		VCCPD6A					P13				
		VCCPD6C					Y13				
		VCCPD7A					N14				
		VCCPD7B					N16				
		VCCPD7C					N18				
		VCCPD8A					N24				
		VCCPD8B					N22				
		VCCPD8C					N20				
1A	VREFB1AN0	VREFB1AN0	VREFB1AN0				K31				
1C	VREFB1CN0	VREFB1CN0	VREFB1CN0				V32				
2A	VREFB2AN0	VREFB2AN0	VREFB2AN0				AJ30				
2C	VREFB2CN0	VREFB2CN0	VREFB2CN0				Y34				
3A	VREFB3AN0	VREFB3AN0	VREFB3AN0				AP30				
3B	VREFB3BN0	VREFB3BN0	VREFB3BN0				AM24				
3C	VREFB3CN0	VREFB3CN0	VREFB3CN0				AN20				
4A	VREFB4AN0	VREFB4AN0	VREFB4AN0				AM12				
4B	VREFB4BN0	VREFB4BN0	VREFB4BN0				AM16				
4C	VREFB4CN0	VREFB4CN0	VREFB4CN0				AN17				
5A	VREFB5AN0	VREFB5AN0	VREFB5AN0				AK9				
5C	VREFB5CN0	VREFB5CN0	VREFB5CN0				AB8				
6A	VREFB6AN0	VREFB6AN0	VREFB6AN0				L10				
6C	VREFB6CN0	VREFB6CN0	VREFB6CN0				Y6				
7A	VREFB7AN0	VREFB7AN0	VREFB7AN0				F10				
7B	VREFB7BN0	VREFB7BN0	VREFB7BN0				H16				
7C	VREFB7CN0	VREFB7CN0	VREFB7CN0				G20				
8A	VREFB8AN0	VREFB8AN0	VREFB8AN0				H28				
8B	VREFB8BN0	VREFB8BN0	VREFB8BN0				H24				
8C	VREFB8CN0	VREFB8CN0	VREFB8CN0				G23				
		NC					H33				
		NC					AM33				
		NC					AG12				
		NC					H7				
		NC *(6)*					AH1				
		NC					AP35				
		NC *(6)*					AH2				
		NC *(7)*					AH3				
		NC *(6)*					AH4				
		NC *(6)*					AH5				
		NC *(4)*					K8				
		NC *(5)*					Y33				
		NC *(5)*					AL20				

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode (2)	DQ Group for DQS X32/X36 Mode *(2)*
		NC *(5)*					Y7				
		NC *(5)*					J20				
		NC *(6)*					AH37				
		NC *(6)*					AH38				
		NC *(6)*					AH39				
		NC *(6)*					AG1				
		NC *(6)*					AG2				
		NC *(6)*					AG3				
		NC *(6)*					AG4				
		NC *(6)*					AG5				
		NC *(6)*					AG6				
		NC *(6)*					AG7				
		NC *(6)*					AG8				
		NC *(6)*					AG35				
		NC *(6)*					AG36				
		NC *(7)*					AG37				
		NC *(6)*					AG38				
		NC *(6)*					AG39				
		NC *(6)*					AF6				
		NC *(6)*					AF7				
		NC *(6)*					AF9				
		NC *(6)*					AF10				
		NC *(6)*					AF33				
		NC *(6)*					AF34				
		NC *(6)*					AF36				
		NC *(6)*					AF37				
		NC *(8)*					AE8				
		NC *(6)*					AE9				
		NC *(6)*					AE10				
		NC *(6)*					AE11				
		NC *(7)*					AE12				
		NC *(6)*					AE29				
		NC *(6)*					AE30				
		NC *(6)*					AE31				
		NC *(6)*					AE32				
		NC *(7)*					AE33				
		NC *(6)*					AE34				
		NC *(6)*					AE35				
		NC *(6)*					AD9				
		NC *(6)*					AD10				
		NC *(6)*					AD11				
		NC *(6)*					AD12				
		NC *(9)*					AD13				
		NC					AD27				
		NC *(6)*					AD28				
		NC *(6)*					AD29				
		NC *(6)*					AD30				
		NC *(6)*					AD31				
		NC *(8)*					AD32				
		NC *(6)*					AC12				

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode (2)	DQ Group for DQS X32/X36 Mode *(2)*
		NC *(6)*					AC27				
		NC *(6)*					AC28				
		NC *(9)*					AB27				
		NC *(6)*					AB28				
		NC *(6)*					V12				
		NC *(9)*					V13				
		NC *(6)*					U12				
		NC *(6)*					U13				
		NC *(6)*					U28				
		NC *(8)*					T8				
		NC *(6)*					T9				
		NC *(6)*					T10				
		NC *(6)*					T11				
		NC *(6)*					T12				
		NC					T13				
		NC *(9)*					T27				
		NC *(6)*					T28				
		NC *(6)*					T29				
		NC *(6)*					T30				
		NC *(6)*					T31				
		NC *(6)*					R5				
		NC *(6)*					R6				
		NC *(7)*					R7				
		NC *(6)*					R8				
		NC *(6)*					R9				
		NC *(6)*					R10				
		NC *(6)*					R11				
		NC *(7)*					R28				
		NC *(6)*					R29				
		NC *(6)*					R30				
		NC *(6)*					R31				
		NC *(8)*					R32				
		NC *(6)*					P3				
		NC *(6)*					P4				
		NC *(6)*					P6				
		NC *(6)*					P7				
		NC *(6)*					P30				
		NC *(6)*					P31				
		NC *(6)*					P33				
		NC *(6)*					P34				
		NC *(6)*					N1				
		NC *(6)*					N2				
		NC *(7)*					N3				
		NC *(6)*					N4				
		NC *(6)*					N5				
		NC					N12				
		NC					N28				
		NC *(6)*					N32				
		NC *(6)*					N33				
		NC *(6)*					N34				

Bank Number	VREF Group	Pin Name /Function	Optional Function(s)	Configuration Function for Stratix III Only *(1)*	Dedicated Tx_Rx Channel *(2)*	Emulated LVDS Output Channel *(2)*	F1517	DQ Group for DQS X4 Mode *(2)*	DQ Group for DQS X8/X9 Mode *(2)*	DQ Group for DQS X16/X18 Mode (2)	DQ Group for DQS X32/X36 Mode *(2)*
		NC *(6)*					N35				
		NC *(6)*					N36				
		NC *(6)*					N37				
		NC *(6)*					N38				
		NC *(6)*					N39				
		NC *(6)*					M1				
		NC *(6)*					M2				
		NC *(6)*					M3				
		NC *(6)*					M35				
		NC *(6)*					M36				
		NC *(7)*					M37				
		NC *(6)*					M38				
		NC *(6)*					M39				
		NC					L30				
		NC *(3)*		MSEL2			D3				
		NC *(3)*		MSEL1			F5				
		NC *(3)*		MSEL0			M11				

Notes on Pin Table:

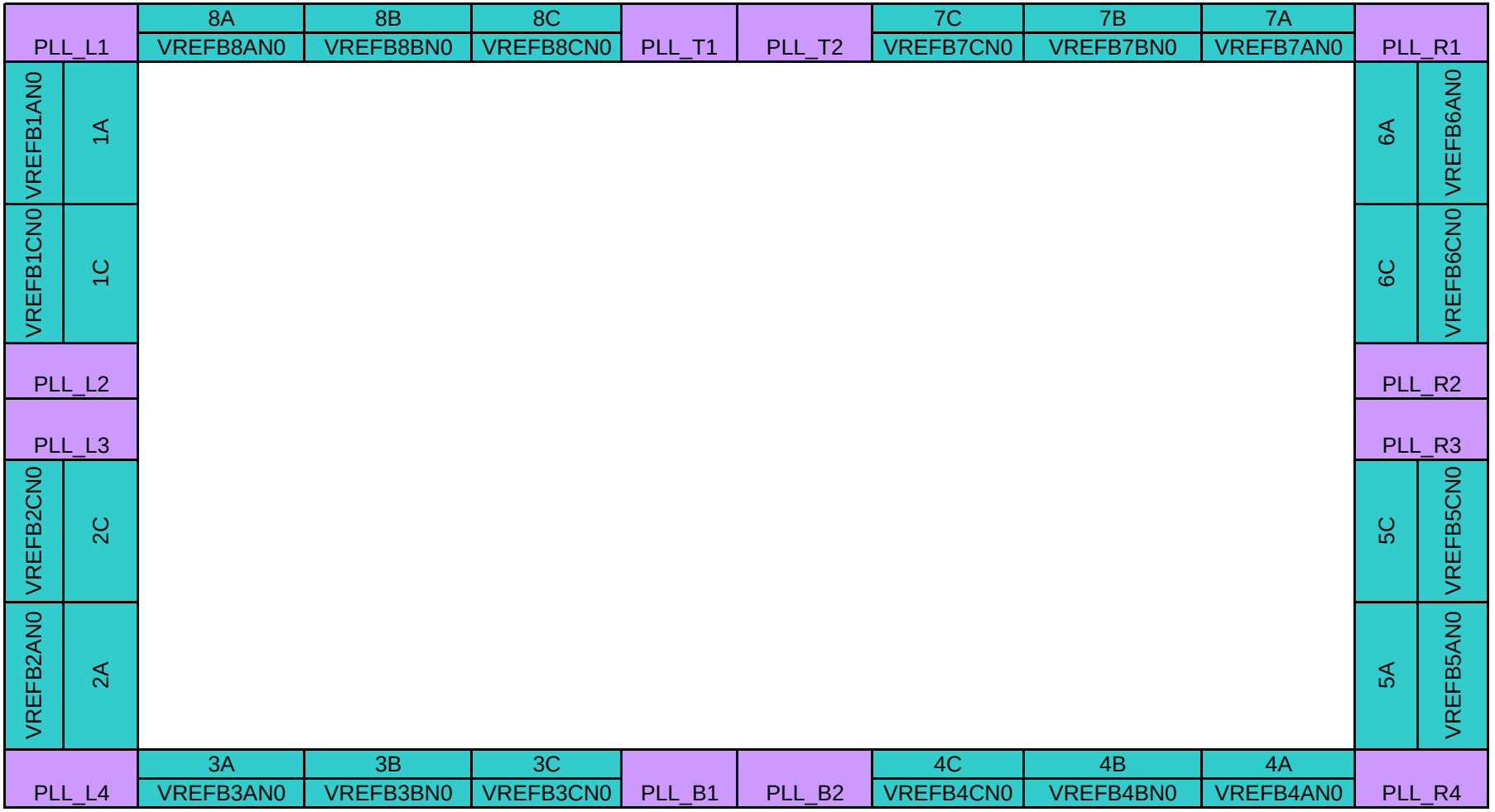
(1) These pins should be connected on the board to properly configure the FPGA prototype. See Stratix® III device pin table for details.
(2) The individual index number of the pin in this column may not be the same as its companion Stratix III device, but the functionality of the pin is fully migratable.
(3) These NO CONNECT (NC) pins are MSEL configuration input pins in the Stratix III device and should be connected on the board to configure the FPGA prototype.
(4) This NC pin is a VCCBAT pin in the Stratix III device and should be connected for the FPGA prototype.
(5) This NC pin is a VCCPT pin in the Stratix III device and should be connected for the FPGA prototype.
(6) This NC pin is an IO pin in the Stratix III device and can be left unconnected.
(7) This NC pin is a VCCIO pin in the Stratix III device and should be connected to VCCIO power for the FPGA prototype.
(8) This NC pin is a VREF pin in the Stratix III device and should be connected to the VREF input reference voltage for the FPGA prototype.
(9) This NC pin is a VCCPD pin in the Stratix III device and should be connected to VCCPD power for the FPGA prototype.

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
	Supply and Reference Pins	
VCCL	Power	VCCL supplies power to the core voltage power supply pins.
VCC	Power	VCC supplies power to the periphery circuitry.
RUP[1..8]A	I/O, Input	Reference pins for I/O banks. The RUP pins share the same VCCIO with the I/O bank where they are located. The external precision resistor RUP must be connected to the designated RUP pin within the bank. If not required, this pin is a regular I/O pin.
RDN[1..8]A	I/O, Input	Reference pins for I/O banks. The RDN pins share the same GND with the I/O bank where they are located. The external precision resistor RDN must be connected to the designated RDN pin within the bank. If not required, this pin is a regular I/O pin.
VCCIO[1..8][A,B,C]	Power	These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all LVDS, LVCMOS(1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.0 V), HSTL(12, 15, 18), SSTL(15, 18, 2), 3.0-V PCI/PCI-X I/O, and 3.0 V LVTTL I/O standards. VCCIO also supplies power to the input buffers used for LVCMOS(1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.0 V), 3.0-V PCI/PCI-X and 3.0 V LVTTL I/O standards.
VREF[1..8][A,B,C]	Power	Input reference voltage for each I/O bank. If a bank uses a voltage-referenced I/O standard, these pins are used as the voltage-referenced pins for the bank.
VCCA_PLL[L[1:4],R[1:4],T[1:2],B[1:2]]	Power	Analog power for PLLs[L[1:4],R[1:4],T[1:2],B[1:2]]. You must power up these pins even if the PLL is not used. You are advised to keep this pin isolated from other VCC for better jitter performance.
VCCD_PLL[L[1:4],R[1:4],T[1:2],B[1:2]]	Power	Digital power for PLLs[L[1:4],R[1:4],T[1:2],B[1:2]]. You must power up these pins even if the PLL is not used.
VCCPT	Power	Power supply for the programmable power technology.
VCCPGM	Power	Power supply for configuration pins. Can be connected to 1.8 V, 2.5 V or 3.0 V depending on the particular design.
VCCPD[1..8][A,B,C]	Power	Dedicated power pins. This supply is used to power the I/O pre-drivers. This can be connected to 3.0 V or 2.5 V. VCCPD for 3.0-V I/O standard is 3.0 V, and VCCPD for 2.5-V/1.8-V/1.2-V I/O standards is 2.5 V.
VCC_CLKIN[3,4,7,8]	Power	Differential clock input power supply for top and bottom I/O banks.
GND	Ground	Device ground pins.
DNU	Do Not Use	Do not connect to power or ground or any other signal; must be left floating.
NC	No Connect	Do not drive signals into these pins.
	Dedicated Configuration/JTAG Pins	
nIO_PULLUP	Input	Dedicated input that chooses whether the internal pull-up resistors on the user I/O pins are on or off during power up. A logic high (0.9 V) turns off the weak pull-ups, while a logic low turns them on.
TEMPDIODEp	Input	Pin used in conjunction with the temperature-sensing diode (bias-high input) inside the HardCopy III device.
TEMPDIODEn	Input	Pin used in conjunction with the temperature-sensing diode (bias-low input) inside the HardCopy III device.
nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled.
nCONFIG	Input	Dedicated power up block control input. Pulling this pin low during user-mode will cause the HardCopy III to enter a reset state & tri-state all I/O pins. Returning this pin to a logic high level will initiate the power up and initialization sequence. It is not available as a user I/O pin.
CONF_DONE	Bidirectional (open-drain)	This is a dedicated power up block status pin. As a status output, the CONF_DONE pin drives low before and during initialization. Driven this pin high indicates that the device is entering user mode.
nCEO	Output	Output that drives low when device initialization is complete.
nSTATUS	Bidirectional (open-drain)	This is a dedicated power up block status pin. The HardCopy III drives nSTATUS low indicates that the device is being initialized. As a status output, the nSTATUS is pulled low if an error occurs during initialization. As a status input, this pin delays the completion of the Initialization phase when nSTATUS is driven low by an external source during initialization. It is not available as a user I/O pin.
PORSEL	Input	Dedicated input which selects between a POR time of 12 ms or 100 ms. A logic high (1.5 V, 1.8 V, 2.5 V,3.0 V) selects a POR time of 12 ms and a logic low selects POR time of 100 ms.
TCK	Input	Dedicated JTAG input pin. Connect TCK to GND if the JTAG circuitry is not used.
TMS	Input	Dedicated JTAG input pin. Connect TMS to VCCPD if the JTAG circuitry is not used.
TDI	Input	Dedicated JTAG input pin. Connect TDI to VCCPD if the JTAG circuitry is not used.
TDO	Output	Dedicated JTAG output pin.
TRST	Input	Dedicated active-low JTAG input pin. TRST is used to asynchronously reset the JTAG boundary-scan circuit.

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
	Clock and PLL Pins	
CLK[1,3,8,10]p	Clock, Input	Dedicated high speed clock input pins 1, 3, 8, and 10 that can also be used for data inputs. OCT Rd is not supported on these pins.
CLK[1,3,8,10]n	Clock, Input	Dedicated negative clock input pins for differential clock input that can also be used for data inputs. OCT Rd is not supported on these pins.
CLK[0,2,4,5,6,7,9,11..15]p	I/O, Clock	These pins can be used as I/O pins or clock input pins. OCT Rd is supported on these pins.
CLK[0,2,4,5,6,7,9,11..15]n	I/O, Clock	These pins can be used as I/O pins or negative clock input pins for differential clock inputs. OCT Rd is supported on these pins.
PLL_[L1,L4,R1,R4]_CLKp	Clock, Input	Dedicated clock input pins to PLL L1, L4, R1, and R4 respectively.
PLL_[L1,L4,R1,R4]_CLKn	Clock, Input	Dedicated negative clock input pins for dfferential clock input to PLL L1, L4, R1, and R4 respectively.
PLL_[L2,L3,R2,R3]_CLKOUT0n	I/O, Clock	Each left and right PLL supports 2 clock I/O pins, configured either as 2 single-ended I/O or one differential I/O pair. When using both pins as single-ended I/Os, PLL_#_CLKOUT0n can be the clock output while the PLL_#_FB_CLKOUT0p is the external feedback input pin.
PLL_[L2,L3,R2,R3]_FB_CLKOUT0p	I/O, Clock	
PLL_[T1,T2,B1,B2]_FBp/CLKOUT1	I/O, Clock	Dual-purpose I/O pins that can be used as two single-ended outputs or one differential external feedback input pin.
PLL_[T1,T2,B1,B2]_FBn/CLKOUT2	I/O, Clock	
PLL_[T1,T2,B1,B2]_CLKOUT[3,4]	I/O, Clock	These pins can be used as I/O pins or two single-ended clock ouput pins.
PLL_[T1,T2,B1,B2]_CLKOUT0[p,n]	I/O, Clock	I/O pins that be used as two single-ended clock output pins or one differential clock output pair.
	Optional/Dual-Purpose Configuration Pins	
nCSO	I/O Output	Dedicated control signal from Stratix III devices, but kept in HardCopy III for compatibility reasons.
ASDO	I/O Output	Dedicated control signal from Stratix III devices, but kept in HardCopy III for compatibility reasons.
DCLK	Input (PS, FPP) Output (AS)	Dedicated configuration clock pin on Stratix III devices, but kept in HardCopy III for compatibility reasons. It's not required to clock this pin for HardCopy III.
	Differential I/O Pins	
DIFFIO_RX[##]p/n	I/O, RX channel	These are true LVDS receiver channels on side and column I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFIO_TX[##]p/n	I/O, TX channel	These are true LVDS transmitter channels on side I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFOUT_[##]p/n	I/O, TX channel	These are emulated LVDS output channels. On column I/O banks, there are true LVDS input buffers but no true LVDS output buffers. However, all column user I/Os, including I/Os with true LVDS input buffers, can be configured as emulated LVDS output buffers.Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
	External Memory Interface Pins	
DQS[1..44][T,B], DQS[1..40][L,R]	I/O,DQS	Optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase-shift circuitry. The shifted DQS signal can also drive to internal logic.
DQSn[1..44][T,B], DQSn[1..40][L,R]	I/O,DQSn	Optional complementary data strobe signal for use in QDRII SRAM. These pins drive to dedicated DQS phase-shift circuitry.
DQ[1..44][T,B],DQ[1..40][L,R]	I/O,DQ	Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important; however, use caution when making pin assignments if you plan on migrating to a different memory interface that has a different DQ bus width. Analyze the available DQ pins across all pertinent DQS columns in the pin list.
CQ[1..44][T,B], CQ[1..40][L,R]	DQS	Optional data strobe signal for use in QDRII SRAM. These are the pins for echo clocks.
CQn[1..44][T,B], CQ[1..40][L,R]	DQS	Optional complementary data strobe signal for use in QDRII SRAM. These are the pins for echo clocks.

Notes:

(1) These pin definitions are prepared based on the device with the largest density, HC335. Refer to the pin list for the availability of pins in each density.



Notes:

1. This is a top view of the silicon die. For flip chip packages, the die is mounted upside down in the package; therefore, to obtain the top package view, flip this diagram on its vertical axis.
2. This is a pictorial representation only to get an idea of placement on the device. Refer to the pin list and the Quartus® II software for exact locations.

Version Number	Date	Changes Made
1.0	7/24/2009	Initial release.