Pin Information for HardCopy® II HC220 / Stratix® II EP2S60 F672 Companion Devices Version 1.1

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/DQ Group for DQS x4 Mode	Configuration Function for Stratix II Only (Note 1)	F672	DQ Group for DQS x8/x9 Mode	DQ Group for DQS x16/x18 Mode
		NC (Note 3)			D23		
B2		IO	DIFFIO_RX36p		C26		
B2		IO	DIFFIO_RX36n		C25		
B2		IO	DIFFIO_TX36p		H20		
B2		IO	DIFFIO_TX36n		H19		
B2		IO	DIFFIO_RX35p		D25		
B2		IO	DIFFIO_RX35n		D24		
B2		IO	DIFFIO_TX35p		G21		
B2		IO	DIFFIO_TX35n		G20		
B2		IO	DIFFIO_RX34p		E24		
B2		IO	DIFFIO_RX34n		E23		
B2		IO	DIFFIO_TX34p		F22		
B2		IO	DIFFIO_TX34n		F21		
B2		IO	DIFFIO_RX33p		E26		
B2		IO	DIFFIO_RX33n		E25		
B2		IO	DIFFIO_TX33p		H22		
B2		IO	DIFFIO_TX33n		H21		
B2		IO	DIFFIO_RX32p		F24		
B2		IO	DIFFIO_RX32n		F23		
B2		IO	DIFFIO_TX32p		J22		
B2		IO	DIFFIO_TX32n		J21		
		NC (Note 3)			G22		
B2		IO	DIFFIO_RX31p		F26		
B2		IO	DIFFIO_RX31n		F25		
B2		IO	DIFFIO_TX31p		J20		
B2		IO	DIFFIO_TX31n		J19		
B2		IO	DIFFIO_RX30p		G24		
B2		IO	DIFFIO_RX30n		G23		
B2		IO	DIFFIO_TX30p		K22		
B2		IO	DIFFIO_TX30n		K21		
B2		IO	DIFFIO_RX29p		H24		
B2		IO	DIFFIO_RX29n		H23		
B2		IO	DIFFIO_TX29p		K20		
B2		IO	DIFFIO_TX29n		K19		
B2		IO	DIFFIO_RX28p		J24		
B2		IO	DIFFIO_RX28n		J23		
B2		IO	DIFFIO_TX28p		L23		
B2		IO	DIFFIO_TX28n		L22		
B2		IO	DIFFIO_RX27p		K24		
B2		IO	DIFFIO_RX27n		K23		
B2		IO	DIFFIO_TX27p		L21		
B2		IO	DIFFIO_TX27n		L20		
B2		IO	DIFFIO_RX26p		G26		
B2		IO	DIFFIO_RX26n		G25		
B2		IO	DIFFIO_TX26p		L19		
B2		IO	DIFFIO_TX26n		L18		
B2		IO	DIFFIO_RX25p		H26		
B2		IO	DIFFIO_RX25n		H25		
B2		IO	DIFFIO_TX25p		M24		
B2		IO	DIFFIO_TX25n		M23		
B2		IO	DIFFIO_RX24p		J26		
B2		IO	DIFFIO_RX24n		J25		
B2		IO	DIFFIO_TX24p		M22		
B2		IO	DIFFIO_TX24n		M21		
		NC (Note 3)			N23		
B2		IO	DIFFIO_RX23p		L25		
B2		IO	DIFFIO_RX23n		L24		
B2		IO	DIFFIO_TX23p		N22		
B2		IO	DIFFIO_TX23n		N21		
B2		IO	DIFFIO_RX22p		K26		
B2		IO	DIFFIO_RX22n		K25		
B2		IO	DIFFIO_TX22p		N20		
B2		IO	DIFFIO_TX22n		N19		
B2		IO	DIFFIO_RX21p		M26		

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/DQ Group for DQS x4 Mode	Configuration Function for Stratix II Only (Note 1)	F672	DQ Group for DQS x8/x9 Mode	DQ Group for DQS x16/x18 Mode
B2		IO	DIFFIO_RX21n		M25		
B2		IO	DIFFIO_TX21p		M20		
B2		IO	DIFFIO_TX21n		M19		
B2		IO	CLK0n/DIFFIO_RX_C0n		P24		
B2		IO	CLK0p/DIFFIO_RX_C0p		P25		
B2		CLK1n	INPUT		N24		
B2		CLK1p	INPUT		N25		
		VCCD_PLL1			P19		
		VCCA_PLL1			P21		
		GNDA_PLL1			N18		
		GNDA_PLL1			P18		
		GNDA_PLL2			R19		
		GNDA_PLL2			R20		
		VCCA_PLL2			R21		
		VCCD_PLL2			P20		
B1		IO	CLK2p/DIFFIO_RX_C1p		R26		
B1		IO	CLK2n/DIFFIO_RX_C1n		R25		
B1		CLK3p	INPUT		P23		
B1		CLK3n	INPUT		P22		
B1		IO	DIFFIO_RX20p		T25		
B1		IO	DIFFIO_RX20n		T24		
B1		IO	DIFFIO_TX20p		R24		
B1		IO	DIFFIO_TX20n		R23		
B1		IO	DIFFIO_RX19p		U26		
B1		IO	DIFFIO_RX19n		U25		
B1		IO	DIFFIO_TX19p		U24		
B1		IO	DIFFIO_TX19n		U23		
		NC (Note 3)			T23		
B1		IO	DIFFIO_RX18p		V26		
B1		IO	DIFFIO_RX18n		V25		
B1		IO	DIFFIO_TX18p		V24		
B1		IO	DIFFIO_TX18n		V23		
B1		IO	DIFFIO_RX17p		W26		
B1		IO	DIFFIO_RX17n		W25		
B1		IO	DIFFIO_TX17p		W22		
B1		IO	DIFFIO_TX17n		W21		
B1		IO	DIFFIO_RX16p		Y26		
B1		IO	DIFFIO_RX16n		Y25		
B1		IO	DIFFIO_TX16p		V22		
B1		IO	DIFFIO_TX16n		V21		
B1		IO	DIFFIO_RX15p		AA26		
B1		IO	DIFFIO_RX15n		AA25		
B1		IO	DIFFIO_TX15p		U22		
B1		IO	DIFFIO_TX15n		U21		
B1		IO	DIFFIO_RX14p		AA24		
B1		IO	DIFFIO_RX14n		AA23		
B1		IO	DIFFIO_TX14p		T20		
B1		IO	DIFFIO_TX14n		T19		
B1		IO	DIFFIO_RX13p		Y24		
B1		IO	DIFFIO_RX13n		Y23		
B1		IO	DIFFIO_TX13p		T22		
B1		IO	DIFFIO_TX13n		T21		
B1		IO	DIFFIO_RX12p		W24		
B1		IO	DIFFIO_RX12n		W23		
B1		IO	DIFFIO_TX12p		U20		
B1		IO	DIFFIO_TX12n		U19		
		NC (Note 3)			Y22		
B1		IO	DIFFIO_RX11p		AB26		
B1		IO	DIFFIO_RX11n		AB25		
B1		IO	DIFFIO_TX11p		V20		
B1		IO	DIFFIO_TX11n		V19		
B1		IO	DIFFIO_RX10p		AB24		
B1		IO	DIFFIO_RX10n		AB23		
B1		IO	DIFFIO_TX10p		AA22		

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/DQ Group for DQS x4 Mode	Configuration Function for Stratix II Only (Note 1)	F672	DQ Group for DQS x8/x9 Mode	DQ Group for DQS x16/x18 Mode
B1		IO	DIFFIO_TX10n		AA21		
B1		IO	DIFFIO_RX9p		AC25		
B1		IO	DIFFIO_RX9n		AC24		
B1		IO	DIFFIO_TX9p		Y21		
B1		IO	DIFFIO_TX9n		Y20		
B1		IO	DIFFIO_RX8p		AD26		
B1		IO	DIFFIO_RX8n		AD25		
B1		IO	DIFFIO_TX8p		W20		
B1		IO	DIFFIO_TX8n		W19		
		NC (Note 3)			AC23		
B8		TDI		TDI	AE25		
B8		TMS		TMS	AD24		
B8		TCK		TCK	AB22		
B8		TRST		TRST	AB21		
B8		nCONFIG		nCONFIG	AA20		
B8		VCCSEL		VCCSEL	Y19		
B8		IO			AC19		
B8		IO		CS	AC21		
B8		IO		CLKUSR	AA19		
B8		IO		nWS	AB20		
B8		IO		nRS	AC20		
B8		IO			AE24		
B8		IO			AD23		
		NC (Note 3)			AC22		
B8		IO			AF24		
B8		IO			AE22		
B8		IO			AD22		
B8		IO			AE23		
B8		IO			V18		
B8		IO			AB19		
B8		IO			W18		
B8		IO			AC18		
B8		IO			Y18		
B8		IO			AF22		
B8		IO			AE21		
B8		IO			AD21		
B8		IO			AD20		
B8		IO			AF21		
B8		IO			AE20		
B8		IO			AB18		
B8		IO			V17		
B8		IO			AC17		
B8		IO			W17		
B8		IO			AF20		
B8		IO			AE19		
		NC (Note 3)			AA18		
B8		IO			AD19		
B8		IO			AD18		
B8		IO			AF19		
B8		IO			AE18		
B8		IO			Y17		
B8		IO			AB17		
B8		IO			V16		
B8		IO			AA17		
B8		IO			W16		
B8		IO			AF18		
B8		IO			AE17		
B8		IO			AD17		
B8		IO			AF17		
B8		IO			AD16		
B8		IO			AE16		
B8		IO			AA16		
B8		IO			V14		
B8		IO			W15		

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/DQ Group for DQS x4 Mode	Configuration Function for Stratix II Only (Note 1)	F672	DQ Group for DQS x8/x9 Mode	DQ Group for DQS x16/x18 Mode
		NC (Note 3)			AC16		
B8		IO			Y16		
B8		IO		RUnLU	Y15		
B8		IO	DEV_OE	DEV_OE	AA14		
B8		IO	DEV_CLRn	DEV_CLRn	AA15		
B8		IO		nCS	AB15		
B8		IO			AC15		
B8		IO			AB16		
B8		IO			AD15		
B8		IO	CLK5n		AB14		
B8		IO	CLK5p		AC14		
B8		IO	CLK4n		AE15		
B8		IO	CLK4p		AF15		
		GNDA_PLL6			W13		
		GNDA_PLL6			W14		
		VCCA_PLL6			Y13		
		VCCD_PLL6			Y14		
B10		VCC_PLL6_OUT			V13		
B7		IO	CLK7p		AC13		
B7		IO	CLK7n		AB13		
B7		IO	CLK6p		AE14		
B7		IO	CLK6n		AD14		
B10		IO	PLL6_OUT1p		AE13		
B10		IO	PLL6_OUT1n		AD13		
B10		IO	PLL6_OUT0p		AF12		
B10		IO	PLL6_OUT0n		AE12		
B10		IO	PLL6_FBp/OUT2p		AD12		
B10		IO	PLL6_FBn/OUT2n		AC12		
B7		IO			AE11		
B7		IO			AE10		
		NC (Note 3)			AC11		
B7		IO			AC10		
B7		IO			AF10		
B7		IO			AD11		
B7		IO			AD10		
B7		IO			Y12		
B7		IO			W12		
B7		IO			Y11		
B7		IO			AA12		
B7		IO			AF9		
B7		IO			AE9		
B7		IO			AD8		
B7		IO			AC8		
B7		IO			AC9		
B7		IO			AD9		
B7		IO			V12		
B7		IO			AA11		
B7		IO			W11		
B7		IO			AB12		
B7		IO			AF8		
B7		IO			AE8		
		NC (Note 3)			AA9		
B7		IO			AC7		
B7		IO			AD7		
B7		IO			AF7		
B7		IO			AE7		
B7		IO			Y10		
B7		IO			AB11		
B7		IO			Y9		
B7		IO			AA10		
B7		IO			AF6		
B7		IO			AE6		
B7		IO			AC6		
B7		IO			AE5		

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/DQ Group for DQS x4 Mode	Configuration Function for Stratix II Only (Note 1)	F672	DQ Group for DQS x8/x9 Mode	DQ Group for DQS x16/x18 Mode
B7		IO			AF5		
B7		IO			AD6		
B7		IO			W10		
B7		IO			W9		
B7		IO			AD5		
B7		IO			AE4		
		NC (Note 3)			AC5		
B7		IO			AD3		
B7		IO			AD4		
B7		IO			AF3		
B7		IO			AE3		
B7		IO			AB9		
B7		IO			AB10		
B7		IO			AA8		
B7		IO			AB8		
B7		IO			V10		
B7		IO			AB7		
B7		PORSEL		PORSEL	Y8		
B7		nIO_PULLUP		nIO_PULLUP	AE2		
B7		PLL_ENA		PLL_ENA	AB6		
		GND			AA7		
B7		nCEO		nCEO	AB5		
		NC (Note 3)			AC4		
B6		IO			Y7		
B6		IO			Y6		
B6		IO			AD2		
B6		IO			AD1		
B6		IO			AA6		
B6		IO			AA5		
B6		IO			AC3		
B6		IO			AC2		
B6		IO			W8		
B6		IO			W7		
B6		IO			AB4		
B6		IO			AB3		
B6		IO			W6		
B6		IO			W5		
B6		IO			AA4		
B6		IO			AA3		
		NC (Note 3)			Y5		
B6		IO			V8		
B6		IO			V7		
B6		IO			Y4		
B6		IO			Y3		
B6		IO			V6		
B6		IO			V5		
B6		IO			W4		
B6		IO			W3		
B6		IO			U8		
B6		IO			U7		
B6		IO			AB2		
B6		IO			AB1		
B6		IO			T7		
B6		IO			T6		
B6		IO			AA2		
B6		IO			AA1		
B6		IO			U6		
B6		IO			U5		
B6		IO			Y2		
B6		IO			Y1		
B6		IO			V4		
B6		IO			V3		
B6		IO			W2		
B6		IO			W1		

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/DQ Group for DQS x4 Mode	Configuration Function for Stratix II Only (Note 1)	F672	DQ Group for DQS x8/x9 Mode	DQ Group for DQS x16/x18 Mode
B6		IO			T9		
B6		IO			T8		
B6		IO			V2		
B6		IO			V1		
		NC (Note 3)			R5		
B6		IO			U4		
B6		IO			U3		
B6		IO			U2		
B6		IO			U1		
B6		IO			T5		
B6		IO			T4		
B6		IO			T3		
B6		IO			T2		
B6		CLK9n	INPUT		R4		
B6		CLK9p	INPUT		R3		
B6		IO	CLK8n		R2		
B6		IO	CLK8p		R1		
		NC (Note 4)			P7		
		NC (Note 5)			R6		
		NC (Note 6)			R7		
		NC (Note 6)			R8		
		NC (Note 6)			N8		
		NC (Note 6)			N9		
		NC (Note 5)			P8		
		NC (Note 4)			P9		
B5		CLK11p	INPUT		N2		
B5		CLK11n	INPUT		N3		
B5		IO	CLK10p		P2		
B5		IO	CLK10n		P3		
B5		IO			N7		
B5		IO			N6		
B5		IO			M2		
B5		IO			M1		
B5		IO			P5		
B5		IO			P4		
B5		IO			L3		
B5		IO			L2		
B5		IO			N5		
B5		IO			N4		
B5		IO			K2		
B5		IO			K1		
		NC (Note 3)			K5		
B5		IO			M6		
B5		IO			M5		
B5		IO			J2		
B5		IO			J1		
B5		IO			M8		
B5		IO			M7		
B5		IO			K4		
B5		IO			K3		
B5		IO			L9		
B5		IO			L8		
B5		IO			H2		
B5		IO			H1		
B5		IO			L7		
B5		IO			L6		
B5		IO			G2		
B5		IO			G1		
B5		IO			M4		
B5		IO			M3		
B5		IO			J4		
B5		IO			J3		
B5		IO			L5		
B5		IO			L4		

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/DQ Group for DQS x4 Mode	Configuration Function for Stratix II Only (Note 1)	F672	DQ Group for DQS x8/x9 Mode	DQ Group for DQS x16/x18 Mode
B5		IO			H4		
B5		IO			H3		
B5		IO			K9		
B5		IO			K8		
B5		IO			G4		
B5		IO			G3		
B5		IO			K7		
B5		IO			K6		
B5		IO			F4		
B5		IO			F3		
		NC (Note 3)			G5		
B5		IO			J8		
B5		IO			J7		
B5		IO			F2		
B5		IO			F1		
B5		IO			H8		
B5		IO			H7		
B5		IO			E4		
B5		IO			E3		
B5		IO			J6		
B5		IO			J5		
B5		IO			E2		
B5		IO			E1		
B5		IO			H6		
B5		IO			H5		
B5		IO			D3		
B5		IO			D2		
B5		IO			G7		
B5		IO			G6		
B5		IO			C2		
B5		IO			C1		
		NC (Note 3)			D4		
		TEMPDIODEp			E5		
		TEMPDIODEn			F5		
B4	VREFB4N0	TDO		TDO	F6		
		NC (Note 2)		MSEL3	F7		
		NC (Note 2)		MSEL2	E6		
		NC (Note 2)		MSEL1	B2		
		NC (Note 2)		MSEL0	G8		
B4	VREFB4N0	IO			J9		
B4	VREFB4N0	IO			F8		
B4	VREFB4N0	IO	RUP4		E7		
B4	VREFB4N0	IO	RDN4		E8		
B4	VREFB4N0	IO	DQS1T		B3		
B4	VREFB4N0	IO	DQ1T		A3		
B4	VREFB4N0	IO	DQ1T		C4		
B4	VREFB4N0	IO	DQ1T		C3		
B4	VREFB4N0	VREFB4N0	VREFB4N0		D5		
B4	VREFB4N0	IO	DQSn1T		B4		
B4	VREFB4N0	IO	DQ1T		C5		
B4	VREFB4N1	IO			E9		
B4	VREFB4N0	IO			K10		
B4	VREFB4N0	IO			H9		
B4	VREFB4N0	IO			G9		
B4	VREFB4N0	IO	DQS3T		C6	DQS0T	
B4	VREFB4N0	IO	DQ3T		A5	DQ0T	DQ0T
B4	VREFB4N0	IO	DQ3T		B5	DQ0T	DQ0T
B4	VREFB4N0	IO	DQ3T		D6	DQ0T	DQ0T
B4	VREFB4N1	IO	DQSn3T		B6	DQSn0T	DQ0T
B4	VREFB4N1	IO	DQ3T		A6	DQ0T	DQ0T
B4	VREFB4N0	IO			J10		
B4	VREFB4N1	IO			H10		
B4	VREFB4N1	IO			K11		
B4	VREFB4N1	IO			E10		

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/DQ Group for DQS x4 Mode	Configuration Function for Stratix II Only (Note 1)	F672	DQ Group for DQS x8/x9 Mode	DQ Group for DQS x16/x18 Mode
B4	VREFB4N1	IO			F10		
B4	VREFB4N1	IO	DQS5T		B7	DQVLD0T	DQS0T
B4	VREFB4N1	IO	DQ5T		A7	DQ0T	DQ0T
B4	VREFB4N1	IO	DQ5T		C7	DQ0T	DQ0T
B4	VREFB4N1	IO	DQ5T		D7	DQ0T	DQ0T
B4	VREFB4N1	VREFB4N1	VREFB4N1		F9		
B4	VREFB4N1	IO	DQSn5T		B8	DQ0T	DQSn0T
B4	VREFB4N1	IO	DQ5T		A8	DQ0T	DQ0T
B4	VREFB4N1	IO			G10		
B4	VREFB4N1	IO			J11		
B4	VREFB4N2	IO			E11		
B4	VREFB4N2	IO			F11		
B4	VREFB4N1	IO	DQS7T		C9	DQS1T	DQVLD0T
B4	VREFB4N1	IO	DQ7T		D9	DQ1T	DQ0T
B4	VREFB4N1	IO	DQ7T		D8	DQ1T	DQ0T
B4	VREFB4N1	IO	DQ7T		C8	DQ1T	DQ0T
B4	VREFB4N1	IO	DQSn7T		B9	DQSn1T	DQ0T
B4	VREFB4N2	IO	DQ7T		A9	DQ1T	DQ0T
B4	VREFB4N2	IO			E12		
B4	VREFB4N1	IO			G11		
B4	VREFB4N1	IO			H11		
B4	VREFB4N2	IO			F12		
B4	VREFB4N2	IO	DQS9T		C10	DQVLD1T	
B4	VREFB4N2	IO	DQ9T		C11	DQ1T	DQ0T
B4	VREFB4N2	IO	DQ9T		A10	DQ1T	DQ0T
B4	VREFB4N2	IO	DQ9T		D10	DQ1T	DQ0T
B4	VREFB4N2	VREFB4N2	VREFB4N2		D11		
B4	VREFB4N2	IO	DQSn9T		B10	DQ1T	DQ0T
B4	VREFB4N2	IO	DQ9T		B11	DQ1T	
B4	VREFB4N2	IO			F13		
B9	VREFB4N2	IO	PLL5_FBn/OUT2n		D12		
B9	VREFB4N2	IO	PLL5_FBp/OUT2p		C12		
B9	VREFB4N2	IO	PLL5_OUT0n		B12		
B9	VREFB4N2	IO	PLL5_OUT0p		A12		
B9	VREFB4N2	IO	PLL5_OUT1n		E13		
B9	VREFB4N2	IO	PLL5_OUT1p		D13		
B4	VREFB4N2	IO	CLK12n		C13		
B4	VREFB4N2	IO	CLK12p		B13		
B4	VREFB4N2	IO	CLK13n		C14		
B4	VREFB4N2	IO	CLK13p		B14		
B9		VCC_PLL5_OUT			H12		
		VCCD_PLL5			H14		
		VCCA_PLL5			G12		
		GNDA_PLL5			H13		
		GNDA_PLL5			J13		
B3	VREFB3N0	IO	CLK14p		A15		
B3	VREFB3N0	IO	CLK14n		B15		
B3	VREFB3N0	IO	CLK15p		C15		
B3	VREFB3N0	IO	CLK15n		D15		
B3	VREFB3N0	IO			D14		
B3	VREFB3N0	IO			J14		
B3	VREFB3N0	IO		PGM2	E15		
B3	VREFB3N0	IO		PGM1	F15		
B3	VREFB3N0	IO		PGM0	F14		
B3	VREFB3N0	IO		ASDO	G14		
B3	VREFB3N0	IO		nCSO	E14		
B3	VREFB3N0	IO		CRC_ERROR	F16		
B3	VREFB3N0	IO		DATA0	E16		
B3	VREFB3N0	IO		DATA1	G15		
B3	VREFB3N0	VREFB3N0	VREFB3N0		D16		
B3	VREFB3N1	IO			D17		
B3	VREFB3N0	IO			H15		
B3	VREFB3N1	IO			G16		
B3	VREFB3N0	IO			J15		

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/DQ Group for DQS x4 Mode	Configuration Function for Stratix II Only (Note 1)	F672	DQ Group for DQS x8/x9 Mode	DQ Group for DQS x16/x18 Mode
B3	VREFB3N0	IO	DQS11T		B16	DQS2T	
B3	VREFB3N0	IO	DQ11T		C16	DQ2T	DQ1T
B3	VREFB3N0	IO	DQ11T		A17	DQ2T	DQ1T
B3	VREFB3N0	IO	DQ11T		C17	DQ2T	DQ1T
B3	VREFB3N1	IO	DQSn11T		B17	DQSn2T	DQ1T
B3	VREFB3N1	IO	DQ11T		A18	DQ2T	DQ1T
B3	VREFB3N1	IO			H16		
B3	VREFB3N1	IO			F17		
B3	VREFB3N1	IO			K16		
B3	VREFB3N1	IO			G17		
B3	VREFB3N1	IO			H17		
B3	VREFB3N1	IO	DQS13T		B18	DQVLD2T	DQS1T
B3	VREFB3N1	IO	DQ13T		A19	DQ2T	DQ1T
B3	VREFB3N1	IO	DQ13T		C18	DQ2T	DQ1T
B3	VREFB3N1	IO	DQ13T		C19	DQ2T	DQ1T
B3	VREFB3N1	VREFB3N1	VREFB3N1		F18		
B3	VREFB3N1	IO	DQSn13T		B19	DQ2T	DQSn1T
B3	VREFB3N1	IO	DQ13T		A20	DQ2T	DQ1T
B3	VREFB3N1	IO			E17		
B3	VREFB3N2	IO			J17		
B3	VREFB3N1	IO			G18		
B3	VREFB3N2	IO			K17		
B3	VREFB3N1	IO	DQS15T		B20	DQS3T	DQVLD1T
B3	VREFB3N1	IO	DQ15T		A21	DQ3T	DQ1T
B3	VREFB3N1	IO	DQ15T		C20	DQ3T	DQ1T
B3	VREFB3N1	IO	DQ15T		C21	DQ3T	DQ1T
B3	VREFB3N2	IO	DQSn15T		B21	DQSn3T	DQ1T
B3	VREFB3N2	IO	DQ15T		A22	DQ3T	DQ1T
B3	VREFB3N1	IO			H18		
B3	VREFB3N1	IO			E18		
B3	VREFB3N2	IO			J18		
B3	VREFB3N1	IO			D18		
B3	VREFB3N2	IO	DQS17T		B23	DQVLD3T	
B3	VREFB3N2	IO	DQ17T		C22	DQ3T	DQ1T
B3	VREFB3N2	IO	DQ17T		B22	DQ3T	DQ1T
B3	VREFB3N2	IO	DQ17T		A24	DQ3T	DQ1T
B3	VREFB3N2	VREFB3N2	VREFB3N2		D22		
B3	VREFB3N2	IO	DQSn17T		C23	DQ3T	DQ1T
B3	VREFB3N2	IO	DQ17T		B24	DQ3T	
B3	VREFB3N2	IO			K18		
B3	VREFB3N2	IO		DATA2	E19		
B3	VREFB3N2	IO		DATA3	D20		
B3	VREFB3N2	IO		DATA4	G19		
B3	VREFB3N2	IO		DATA5	D19		
B3	VREFB3N2	IO		DATA6	E20		
B3	VREFB3N2	IO		DATA7	F20		
B3	VREFB3N2	IO		RDYnBSY	F19		
B3	VREFB3N2	IO	INIT_DONE	INIT_DONE	D21		
B3	VREFB3N2	nSTATUS		nSTATUS	E21		
B3	VREFB3N2	nCE		nCE	E22		
B3	VREFB3N2	DCLK		DCLK	C24		
B3	VREFB3N2	CONF_DONE		CONF_DONE	B25		
		VCCIO2			D26		
		VCCIO2			L26		
		VCCIO2			M17		
		VCCIO1			AC26		
		VCCIO1			P17		
		VCCIO1			T26		
		VCCIO8			AF16		
		VCCIO8			AF23		
		VCCIO8			U14		
		VCCIO7			AF4		
		VCCIO7			AF11		
		VCCIO7			U12		

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/DQ Group for DQS x4 Mode	Configuration Function for Stratix II Only (Note 1)	F672	DQ Group for DQS x8/x9 Mode	DQ Group for DQS x16/x18 Mode
		VCCIO6			AC1		
		VCCIO6			R10		
		VCCIO6			T1		
		VCCIO5			D1		
		VCCIO5			L1		
		VCCIO5			N10		
		VCCIO4			A4		
		VCCIO4			A11		
		VCCIO4			K13		
		VCCIO3			A16		
		VCCIO3			A23		
		VCCIO3			K15		
		VCCINT			L10		
		VCCINT			L12		
		VCCINT			L14		
		VCCINT			L16		
		VCCINT			M11		
		VCCINT			M13		
		VCCINT			M15		
		VCCINT			N12		
		VCCINT			N14		
		VCCINT			N16		
		VCCINT			P11		
		VCCINT			P13		
		VCCINT			P15		
		VCCINT			R12		
		VCCINT			R14		
		VCCINT			R16		
		VCCINT			T11		
		VCCINT			T13		
		VCCINT			T15		
		VCCINT			T17		
		VCCINT			U10		
		VCCINT			U16		
		VCCINT			U18		
		VCCINT			V9		
		GND			A2		
		GND			A13		
		GND			A14		
		GND			A25		
		GND			AA13		
		GND			AE1		
		GND			AE26		
		GND			AF2		
		GND			AF13		
		GND			AF14		
		GND			AF25		
		GND			B1		
		GND			B26		
		GND			G13		
		GND			K12		
		GND			K14		
		GND			L11		
		GND			L13		
		GND			L15		
		GND			L17		
		GND			M10		
		GND			M12		
		GND			M14		
		GND			M16		
		GND			N1		
		GND			N11		
		GND			N13		
		GND			N15		

Bank Number	VREF Group	Pin Name/Function	Optional Function(s)/DQ Group for DQS x4 Mode	Configuration Function for Stratix II Only (Note 1)	F672	DQ Group for DQS x8/x9 Mode	DQ Group for DQS x16/x18 Mode
		GND			N17		
		GND			N26		
		GND			P1		
		GND			P6		
		GND			P10		
		GND			P12		
		GND			P14		
		GND			P16		
		GND			P26		
		GND			R11		
		GND			R13		
		GND			R15		
		GND			R17		
		GND			R22		
		GND			T10		
		GND			T12		
		GND			T14		
		GND			T16		
		GND			T18		
		GND			U9		
		GND			U11		
		GND			U13		
		GND			U15		
		GND			U17		
		VCCPD2			M18		
		VCCPD1			R18		
		VCCPD8			V15		
		VCCPD7			V11		
		VCCPD6			R9		
		VCCPD5			M9		
		VCCPD4			J12		
		VCCPD3			J16		

Notes on Pin Table:

(1) These pins should be connected on the board to properly configure the FPGA prototype. See Stratix II device pin table for details.

(2) These NO CONNECT (NC) pins are MSEL configuration input pins in the Stratix II device and should be connected on the board to configure the FPGA prototype.

(3) This NC pin is a VREF pin in the Stratix II device and should be connected to the VREF input reference voltage for the FPGA prototype. If the VREF is not used, connect pin to VCC or GND.

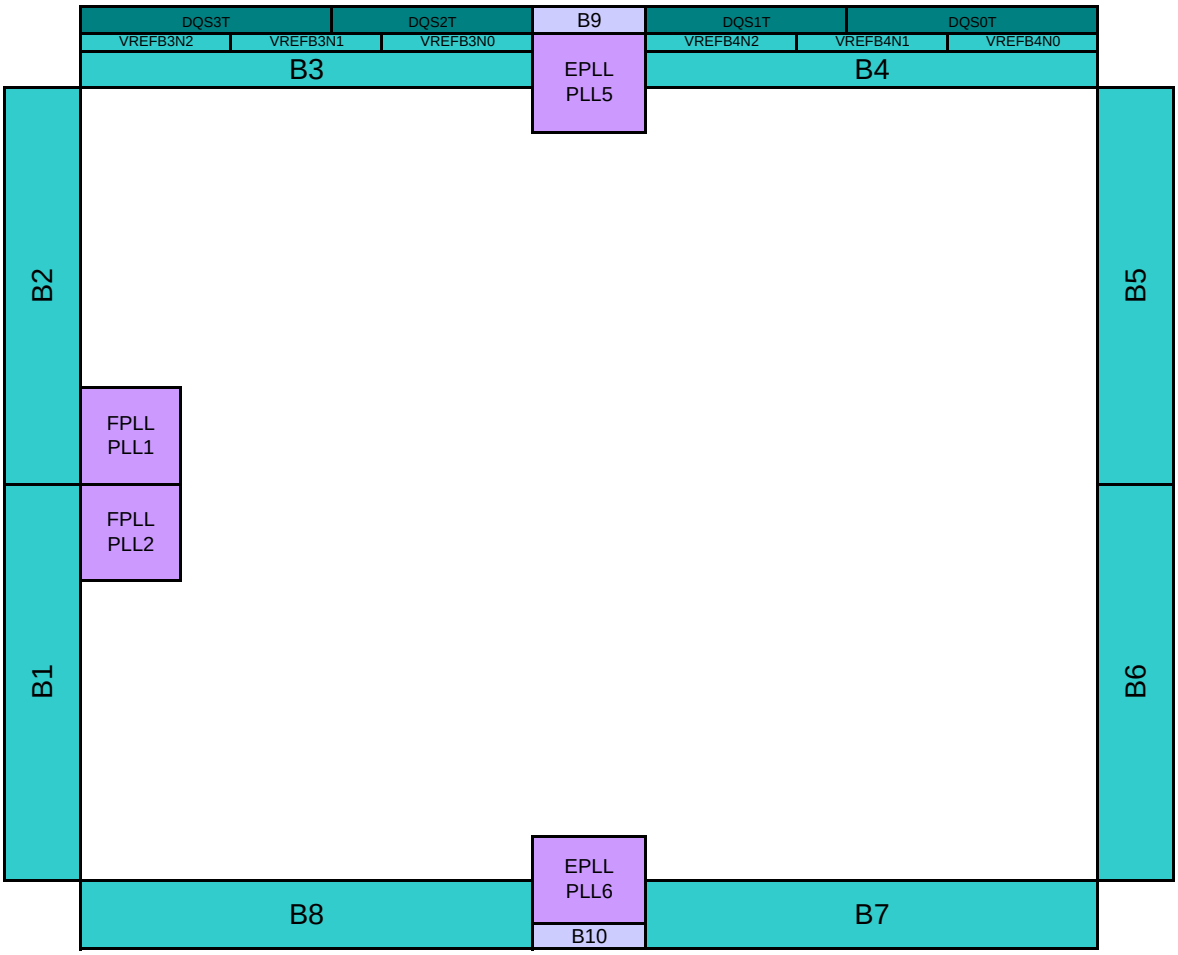
(4) This NC pin is a VCCD_PLL pin in the Stratix II device and should be connected to the VCCD_PLL power for the FPGA prototype.

(5) This NC pin is a VCCA_PLL pin in the Stratix II device and should be connected to the VCCA_PLL power for the FPGA prototype.

(6) This NC pin is a GNDA_PLL pin in the Stratix II device and should be connected to the GNDA_PLL ground for the FPGA prototype.

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
	Supply and Reference Pins	
VCCINT	Power	These are internal logic array voltage supply pins. VCCINT also supplies power to the input buffers used for the LVDS, LVPECL, HyperTransport™ technology, differential HSTL, differential SSTL, HSTL, and SSTL I/O standards. All VCCINT pins must be connected to 1.2 V.
VCCIO[1..8]	Power	These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all I/O standards including TDO and nCEO. VCCIO also supplies power to the input buffers used for the LVTTL, LVCMOS, 1.5 V, 1.8 V, 2.5 V, 3.3-V PCI, and 3.3-V PCI-X I/O standards.
VCCPD[1..8]	Power	Dedicated power pins. This supply is used to power the I/O pre-drivers and the 3.3-V/2.5-V buffers of the configuration input pins and JTAG pins. VCCPD powers all the JTAG pins (TCK, TMS, TDI, and TRST) and the following configuration pins: nCONFIG, DCLK (when used as an input), nIO_Pullup, and nCE. The VCCPD pins must be connected to 3.3 V and must ramp-up from 0 V to 3.3 V within 100 ms to ensure successful configuration.
GND	Ground	Device ground pins. All GND pins should be connected to the board GND plane.
VREFB[3..4]N[0..2]	Input	Input reference voltage for each I/O bank. If a bank is used for a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for that bank. All the VREF pins within a bank are shorted togetherIf VREF pins are not used, designers should connect them to either VCC or GND.
VCC_PLL5_OUT	Power	External clock output VCCIO power for PLL5 clock outputs PLL5_OUT[1..0]p, PLL5_OUT[1..0]n, PLL5_FBp/OUT2p & PLL5_FBn/OUT2n. This pin should be connected to the VCCIO level of bank 9.
VCC_PLL6_OUT	Power	External clock output VCCIO power for PLL6 clock outputs PLL6_OUT[1..0]p, PLL6_OUT[1..0]n, PLL6_FBp/OUT2p & PLL6_FBn/OUT2n. This pin should be connected to the VCCIO level of bank 10.
VCCA_PLL[1,2,5,6]	Power	Analog power for PLLs[1,2,5,6]. The designer must connect these pins to 1.2 V, even if the PLL is not used.
VCCD_PLL[1,2,5,6]	Power	Digital power for PLLs[1,2,5,6]. The designer must connect these pins to 1.2 V, even if the PLL is not used.
GNDA_PLL[1,2,5,6]	Ground	Analog ground for PLLs[1,2,5,6]. All analog GND pins should be connected to the board analog GND plane.
NC	No Connect	Do not drive signals into these pins. Exceptions are the configuration pins and the pins noted in this pin list. These pins should be properly connected on the board when prototyping with the Stratix II FPGA device. Make sure to check the pin out information for the Stratix II FPGA prototype compiled design when laying out the board to ensure compatibility between the HardCopy II device and the Stratix II FPGA prototype device.
RUP4	I/O, Input	Reference pin for banks 3 & 4. The external precision resistor Rup must be connected to the designated RUP pin within bank 4. If not required, this pin is a regular I/O pin.
RDN4	I/O, Input	Reference pin for banks 3 & 4. The external precision resistor Rdn must be connected to the designated RDN pin within bank 4. If not required, this pin is a regular I/O pin.
	Dedicated Configuration/JTAG Pins	
nIO_PULLUP	Input	Dedicated input that chooses whether the internal pull-ups on the user I/O pins and dual-purpose I/O pins (INIT_DONE, DEV_OE, DEV_CLRn) are on or off before and during power up. A logic high (1.5 V, 1.8 V, 2.5 V, or 3.3 V) turns off the weak pull-up, while a logic low turns them on.
VCCSEL	Input	Dedicated input that selects which input buffer is used on configuration input pins: nCONFIG, DCLK (when used as an input) and nCE. The 3.3-V/2.5-V input buffer is powered by VCCPD, while the 1.8-V/1.5-V input buffer is powered by VCCIO. The VCCSEL input buffer is powered by VCCPD and must be hardwired to VCCPD or ground. A logic high (VCCPD) selects the 1.8-V/1.5-V input buffer, while a logic low selects the 3.3-V/2.5-V input buffer. VCCSEL should be set to comply with the logic levels driven out of the configuration device or MAX II device/microprocessor with flash memory.
TEMPDIODEp	Input	Pin used in conjunction with the temperature sensing diode (bias-high input) inside the HardCopy II device. If the temperature sensing diode is not used then connect this pin to GND.
TEMPDIODEn	Input	Pin used in conjunction with the temperature sensing diode (bias-low input) inside the HardCopy II device. If the temperature sensing diode is not used then connect this pin to GND.
DCLK	Input	Dedicated configuration clock pin on Stratix II devices, but kept in HardCopy II for compatibility reasons. It's not required to clock this pin for HardCopy II.
nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled. In multi-device configuration, nCE of the first device is tied low while its nCEO pin drives the nCE of the next device in the chain. In single device configuration, nCE is tied low.
nCONFIG	Input	Dedicated power up block control input. Pulling this pin low during user-mode will cause the HardCopy II to enter a reset state & tri-state all I/O pins. Returning this pin to a logic high level will initiate the power up and initialization sequence. It is not available as a user I/O pin.
CONF_DONE	Bidirectional (open-drain)	This is a dedicated power up block status pin. As a status output, the CONF_DONE pin drives low before and during initialization. Once the power up delays are done and the initialization cycle starts, CONF_DONE is released. It is not available as a user I/O pin.
nCEO	Output	Output that drives low when device initialization is complete. During multi-device configuration, this pin feeds a subsequent device's nCE pin. During single device configuration, this pin is left floating.
nSTATUS	Bidirectional (open-drain)	This is a dedicated power up block status pin. The HardCopy II drives nSTATUS low immediately after power-up and releases it after POR time. As a status output, the nSTATUS is pulled low if an error occurs during initialization. As a status input, the device enters an error state when nSTATUS is driven low by an external source during initialization. It is not available as a user I/O pin.
PORSEL	Input	Dedicated input which selects between a POR time of 12 ms or 100 ms. A logic high (1.5-V, 1.8-V, 2.5-V, 3.3-V) selects a POR time of about 12 ms and a logic low selects POR time of about 100 ms. This is in addition to the Instant On delay mode chosen (i.e. instant or additional 50 ms).
TCK	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TCK to GND.
TMS	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TMS to VCC.
TDI	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TDI to VCC.
TDO	Output	Dedicated JTAG output pin. The JTAG circuitry can be disabled by leaving TDO unconnected.

Pin Name	Pin Type (1st, 2nd, & 3rd Function)	Pin Description
TRST	Input	Dedicated active low JTAG input pin. TRST is used to asynchronously reset the JTAG boundary-scan circuit. The JTAG circuitry can be disabled by connecting TRST to GND.
Clock and PLL Pins		
CLK[1,3,9,11]p	Clock, Input	Dedicated clock input pins 1, 3, 9, & 11 that can also be used for data inputs.
CLK[1,3,9,11]n	Clock, Input	Dedicated negative terminal clock input pins for differential clock input that can also be used for data inputs.
CLK[0,2]p/DIFFIO_RX_C[0,1]p	I/O, Clock, RX channel	These pins can be used as I/O pins, clock input pins, or the positive terminal data pins of differential receiver channels.
CLK[0,2]n/DIFFIO_RX_C[0,1]n	I/O, Clock, RX channel	These pins can be used as I/O pins, the negative terminal clock input pins for differential clock input, or the negative terminal data pins of differential receiver channels.
CLK[4-8,10,12-15]p	I/O, Clock	These pins can be used as I/O pins or clock input pins.
CLK[4-8,10,12-15]n	I/O, Clock	These pins can be used as I/O pins or negative terminal clock input pins for differential clock input.
PLL_ENA	Input	Dedicated input pin that drives the optional pllena port of all or a set of PLLs. If a PLL uses the pllena port, drive the PLL_ENA pin low to reset all PLLs including the counters to their default state. If VCCSEL = 0, then you mus drive the PLL_ENA with a 3.3/2.5 V signal to enable the PLLs. If VCCSEL = 1, connect PLL_ENA to 1.8/1.5 V to enable the PLLs.
PLL5_OUT[0..1]p	I/O, Output	Optional external clock outputs [0..1] from enhanced PLL 5. These pins can be differential (two output pin pairs) or single ended (four clock outputs from PLL5).
PLL5_OUT[0..1]n	I/O, Output	Optional negative terminal for external clock outputs [0..1] from PLL5. If the clock outputs are single ended, then each pair of pins (i.e., PLL5_OUT0p and PLL5_OUT0n are considered one pair) can be either in phase or 180 degrees out of phase.
PLL6_OUT[0..1]p	I/O, Output	Optional external clock outputs [0..1] from enhanced PLL 6. These pins can be differential (two output pin pairs) or single ended (four clock outputs from PLL6).
PLL6_OUT[0..1]n	I/O, Output	Optional negative terminal for external clock outputs [0..1] from PLL6. If the clock outputs are single ended, then each pair of pins (i.e., PLL6_OUT0p and PLL6_OUT0n are considered one pair) can be either in phase or 180 degrees out of phase.
PLL[5..6]_FBp/OUT2p	I/O, Input, Output	These pins can be used as I/O pins, external feedback input pins or external clock outputs for PLL[5..6].
PLL[5..6]_FBn/OUT2n	I/O, Input, Output	These pins can be used as I/O pins, negative terminal input for external feedback input PLL[5..6]_FBp or negative terminal clock output pins for differential clock output.
Optional/Dual-Purpose Configuration Pins		
DEV_CLRn	I/O, Input	Optional pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as programmed.
DEV_OE	I/O, Input	Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design.
INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high at the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration.
Dual-Purpose Differential & External Memory Interface Pins		
DIFFIO_RX[8..36]p/n	I/O, RX channel	Dual-purpose differential receiver channels. These channels can be used for receiving LVDS or HyperTransport compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFIO_TX[8..36]p/n	I/O, TX channel	Dual-purpose differential transmitter channels. These channels can be used for transmitting LVDS or HyperTransport compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. Pin with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DQS[0..1]T (x16/x18) DQS[0..3]T (x8/x9) DQS[1,3,5,7,9,11,13,15,17]T (x4)	I/O, DQS	Optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry. The shifted DQS signal can also drive to internal logic.
DQSn[0..1]T (x16/x18) DQSn[0..3]T (x8/x9) DQSn[1,3,5,7,9,11,13,15,17]T (x4)	I/O, DQSn	Optional complementary data strobe signal for use in QDRII SRAM. These pins drive to dedicated DQS phase shift circuitry.
DQ[0..1]T (x16/x18) DQ[0..3]T (x8/x9) DQ[1,3,5,7,9,11,13,15,17]T (x4)	I/O, DQ	Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important; however, use caution when making pin assignments if you plan on migrating to a different memory interface that has a different DQ bus width. Analyze the available DQ pins across all pertinent DQS columns in the pin list.
DQVLD[0..1]T (x16/x18) DQVLD[0..3]T (x8/x9)	I/O, DQVLD	Optional data valid signal for use in external memory interfacing.



Notes:

1. This is a top view of the silicon die. For flip chip packages, the die is mounted upside down in the package; therefore, to obtain the top package view, flip this diagram on its vertical axis.
2. This is a pictorial representation only to get an idea of placement on the device. Refer to the pin list and the Quartus® II software for exact locations.
3. The DQ/DQS groups depicted above are in x8/x9 mode. DQ/DQS support differs across the package offerings.

Version Number	Date	Changes Made
Preliminary	3/16/2005	
1.0	9/1/2005	Pintable updated to match latest Engineering pintable released 8/10/05. This pintable is compatible with Quartus II Version 5.1
1.1	3/27/2007	Pintable updated to match latest Engineering pintable released 12/13/05.
		Added configuration function column for FPGA prototyping in the pin list.
		Added "DQ Group for DQS x4 Mode" description to the "Optional Function(s)" header in the pin list.
		Added footnotes in the pin list to describe the HardCopy II pins that have functions which differ from the Stratix II.
		Updated PLL numbers for VCCA_PLL, VCCD_PLL, and GNDA_PLL in the pin definition.
		Added more NC pin definition details for the configuration and noted pins.
		Updated CLK[ ]p/n DIFFIO_RX_C[ ]p/n numbers in the pin definition.
		Updated DIFFIO_RX/TX channel numbers in the pin definition.
		Updated DQS, DQSn, DQ, and DQVLD pin numbers in the pin definition.