Pin Information for the MAX®10 10M25SC Device
Version 2017.02.21
Note *(1)*

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	E144 *(2)*
1A	VREFB1N0	IO			DIFFIO_RX_L1n	DIFFOUT_L1n	Low_Speed	6
1A	VREFB1N0	IO			DIFFIO_RX_L1p	DIFFOUT_L1p	Low_Speed	7
1A	VREFB1N0	IO			DIFFIO_RX_L3n	DIFFOUT_L3n	Low_Speed	8
1A	VREFB1N0	IO			DIFFIO_RX_L3p	DIFFOUT_L3p	Low_Speed	10
1A	VREFB1N0	IO			DIFFIO_RX_L5n	DIFFOUT_L5n	Low_Speed	11
1A	VREFB1N0	IO			DIFFIO_RX_L5p	DIFFOUT_L5p	Low_Speed	12
1A	VREFB1N0	IO			DIFFIO_RX_L7n	DIFFOUT_L7n	Low_Speed	13
1A	VREFB1N0	IO			DIFFIO_RX_L7p	DIFFOUT_L7p	Low_Speed	14
1B	VREFB1N0	IO		JTAGEN				15
1B	VREFB1N0	IO		TMS	DIFFIO_RX_L11n	DIFFOUT_L11n	Low_Speed	16
1B	VREFB1N0	IO	VREFB1N0					17
1B	VREFB1N0	IO		TCK	DIFFIO_RX_L11p	DIFFOUT_L11p	Low_Speed	18
1B	VREFB1N0	IO		TDI	DIFFIO_RX_L12n	DIFFOUT_L12n	Low_Speed	19
1B	VREFB1N0	IO		TDO	DIFFIO_RX_L12p	DIFFOUT_L12p	Low_Speed	20
1B	VREFB1N0	IO			DIFFIO_RX_L14n	DIFFOUT_L14n	Low_Speed	21
1B	VREFB1N0	IO			DIFFIO_RX_L14p	DIFFOUT_L14p	Low_Speed	22
1B	VREFB1N0	IO			DIFFIO_RX_L16n	DIFFOUT_L16n	Low_Speed	24
1B	VREFB1N0	IO			DIFFIO_RX_L16p	DIFFOUT_L16p	Low_Speed	25
2	VREFB2N0	IO	CLK0n		DIFFIO_RX_L20n	DIFFOUT_L20n	High_Speed	26
2	VREFB2N0	IO	CLK0p		DIFFIO_RX_L20p	DIFFOUT_L20p	High_Speed	27
2	VREFB2N0	IO	CLK1n		DIFFIO_RX_L22n	DIFFOUT_L22n	High_Speed	28
2	VREFB2N0	IO	CLK1p		DIFFIO_RX_L22p	DIFFOUT_L22p	High_Speed	29
2	VREFB2N0	IO	VREFB2N0					30
2	VREFB2N0	IO	PLL_L_CLKOUTn		DIFFIO_RX_L35n	DIFFOUT_L35n	High_Speed	32
2	VREFB2N0	IO	PLL_L_CLKOUTp		DIFFIO_RX_L35p	DIFFOUT_L35p	High_Speed	33
3	VREFB3N0	IO			DIFFIO_TX_RX_B1n	DIFFOUT_B1n	High_Speed	38
3	VREFB3N0	IO			DIFFIO_TX_RX_B1p	DIFFOUT_B1p	High_Speed	39
3	VREFB3N0	IO			DIFFIO_TX_RX_B3n	DIFFOUT_B3n	High_Speed	41
3	VREFB3N0	IO			DIFFIO_TX_RX_B3p	DIFFOUT_B3p	High_Speed	43
3	VREFB3N0	IO			DIFFIO_TX_RX_B5n	DIFFOUT_B5n	High_Speed	44
3	VREFB3N0	IO			DIFFIO_TX_RX_B5p	DIFFOUT_B5p	High_Speed	45
3	VREFB3N0	IO			DIFFIO_TX_RX_B13n	DIFFOUT_B13n	High_Speed	46
3	VREFB3N0	IO			DIFFIO_TX_RX_B13p	DIFFOUT_B13p	High_Speed	47
3	VREFB3N0	IO			DIFFIO_TX_RX_B15n	DIFFOUT_B15n	High_Speed	50
3	VREFB3N0	IO	VREFB3N0					48
3	VREFB3N0	IO			DIFFIO_TX_RX_B15p	DIFFOUT_B15p	High_Speed	52
3	VREFB3N0	IO						54
3	VREFB3N0	IO	CLK6n		DIFFIO_TX_RX_B18n	DIFFOUT_B18n	High_Speed	55
3	VREFB3N0	IO	CLK6p		DIFFIO_TX_RX_B18p	DIFFOUT_B18p	High_Speed	56
3	VREFB3N0	IO	CLK7n		DIFFIO_TX_RX_B20n	DIFFOUT_B20n	High_Speed	57
3	VREFB3N0	IO	CLK7p		DIFFIO_TX_RX_B20p	DIFFOUT_B20p	High_Speed	58
3	VREFB3N0	IO			DIFFIO_TX_RX_B22n	DIFFOUT_B22n	High_Speed	59
3	VREFB3N0	IO			DIFFIO_TX_RX_B22p	DIFFOUT_B22p	High_Speed	60
4	VREFB4N0	IO	VREFB4N0					61
4	VREFB4N0	IO						62
4	VREFB4N0	IO			DIFFIO_TX_RX_B35n	DIFFOUT_B35n	High_Speed	64
4	VREFB4N0	IO			DIFFIO_TX_RX_B35p	DIFFOUT_B35p	High_Speed	65
4	VREFB4N0	IO						66
4	VREFB4N0	IO			DIFFIO_TX_RX_B49n	DIFFOUT_B49n	High_Speed	69
4	VREFB4N0	IO			DIFFIO_TX_RX_B49p	DIFFOUT_B49p	High_Speed	70
5	VREFB5N0	IO	RUP		DIFFIO_RX_R1p	DIFFOUT_R1p	High_Speed	75
5	VREFB5N0	IO			DIFFIO_RX_R2p	DIFFOUT_R2p	High_Speed	74
5	VREFB5N0	IO	RDN		DIFFIO_RX_R1n	DIFFOUT_R1n	High_Speed	77
5	VREFB5N0	IO			DIFFIO_RX_R2n	DIFFOUT_R2n	High_Speed	76
5	VREFB5N0	IO			DIFFIO_RX_R13p	DIFFOUT_R13p	High_Speed	79
5	VREFB5N0	IO						78
5	VREFB5N0	IO			DIFFIO_RX_R13n	DIFFOUT_R13n	High_Speed	81
5	VREFB5N0	IO	VREFB5N0					80
5	VREFB5N0	IO			DIFFIO_RX_R16p	DIFFOUT_R16p	High_Speed	85
5	VREFB5N0	IO			DIFFIO_RX_R17p	DIFFOUT_R17p	High_Speed	84
5	VREFB5N0	IO			DIFFIO_RX_R16n	DIFFOUT_R16n	High_Speed	87
5	VREFB5N0	IO			DIFFIO_RX_R17n	DIFFOUT_R17n	High_Speed	86
6	VREFB6N0	IO	CLK2p		DIFFIO_RX_R20p	DIFFOUT_R20p	High_Speed	88
6	VREFB6N0	IO	CLK2n		DIFFIO_RX_R20n	DIFFOUT_R20n	High_Speed	89
6	VREFB6N0	IO	CLK3p		DIFFIO_RX_R22p	DIFFOUT_R22p	High_Speed	90
6	VREFB6N0	IO	CLK3n		DIFFIO_RX_R22n	DIFFOUT_R22n	High_Speed	91
6	VREFB6N0	IO			DIFFIO_RX_R24p	DIFFOUT_R24p	High_Speed	92
6	VREFB6N0	IO			DIFFIO_RX_R24n	DIFFOUT_R24n	High_Speed	93
6	VREFB6N0	IO	DPCLK3		DIFFIO_RX_R32p	DIFFOUT_R32p	High_Speed	96
6	VREFB6N0	IO	VREFB6N0					97
6	VREFB6N0	IO	DPCLK2		DIFFIO_RX_R32n	DIFFOUT_R32n	High_Speed	98
6	VREFB6N0	IO			DIFFIO_RX_R33p	DIFFOUT_R33p	High_Speed	99
6	VREFB6N0	IO			DIFFIO_RX_R34p	DIFFOUT_R34p	High_Speed	100
6	VREFB6N0	IO			DIFFIO_RX_R33n	DIFFOUT_R33n	High_Speed	101
6	VREFB6N0	IO			DIFFIO_RX_R34n	DIFFOUT_R34n	High_Speed	102
6	VREFB6N0	IO			DIFFIO_RX_R47p	DIFFOUT_R47p	High_Speed	105
6	VREFB6N0	IO			DIFFIO_RX_R47n	DIFFOUT_R47n	High_Speed	106
7	VREFB7N0	IO			DIFFIO_RX_T1p	DIFFOUT_T1p	High_Speed	110
7	VREFB7N0	IO			DIFFIO_RX_T1n	DIFFOUT_T1n	High_Speed	111
7	VREFB7N0	IO	VREFB7N0					112
7	VREFB7N0	IO						113
7	VREFB7N0	IO						114
7	VREFB7N0	IO			DIFFIO_RX_T30p	DIFFOUT_T30p	High_Speed	118
7	VREFB7N0	IO			DIFFIO_RX_T30n	DIFFOUT_T30n	High_Speed	119
8	VREFB8N0	IO			DIFFIO_RX_T36p	DIFFOUT_T36p	Low_Speed	120
8	VREFB8N0	IO		DEV_CLRn	DIFFIO_RX_T36n	DIFFOUT_T36n	Low_Speed	121
8	VREFB8N0	IO		DEV_OE				122
8	VREFB8N0	IO	VREFB8N0					123
8	VREFB8N0	IO		CONFIG_SEL				126
8	VREFB8N0	IO			DIFFIO_RX_T39p	DIFFOUT_T39p	Low_Speed	124
8	VREFB8N0	Input_only		nCONFIG				129

Bank Number	VREF	Pin Name/Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	IO Performance	E144 *(2)*
8	VREFB8N0	IO			DIFFIO_RX_T39n	DIFFOUT_T39n	Low_Speed	127
8	VREFB8N0	IO			DIFFIO_RX_T40p	DIFFOUT_T40p	Low_Speed	130
8	VREFB8N0	IO			DIFFIO_RX_T40n	DIFFOUT_T40n	Low_Speed	131
8	VREFB8N0	IO			DIFFIO_RX_T42p	DIFFOUT_T42p	Low_Speed	132
8	VREFB8N0	IO		CRC_ERROR	DIFFIO_RX_T42n	DIFFOUT_T42n	Low_Speed	134
8	VREFB8N0	IO						135
8	VREFB8N0	IO		nSTATUS	DIFFIO_RX_T44p	DIFFOUT_T44p	Low_Speed	136
8	VREFB8N0	IO		CONF_DONE	DIFFIO_RX_T44n	DIFFOUT_T44n	Low_Speed	138
8	VREFB8N0	IO			DIFFIO_RX_T46p	DIFFOUT_T46p	Low_Speed	140
8	VREFB8N0	IO			DIFFIO_RX_T46n	DIFFOUT_T46n	Low_Speed	141
		GND						3
		GND						4
		GND						95
		GND						83
		GND						68
		GND						63
		GND						53
		GND						42
		GND						142
		GND						137
		GND						133
		GND						125
		GND						116
		GND						104
		VCCIO1A						9
		VCCIO1B						23
		VCCIO2						31
		VCCIO3						49
		VCCIO3						40
		VCCIO4						67
		VCCIO5						82
		VCCIO6						94
		VCCIO6						103
		VCCIO7						117
		VCCIO8						139
		VCCIO8						128
		VCCA1						35
		VCCA2						34
		VCCA3						5
		VCCA3						107
		VCCA4						143
		VCCA5						71
		VCCA6						2
		VCC_ONE						73
		VCC_ONE						72
		VCC_ONE						51
		VCC_ONE						37
		VCC_ONE						36
		VCC_ONE						144
		VCC_ONE						115
		VCC_ONE						109
		VCC_ONE						108
		VCC_ONE						1

Notes:

(1) For more information about pin definition and pin connection guidelines, refer to the
MAX 10 FPGA Device Family Pin Connection Guidelines.

(2) The E144-pin package has an exposed ground pad at the bottom of the package. The exposed ground pad is used for electrical connectivity and not for thermal purposes. You must connect the exposed ground pad to the ground plane of the PCB.

Date	Version	Changes Made
April 2015	2015.04.07	Initial release.
December 2016	2016.12.23	Removed I/O performance for single-ended pins.
February 2017	2017.02.21	Rebranded as Intel.