Dedicated Pin Information for the MAX® IIZ EPM240Z Devices Version 1.0

Dedicated Pin	68-Pin MBGA	100-Pin MBGA
IO/GCLK0	E2	F2
IO/GCLK1	E1	E1
IO/GCLK2	E9	F10
IO/GCLK3	E8	G11
IO/DEV_OE	J6	L8
IO/DEV_CLRn	H7	K8
TDI	H1	J2
TMS	G1	J1
TCK	J1	K1
TDO	H2	K2
GND*(3)*	C5, E3, E7,G5,C6	E4, G4, H5, H7, G8, E8, D7, D5
VCCINT *(1)*	D7	G3, E9
VCCIO1 *(2)*	D3, G4	E3, J4, J8
VCCIO2 *(2)*	C4, F7	G9, C8, C4
No Connect (N.C.)	-	-
Total User I/O Pins	54	80

Notes:
(1) All VCCINT pins must be connected to 1.8 V.
(2) Each set of VCCIO pins (VCCIO1 or VCCIO2) can be connected to 3.3 V, 2.5 V, 1.8 V, or 1.5 V.
(3) MAX II and MAX IIG devices separate out I/O ground (GNDIO) and core ground (GNDINT), but MAX IIZ devices unify ground to GND only.

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Bank Number	Pad Number Orientation	Pin/Pad Function	Optional Function(s)	68-Pin MBGA	100-Pin MBGA
B1	0	IO			B1
B1	1	IO		A1	C2
B1	2	IO		B1	C1
B1	3	IO		C1	D3
B1	4	IO		C2	D2
B1	5	IO		D1	D1
B1	6	IO		D2	E2
B1	7	VCCIO1			
B1	8	GND			
	9	GND			
B1	10	IO	GCLK0	E2	F2
	11	VCCINT			
B1	12	IO	GCLK1	E1	E1
B1	13	IO			F1
B1	14	IO			G1
B1	15	IO		F1	G2
B1	16	IO			F3
B1	17	IO		F2	H1
B1	18	IO		F3	H3
B1	19	IO		G2	H2
B1	20	TMS		G1	J1
B1	21	TDI		H1	J2
B1	22	TCK		J1	K1
B1	24	TDO		H2	K2
B1	25	IO		J2	L1
B1	26	IO		H3	L2
B1	27	IO		J3	K3
B1	28	IO		H4	L3
B1	29	IO		J4	K4
B1	30	VCCIO1			
B1	31	GND			
B1	32	IO		H5	L4
B1	33	IO		J5	K5
B1	34	IO			L5
B1	35	IO			L6
B1	36	IO			J5
B1	37	IO			K6
B1	38	IO			J7
B1	39	IO			J6
B1	40	IO		G6	L7
B1	41	IO		H6	K7
B1	42	IO	DEV_OE	J6	L8
B1	43	IO	DEV_CLRn	H7	K8
B1	44	VCCIO1			
B1	45	GND			
B1	46	IO		J7	L9
B1	47	IO		H8	K9
B1	48	IO		J8	L10
B1	49	IO		J9	K10
B1	50	IO			L11
B2	51	IO		H9	K11
B2	52	IO		G9	J10
B2	53	IO		G8	J11
B2	54	IO		F8	H9
B2	55	IO			H10
B2	56	IO		F9	H11
B2	57	IO			G10
B2	58	VCCIO2			

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Bank Number	Pad Number Orientation	Pin/Pad Function	Optional Function(s)	68-Pin MBGA	100-Pin MBGA
B2	59	GND			
B2	60	IO			F9
B2	61	IO	GCLK2	E9	F10
	62	VCCINT			
B2	63	IO	GCLK3	E8	G11
	64	GND			
B2	65	IO			F11
B2	66	IO			E11
B2	67	IO		D9	E10
B2	68	IO		C9	D9
B2	69	IO		D8	D11
B2	70	IO		C8	D10
B2	71	IO		B9	C11
B2	72	IO		A9	C10
B2	73	IO			B11
B2	74	IO			B10
B2	75	IO			A11
B2	76	IO			A10
B2	77	IO			B9
B2	78	GND			
B2	79	VCCIO2			
B2	80	IO			A9
B2	81	IO			B8
B2	82	IO		A8	A8
B2	83	IO		B8	B7
B2	84	IO		A7	A7
B2	85	IO		A6	C6
B2	86	IO		B7	B6
B2	87	IO			C7
B2	88	IO		B6	A6
B2	89	IO			C5
B2	90	IO		B5	A5
B2	91	IO		A5	B5
B2	92	GND			
B2	93	VCCIO2			
B2	94	IO		B4	A4
B2	95	IO		A4	B4
B2	96	IO		B3	A3
B2	97	IO		A3	B3
B2	98	IO		B2	A2
B2	99	IO		A2	B2
B2	100	IO			A1

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Pin Name	Pin Type	Pin Description
		Supply and Reference pins
VCCIO[1..2]	Power	I/O supply voltage pins for banks 1 through 2 respectively. Each VCCIO bank supports a different voltage level with the VCCIO pins providing power for the input and output buffers within that particular I/O bank. Each VCCIO bank can be powered with either 3.3 V, 2.5 V, 1.8 V, or 1.5 V.
GND*(1)*	Ground	Device ground pins. Ground pins for all the I/O banks and internal supply. All GND pins should be connected to the board GND plane.
VCCINT	Power	Voltage supply pins for the device.
		Programming and JTAG pins
DEV_CLRn	I/O	Dual-purpose pin that can override all clears on all device registers. All registers are cleared when the pin is driven low and all registers behave as defined in the design when this pin is driven high. If not used for its dual-purpose function, this pin is a regular I/O.
DEV_OE	I/O	Dual-purpose pin that can override all tri-states on the device. All output pins are tristated when the pin is driven low and all output pins behave as defined in the design when this pin is driven high. If not used for its dual-purpose function, this pin is a regular I/O.
TCK	Input	Dedicated JTAG input pin.
TDI	Input	Dedicated JTAG input pin.
TMS	Input	Dedicated JTAG input pin.
TDO	Output	Dedicated JTAG output pin.
		Clock Pins
GCLK [0..3]	I/O	Dual-purpose clock pins that connect to the global clock network. If not used for its dual-purpose function, this pin is a regular I/O.

Note:
(1) MAX II and MAX IIG devices separate out I/O ground (GNDIO) and core ground (GNDINT), but MAX IIZ devices unify ground to GND only.

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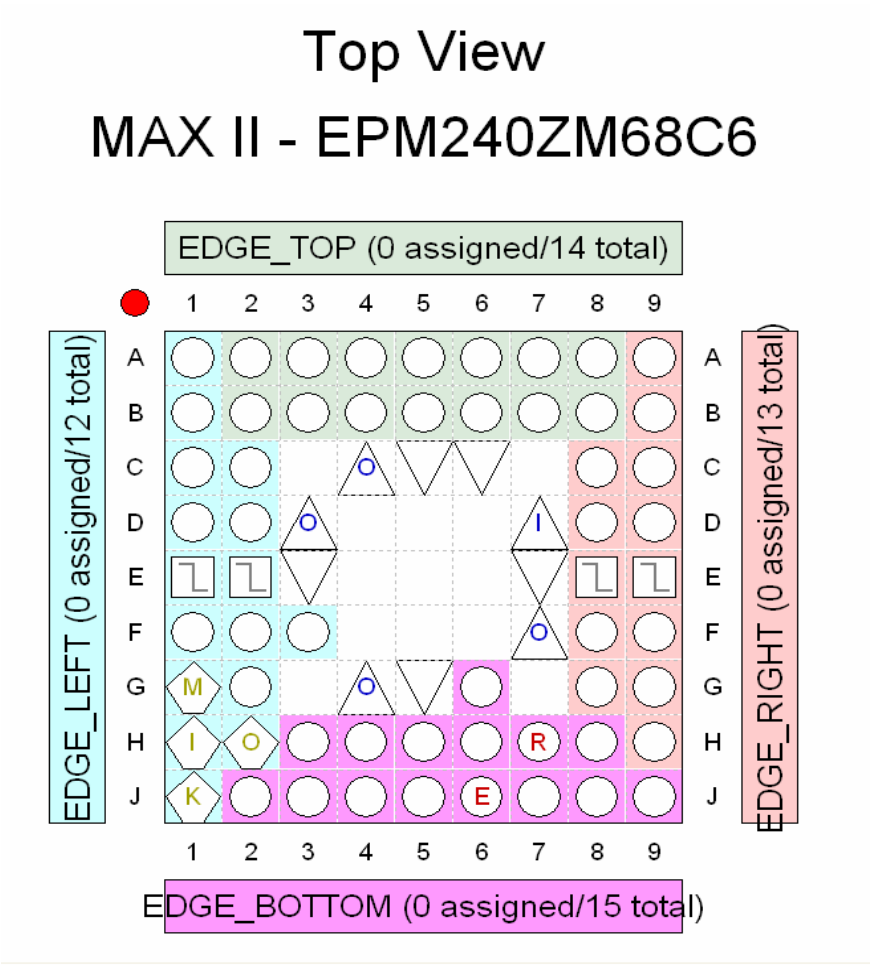
Figure 1. MAX II Z EPM240 M68 Device Top View Package Diagram and Bank Information



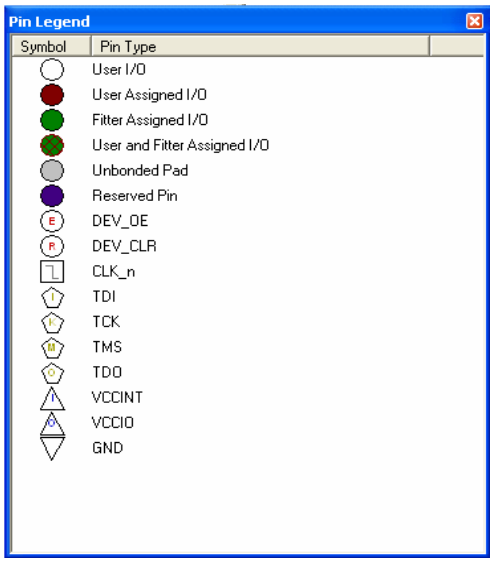


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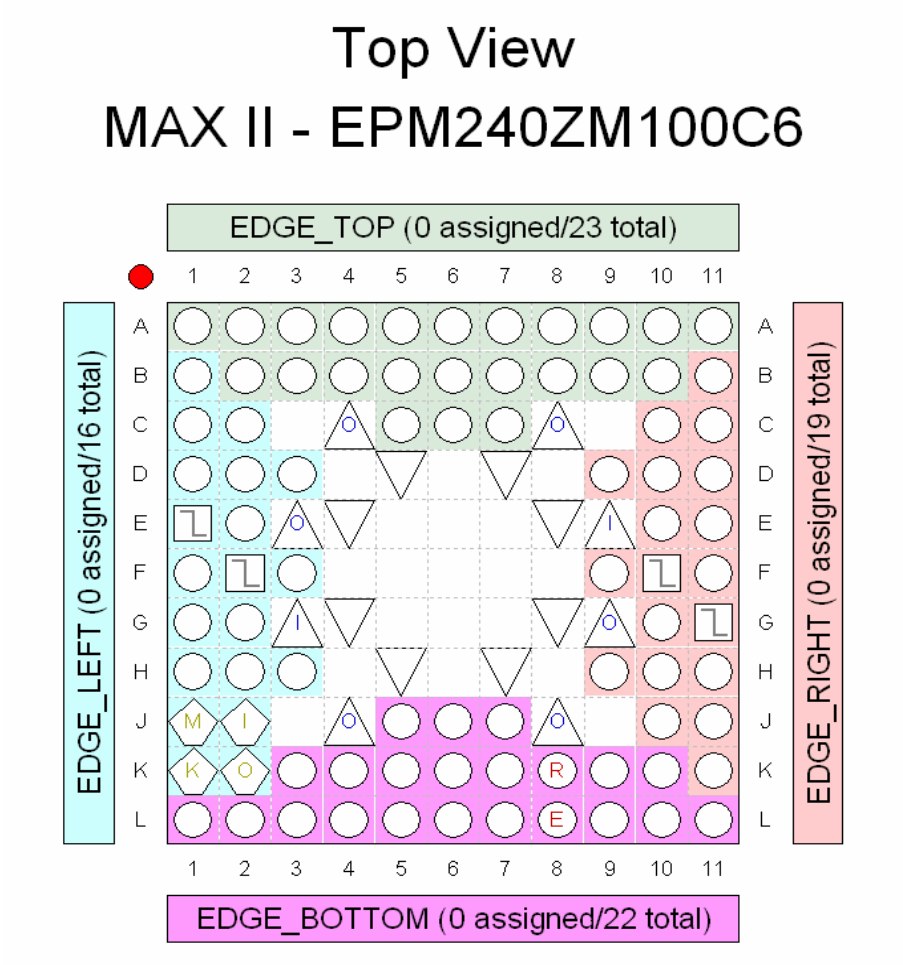
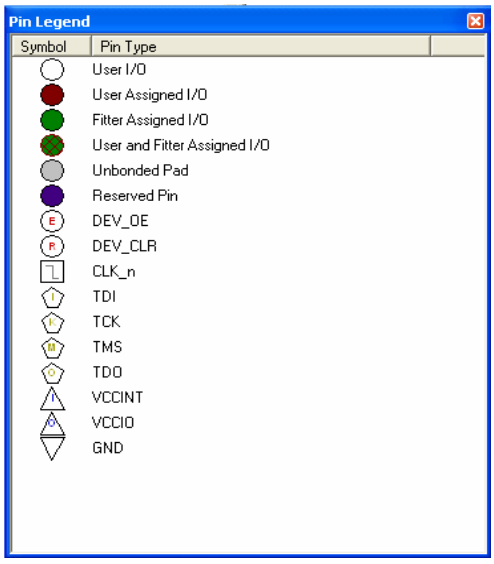
Figure 2. MAX II Z EPM240 M100 Device Top View Package Diagram and Bank Information





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Date	Version	Changes Made
Dec-07	1.0	Initial release

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