Bank Number	VREF Group (Note 5)	Pin Name/Function	Optional Function(s)/ DQ group for DQS x4 Mode	Configuration Function	F672	F484	x8/x9 Mode (Note 2)	x16/x18 Mode (Note 2)	x5 Mode (Note 3)				x4 Mode (Note 4)			
							DQ group for DQS mode	DQ group for DQS mode	DQ group for non-DQS mode (non-migratable) F672	DQ group for non-DQS mode (non-migratable) F484	DQ group for non-DQS mode (migratable) F672	DQ group for non-DQS mode (migratable) F484	DQ group for non-DQS mode (non-migratable) F672	DQ group for non-DQS mode (non-migratable) F484	DQ group for non-DQS mode (migratable) F672	DQ group for non-DQS mode (migratable) F484
B2	VREFB2N0	IO	DIFFIO_RX18p		G24	C22			DQ0L0	DQ0L0	DQ3L0	DQ3L0	DQ0L0	DQ0L0	DQ4L0	DQ4L0
B2	VREFB2N0	IO	DIFFIO_RX18n		G23	C21			DQ0L1	DQ0L1	DQ3L1	DQ3L1	DQ0L1	DQ0L1	DQ4L1	DQ4L1
B2	VREFB2N0	IO	DIFFIO_TX18p		K22	E20			DQ6L0	DQ6L0			DQ7L0	DQ7L0		
B2	VREFB2N0	IO	DIFFIO_TX18n		K21	E19			DQ6L1	DQ6L1			DQ7L1	DQ7L1		
B2	VREFB2N0	IO	DIFFIO_RX17p		H24	D22			DQS0L	DQS0L	DQS3L	DQS3L	DQS0L	DQS0L	DQS4L	DQS4L
B2	VREFB2N0	IO	DIFFIO_RX17n		H23	D21			DQ0L2	DQ0L2	DQ3L2	DQ3L2	DQ0L2	DQ0L2	DQ4L2	DQ4L2
B2	VREFB2N0	IO	DIFFIO_TX17p		K20	G18			DQS6L	DQS6L			DQS7L	DQS7L		
B2	VREFB2N0	IO	DIFFIO_TX17n		K19	G17			DQ6L2	DQ6L2			DQ7L2	DQ7L2		
B2	VREFB2N0	VREFB2N0	VREFB2N0		G22	F18										
B2	VREFB2N0	IO	DIFFIO_RX16p		J24	E22			DQ0L3	DQ0L3	DQ3L3	DQ3L3	DQ0L3	DQ0L3	DQ4L3	DQ4L3
B2	VREFB2N0	IO	DIFFIO_RX16n		J23	E21			DM0L	DM0L	DM3L	DM3L	DQ1L0	DQ1L0	DQ5L0	DQ5L0
B2	VREFB2N0	IO	DIFFIO_TX16p		L23	F20			DQ6L3	DQ6L3	DQ16L0		DQ7L3	DQ7L3		
B2	VREFB2N0	IO	DIFFIO_TX16n		L22	F19			DM6L	DM6L	DQ16L1		DQ8L0	DQ8L0		
B2	VREFB2N0	IO	DIFFIO_RX15p		K24	F22			DQ1L0	DQ1L0	DQ4L0	DQ4L0	DQ1L1	DQ1L1	DQ5L1	DQ5L1
B2	VREFB2N0	IO	DIFFIO_RX15n		K23	F21			DQ1L1	DQ1L1	DQ4L1	DQ4L1	DQS1L	DQS1L	DQS5L	DQS5L
B2	VREFB2N0	IO	DIFFIO_TX15p		L21	H18			DQ7L0	DQ7L0	DQS16L		DQ8L1	DQ8L1		
B2	VREFB2N0	IO	DIFFIO_TX15n		L20	H17			DQ7L1	DQ7L1	DQ16L2		DQS8L	DQS8L		
B2	VREFB2N0	IO	DIFFIO_RX14p		G26	H20			DQS1L	DQS1L	DQS4L	DQS4L	DQ1L2	DQ1L2	DQ5L2	DQ5L2
B2	VREFB2N0	IO	DIFFIO_RX14n		G25	H19			DQ1L2	DQ1L2	DQ4L2	DQ4L2	DQ1L3	DQ1L3	DQ5L3	DQ5L3
B2	VREFB2N0	IO	DIFFIO_TX14p		L19	G20			DQS7L	DQS7L	DQ16L3		DQ8L2	DQ8L2		
B2	VREFB2N0	IO	DIFFIO_TX14n		L18	G19			DQ7L2	DQ7L2	DM16L		DQ8L3	DQ8L3		
B2	VREFB2N1	IO	DIFFIO_RX13p		H26	G22			DQ1L3	DQ1L3	DQ4L3	DQ4L3	DQ2L0	DQ2L0	DQ6L0	DQ6L0
B2	VREFB2N1	IO	DIFFIO_RX13n		H25	G21			DM1L	DM1L	DM4L	DM4L	DQ2L1	DQ2L1	DQ6L1	DQ6L1
B2	VREFB2N1	IO	DIFFIO_TX13p		M24	J17			DQ7L3	DQ7L3	DQ17L0	DQ17L0	DQ9L0	DQ9L0	DQ20L0	DQ20L0
B2	VREFB2N1	IO	DIFFIO_TX13n		M23	J16			DM7L	DM7L	DQ17L1	DQ17L1	DQ9L1	DQ9L1	DQ20L1	DQ20L1
B2	VREFB2N1	IO	DIFFIO_RX12p		J26	H22			DQ2L0	DQ2L0	DQ5L0	DQ5L0	DQS2L	DQS2L	DQS6L	DQS6L
B2	VREFB2N1	IO	DIFFIO_RX12n		J25	H21			DQ2L1	DQ2L1	DQ5L1	DQ5L1	DQ2L2	DQ2L2	DQ6L2	DQ6L2
B2	VREFB2N1	IO	DIFFIO_TX12p		M22	J19			DQ8L0	DQ8L0	DQS17L	DQS17L	DQS9L	DQS9L	DQS20L	DQS20L
B2	VREFB2N1	IO	DIFFIO_TX12n		M21	J18			DQ8L1	DQ8L1	DQ17L2	DQ17L2	DQ9L2	DQ9L2	DQ20L2	DQ20L2
B2	VREFB2N1	IO	DIFFIO_RX11p		L25	J21			DQS2L	DQS2L	DQS5L	DQS5L	DQ2L3	DQ2L3	DQ6L3	DQ6L3
B2	VREFB2N1	IO	DIFFIO_RX11n		L24	J20			DQ2L2	DQ2L2	DQ5L2	DQ5L2	DQ3L0	DQ3L0	DQ7L0	DQ7L0
B2	VREFB2N1	IO	DIFFIO_TX11p		N22	K18			DQS8L	DQS8L	DQ17L3	DQ17L3	DQ9L3	DQ9L3	DQ20L3	DQ20L3
B2	VREFB2N1	IO	DIFFIO_TX11n		N21	K17			DQ8L2	DQ8L2	DM17L	DM17L	DQ10L0	DQ10L0	DQ21L0	DQ21L0
B2	VREFB2N1	VREFB2N1	VREFB2N1		N23	L19										
B2	VREFB2N1	IO	DIFFIO_RX10p		K26	K20			DQ2L3	DQ2L3	DQ5L3	DQ5L3	DQ3L1	DQ3L1	DQ7L1	DQ7L1
B2	VREFB2N1	IO	DIFFIO_RX10n		K25	K19			DM2L	DM2L	DM5L	DM5L	DQS3L	DQS3L	DQS7L	DQS7L
B2	VREFB2N1	IO	DIFFIO_TX10p		N20	K16			DQ8L3	DQ8L3	DQ18L0	DQ18L0	DQ10L1	DQ10L1	DQ21L1	DQ21L1
B2	VREFB2N1	IO	DIFFIO_TX10n		N19	K15			DM8L	DM8L	DQ18L1	DQ18L1	DQS10L	DQS10L	DQS21L	DQS21L
B2	VREFB2N1	IO	DIFFIO_RX9p		M26	K22					DQS18L	DQS18L	DQ3L2	DQ3L2	DQ7L2	DQ7L2
B2	VREFB2N1	IO	DIFFIO_RX9n		M25	K21					DQ18L2	DQ18L2	DQ3L3	DQ3L3	DQ7L3	DQ7L3
B2	VREFB2N1	IO	DIFFIO_TX9p		M20	L16					DQ18L3	DQ18L3	DQ10L2	DQ10L2	DQ21L2	DQ21L2

B2	VREFB2N1	IO	DIFFIO_TX9n		M19	L15					DM18L	DM18L	DQ10L3	DQ10L3	DQ21L3	DQ21L3
B2	VREFB2N1	IO	CLK0n/DIFFIO_RX_C0n		P24	L20										
B2	VREFB2N1	IO	CLK0p/DIFFIO_RX_C0p		P25	L21										
B2	VREFB2N1	CLK1n	INPUT		N24	M20										
B2	VREFB2N1	CLK1p	INPUT		N25	M21										
		VCCD_PLL1			P19	M16										
		VCCA_PLL1			P21	M17										
		GNDA_PLL1			N18	L17										
		GNDA_PLL1			P18	L18										
		GNDA_PLL2			R19	N17										
		GNDA_PLL2			R20	N18										
		VCCA_PLL2			R21	M19										
		VCCD_PLL2			P20	M18										
B1	VREFB1N0	IO	CLK2p/DIFFIO_RX_C1p		R26	N22										
B1	VREFB1N0	IO	CLK2n/DIFFIO_RX_C1n		R25	N21										
B1	VREFB1N0	CLK3p	INPUT		P23	N20										
B1	VREFB1N0	CLK3n	INPUT		P22	N19										
B1	VREFB1N0	IO	DIFFIO_RX8p		T25	P21			DQ3L0	DQ3L0	DQ6L0	DQ6L0	DQ4L0	DQ4L0	DQ8L0	DQ8L0
B1	VREFB1N0	IO	DIFFIO_RX8n		T24	P20			DQ3L1	DQ3L1	DQ6L1	DQ6L1	DQ4L1	DQ4L1	DQ8L1	DQ8L1
B1	VREFB1N0	IO	DIFFIO_TX8p		R24	N16			DQ9L0	DQ9L0	DQ19L0		DQ11L0	DQ11L0		
B1	VREFB1N0	IO	DIFFIO_TX8n		R23	N15			DQ9L1	DQ9L1	DQ19L1		DQ11L1	DQ11L1		
B1	VREFB1N0	VREFB1N0	VREFB1N0		T23	R20										
B1	VREFB1N0	IO	DIFFIO_RX7p		U26	R22			DQS3L	DQS3L	DQS6L	DQS6L	DQS4L	DQS4L	DQS8L	DQS8L
B1	VREFB1N0	IO	DIFFIO_RX7n		U25	R21			DQ3L2	DQ3L2	DQ6L2	DQ6L2	DQ4L2	DQ4L2	DQ8L2	DQ8L2
B1	VREFB1N0	IO	DIFFIO_TX7p		U24	P19			DQS9L	DQS9L	DQS19L		DQS11L	DQS11L		
B1	VREFB1N0	IO	DIFFIO_TX7n		U23	P18			DQ9L2	DQ9L2	DQ19L2		DQ11L2	DQ11L2		
B1	VREFB1N0	IO	DIFFIO_RX6p		V26	T22			DQ3L3	DQ3L3	DQ6L3	DQ6L3	DQ4L3	DQ4L3	DQ8L3	DQ8L3
B1	VREFB1N0	IO	DIFFIO_RX6n		V25	T21			DM3L	DM3L	DM6L	DM6L	DQ5L0	DQ5L0	DQ9L0	DQ9L0
B1	VREFB1N0	IO	DIFFIO_TX6p		V24	P17			DQ9L3	DQ9L3	DQ19L3		DQ11L3	DQ11L3		
B1	VREFB1N0	IO	DIFFIO_TX6n		V23	P16			DM9L	DM9L	DM19L		DQ12L0	DQ12L0		
B1	VREFB1N0	IO	DIFFIO_RX5p		W26	U22			DQ4L0	DQ4L0	DQ7L0	DQ7L0	DQ5L1	DQ5L1	DQ9L1	DQ9L1
B1	VREFB1N0	IO	DIFFIO_RX5n		W25	U21			DQ4L1	DQ4L1	DQ7L1	DQ7L1	DQS5L	DQS5L	DQS9L	DQS9L
B1	VREFB1N0	IO	DIFFIO_TX5p		W22	R19			DQ10L0	DQ10L0	DQ20L0		DQ12L1	DQ12L1		
B1	VREFB1N0	IO	DIFFIO_TX5n		W21	R18			DQ10L1	DQ10L1	DQ20L1		DQS12L	DQS12L		
B1	VREFB1N1	IO	DIFFIO_RX4p		Y26	T20			DQS4L	DQS4L	DQS7L	DQS7L	DQ5L2	DQ5L2	DQ9L2	DQ9L2
B1	VREFB1N1	IO	DIFFIO_RX4n		Y25	T19			DQ4L2	DQ4L2	DQ7L2	DQ7L2	DQ5L3	DQ5L3	DQ9L3	DQ9L3
B1	VREFB1N1	IO	DIFFIO_TX4p		V22	T18			DQS10L	DQS10L	DQS20L		DQ12L2	DQ12L2		
B1	VREFB1N1	IO	DIFFIO_TX4n		V21	T17			DQ10L2	DQ10L2	DQ20L2		DQ12L3	DQ12L3		
B1	VREFB1N1	IO	DIFFIO_RX3p		AA26	U20			DQ4L3	DQ4L3	DQ7L3	DQ7L3	DQ6L0	DQ6L0	DQ10L0	
B1	VREFB1N1	IO	DIFFIO_RX3n		AA25	U19			DM4L	DM4L	DM7L	DM7L	DQ6L1	DQ6L1	DQ10L1	
B1	VREFB1N1	IO	DIFFIO_TX3p		U22	U18			DQ10L3	DQ10L3	DQ20L3		DQ13L0	DQ13L0		
B1	VREFB1N1	IO	DIFFIO_TX3n		U21	U17			DM10L	DM10L	DM20L		DQ13L1	DQ13L1		
B1	VREFB1N1	VREFB1N1	VREFB1N1		Y22	V20										
B1	VREFB1N1	IO	DIFFIO_RX2p		AA24	V22			DQ5L0	DQ5L0	DQ8L0		DQS6L	DQS6L	DQS10L	
B1	VREFB1N1	IO	DIFFIO_RX2n		AA23	V21			DQ5L1	DQ5L1	DQ8L1		DQ6L2	DQ6L2	DQ10L2	
B1	VREFB1N1	IO	DIFFIO_TX2p		T20	V19			DQ11L0	DQ11L0	DQ21L0		DQS13L	DQS13L	DQ22L0	
B1	VREFB1N1	IO	DIFFIO_TX2n		T19	V18			DQ11L1	DQ11L1	DQ21L1		DQ13L2	DQ13L2	DQ22L1	
B1	VREFB1N1	IO	DIFFIO_RX1p		Y24	W22			DQS5L	DQS5L	DQS8L		DQ6L3	DQ6L3	DQ10L3	
B1	VREFB1N1	IO	DIFFIO_RX1n		Y23	W21			DQ5L2	DQ5L2	DQ8L2				DQ11L0	
B1	VREFB1N1	IO	DIFFIO_TX1p		T22	W20			DQS11L	DQS11L	DQS21L		DQ13L3	DQ13L3	DQS22L	
B1	VREFB1N1	IO	DIFFIO_TX1n		T21	W19			DQ11L2	DQ11L2	DQ21L2				DQ22L2	
B1	VREFB1N1	IO	DIFFIO_RX0p		W24	Y22			DQ5L3	DQ5L3	DQ8L3				DQ11L1	
B1	VREFB1N1	IO	DIFFIO_RX0n		W23	Y21			DM5L	DM5L	DM8L				DQS11L	

B1	VREFB1N1	IO	DIFFIO_TX0p		U20	R17			DQ11L3	DQ11L3	DQ21L3				DQ22L3	
B1	VREFB1N1	IO	DIFFIO_TX0n		U19	R16			DM11L	DM11L	DM21L				DQ23L0	
B8	VREFB8N0	TDI		TDI	AE25	AB21										
B8	VREFB8N0	TMS		TMS	AD24	AA20										
B8	VREFB8N0	TCK		TCK	AB22	AA19										
B8	VREFB8N0	TRST		TRST	AB21	AB19										
B8	VREFB8N0	nCONFIG		nCONFIG	AA20	W18										
B8	VREFB8N0	VCCSEL		VCCSEL	Y19	V17										
B8	VREFB8N0	IO			W18	R15			DQ0B0	DQ0B0			DQ0B0	DQ0B0		
B8	VREFB8N0	IO			AB19	Y20			DQ0B1	DQ0B1			DQ0B1	DQ0B1		
B8	VREFB8N0	IO		CS	AC21	T16										
B8	VREFB8N0	IO		CLKUSR	AA19	U16										
B8	VREFB8N0	IO		nWS	AB20	V16										
B8	VREFB8N0	IO		nRS	AC20	W17										
B8	VREFB8N0	VREFB8N0	VREFB8N0		AC22	Y19										
B8	VREFB8N0	IO			Y18				DQS0B				DQS0B			
B8	VREFB8N0	IO			AC19	T15			DQ0B2	DQS0B			DQ0B2	DQS0B		
B8	VREFB8N0	IO	DQ17B		AE24	V15	DQ3B		DQ0B3	DQ0B2	DQ17B3		DQ0B3	DQ0B2	DQ17B3	
B8	VREFB8N0	IO	DQSn17B		AD23	U15	DQ3B	DQ1B	DM0B	DQ0B3	DQSB17B		DQ1B0	DQ0B3	DQSB17B	
B8	VREFB8N0	IO	DQ17B		AF24		DQ3B	DQ1B	DQ1B0		DQ17B2		DQ1B1		DQ17B2	
B8	VREFB8N0	IO	DQ17B		AE22	W15	DQ3B	DQ1B	DQ1B1	DM0B	DQ17B1		DQS1B	DQ1B0	DQ17B1	
B8	VREFB8N0	IO	DQ17B		AD22	W16	DQ3B	DQ1B	DQS1B	DQ1B0	DQ17B0		DQ1B2	DQ1B1	DQ17B0	
B8	VREFB8N0	IO	DQS17B		AE23	U14	DQVLD3B		DQ1B2	DQ1B1	DQS17B		DQ1B3	DQS1B	DQS17B	
B8	VREFB8N0	IO			W17				DQ1B3				DQ2B0			
B8	VREFB8N0	IO			AB18	R14			DM1B	DQS1B			DQ2B1	DQ1B2		
B8	VREFB8N0	IO	DQ15B		AF22	V14	DQ3B	DQ1B	DQ2B0	DQ1B2	DQ15B3		DQS2B	DQ1B3	DQ15B3	
B8	VREFB8N0	IO	DQSn15B		AE21		DQSn3B	DQ1B	DQ2B1		DQSB15B		DQ2B2		DQSB15B	
B8	VREFB8N0	IO	DQ15B		AD21	T14	DQ3B	DQ1B	DQS2B	DQ1B3	DQ15B2		DQ2B3	DQ2B0	DQ15B2	
B8	VREFB8N0	IO	DQ15B		AD20	Y14	DQ3B	DQ1B	DQ2B2	DM1B	DQ15B1		DQ3B0	DQ2B1	DQ15B1	
B8	VREFB8N0	IO	DQ15B		AF21	W14	DQ3B	DQ1B	DQ2B3	DQ2B0	DQ15B0		DQ3B1	DQS2B	DQ15B0	
B8	VREFB8N0	IO	DQS15B		AE20		DQS3B	DQVLD1B	DM2B		DQS15B		DQS3B		DQS15B	
B8	VREFB8N1	IO			Y17	U13			DQ3B0	DQ2B1			DQ3B2	DQ2B2		
B8	VREFB8N1	IO			AC18	V13			DQ3B1	DQS2B			DQ3B3	DQ2B3		
B8	VREFB8N1	IO	DQ13B		AF20	Y18	DQ2B	DQ1B	DQS3B	DQ2B2	DQ13B3	DQ13B3	DQ4B0	DQ3B0	DQ13B3	DQ13B3
B8	VREFB8N1	IO	DQSn13B		AE19	AA18	DQ2B	DQSn1B	DQ3B2	DQ2B3	DQSB13B	DQSB13B	DQ4B1	DQ3B1	DQSB13B	DQSB13B
B8	VREFB8N1	IO	DQ13B		AD19	Y17	DQ2B	DQ1B	DQ3B3	DM2B	DQ13B2	DQ13B2	DQS4B	DQS3B	DQ13B2	DQ13B2
B8	VREFB8N1	IO	DQ13B		AD18	AB18	DQ2B	DQ1B	DM3B	DQ3B0	DQ13B1	DQ13B1	DQ4B2	DQ3B2	DQ13B1	DQ13B1
B8	VREFB8N1	IO	DQ13B		AF19	AB17	DQ2B	DQ1B	DQ4B0	DQ3B1	DQ13B0	DQ13B0	DQ4B3	DQ3B3	DQ13B0	DQ13B0
B8	VREFB8N1	IO	DQS13B		AE18	AA17	DQVLD2B	DQS1B	DQ4B1	DQS3B	DQS13B	DQS13B	DQ5B0	DQ4B0	DQS13B	DQS13B
B8	VREFB8N1	IO			AA17	T13			DQS4B	DQ3B2			DQ5B1	DQ4B1		
B8	VREFB8N1	IO			AB17				DQ4B2				DQS5B			
B8	VREFB8N1	IO	DQ11B		AF18	Y16	DQ2B	DQ1B	DQ4B3	DQ3B3	DQ11B3	DQ11B3	DQ5B2	DQS4B	DQ11B3	DQ11B3
B8	VREFB8N1	IO	DQSn11B		AE17	AA16	DQSn2B	DQ1B	DM4B	DM3B	DQSB11B	DQSB11B	DQ5B3	DQ4B2	DQSB11B	DQSB11B
B8	VREFB8N1	VREFB8N1	VREFB8N1		AC16	AA14										
B8	VREFB8N1	IO	DQ11B		AD17	AB16	DQ2B	DQ1B	DQ5B0	DQ4B0	DQ11B2	DQ11B2	DQ6B0	DQ4B3	DQ11B2	DQ11B2
B8	VREFB8N1	IO	DQ11B		AF17	Y15	DQ2B	DQ1B	DQ5B1	DQ4B1	DQ11B1	DQ11B1	DQ6B1	DQ5B0	DQ11B1	DQ11B1
B8	VREFB8N1	IO	DQ11B		AD16	AB15	DQ2B	DQ1B	DQS5B	DQS4B	DQ11B0	DQ11B0	DQS6B	DQ5B1	DQ11B0	DQ11B0
B8	VREFB8N1	IO	DQS11B		AE16	AA15	DQS2B		DQ5B2	DQ4B2	DQS11B	DQS11B	DQ6B2	DQS5B	DQS11B	DQS11B
B8	VREFB8N1	IO			Y16	W13			DQ5B3	DQ4B3			DQ6B3	DQ5B2		
B8	VREFB8N1	IO			AA16	U12			DM5B	DM4B				DQ5B3		
B8	VREFB8N1	IO			AC17											
B8	VREFB8N1	IO			AB16	Y13										
B8	VREFB8N1	IO		RUnLU	Y15	V11										

B8	VREFB8N1	IO		DEV_OE	AA14	V12										
B8	VREFB8N1	IO		DEV_CLRn	AA15	W11										
B8	VREFB8N1	IO		nCS	AB15	W12										
B8	VREFB8N1	IO	CLK5n		AB14	Y12										
B8	VREFB8N1	IO	CLK5p		AC14	AA12										
B8	VREFB8N1	IO	CLK4n		AE15	AA13										
B8	VREFB8N1	IO	CLK4p		AF15	AB13										
		GNDA_PLL6			W13	T11										
		GNDA_PLL6			W14	T12										
		VCCA_PLL6			Y13	R12										
		VCCD_PLL6			Y14	U11										
B10		VCC_PLL6_OUT			V13	R11										
B7	VREFB7N0	IO	CLK7p		AC13	Y10										
B7	VREFB7N0	IO	CLK7n		AB13	W10										
B7	VREFB7N0	IO	CLK6p		AE14	AA11										
B7	VREFB7N0	IO	CLK6n		AD14	Y11										
B10	VREFB7N0	IO	PLL6_OUT1p		AE13	AA9										
B10	VREFB7N0	IO	PLL6_OUT1n		AD13	Y9										
B10	VREFB7N0	IO	PLL6_OUT0p		AF12	AB10										
B10	VREFB7N0	IO	PLL6_OUT0n		AE12	AA10										
B10	VREFB7N0	IO	PLL6_FBp/OUT2p		AD12	W9										
B10	VREFB7N0	IO	PLL6_FBn/OUT2n		AC12	V9										
B7	VREFB7N0	IO	DQ9B		AE11	AB8	DQ1B		DQ6B0	DQ5B0	DQ9B3	DQ9B3	DQ7B0	DQ6B0	DQ9B3	DQ9B3
B7	VREFB7N0	IO	DQSn9B		AE10	AA8	DQ1B	DQ0B	DQ6B1	DQ5B1	DQSB9B	DQSB9B	DQ7B1	DQ6B1	DQSB9B	DQSB9B
B7	VREFB7N0	VREFB7N0	VREFB7N0		AC11	W8										
B7	VREFB7N0	IO	DQ9B		AC10	Y8	DQ1B	DQ0B	DQS6B	DQS5B	DQ9B2	DQ9B2	DQS7B	DQS6B	DQ9B2	DQ9B2
B7	VREFB7N0	IO	DQ9B		AF10	Y7	DQ1B	DQ0B	DQ6B2	DQ5B2	DQ9B1	DQ9B1	DQ7B2	DQ6B2	DQ9B1	DQ9B1
B7	VREFB7N0	IO	DQ9B		AD11	AB7	DQ1B	DQ0B	DQ6B3	DQ5B3	DQ9B0	DQ9B0	DQ7B3	DQ6B3	DQ9B0	DQ9B0
B7	VREFB7N0	IO	DQS9B		AD10	AA7	DQVLD1B		DM6B	DM5B	DQS9B	DQS9B	DQ8B0	DQ7B0	DQS9B	DQS9B
B7	VREFB7N0	IO			AA12	T10			DQ7B0	DQ6B0			DQ8B1	DQ7B1		
B7	VREFB7N0	IO			AB12	U10			DQ7B1	DQ6B1			DQS8B	DQS7B		
B7	VREFB7N0	IO	DQ7B		AF9	AB6	DQ1B	DQ0B	DQS7B	DQS6B	DQ7B3	DQ7B3	DQ8B2	DQ7B2	DQ7B3	DQ7B3
B7	VREFB7N0	IO	DQSn7B		AE9	AA6	DQSn1B	DQ0B	DQ7B2	DQ6B2	DQSB7B	DQSB7B	DQ8B3	DQ7B3	DQSB7B	DQSB7B
B7	VREFB7N0	IO	DQ7B		AD8	Y6	DQ1B	DQ0B	DQ7B3	DQ6B3	DQ7B2	DQ7B2	DQ9B0	DQ8B0	DQ7B2	DQ7B2
B7	VREFB7N0	IO	DQ7B		AC8	Y5	DQ1B	DQ0B	DM7B	DM6B	DQ7B1	DQ7B1	DQ9B1	DQ8B1	DQ7B1	DQ7B1
B7	VREFB7N0	IO	DQ7B		AC9	AB5	DQ1B	DQ0B	DQ8B0	DQ7B0	DQ7B0	DQ7B0	DQS9B	DQS8B	DQ7B0	DQ7B0
B7	VREFB7N0	IO	DQS7B		AD9	AA5	DQS1B	DQVLD0B	DQ8B1	DQ7B1	DQS7B	DQS7B	DQ9B2	DQ8B2	DQS7B	DQS7B
B7	VREFB7N1	IO			AA11				DQS8B				DQ9B3			
B7	VREFB7N1	IO			AB11	V8			DQ8B2	DQS7B			DQ10B0	DQ8B3		
B7	VREFB7N1	IO	DQ5B		AF8	V10	DQ0B	DQ0B	DQ8B3	DQ7B2	DQ5B3		DQ10B1	DQ9B0	DQ5B3	
B7	VREFB7N1	IO	DQSn5B		AE8		DQ0B	DQSn0B	DM8B		DQSB5B		DQS10B		DQSB5B	
B7	VREFB7N1	IO	DQ5B		AC7	R9	DQ0B	DQ0B	DQ9B0	DQ7B3	DQ5B2		DQ10B2	DQ9B1	DQ5B2	
B7	VREFB7N1	IO	DQ5B		AD7	T9	DQ0B	DQ0B	DQ9B1	DM7B	DQ5B1		DQ10B3	DQS9B	DQ5B1	
B7	VREFB7N1	IO	DQ5B		AF7		DQ0B	DQ0B	DQS9B		DQ5B0		DQ11B0		DQ5B0	
B7	VREFB7N1	IO	DQS5B		AE7	U9	DQVLD0B	DQS0B	DQ9B2	DQ8B0	DQS5B		DQ11B1	DQ9B2	DQS5B	
B7	VREFB7N1	IO			AA10	T8			DQ9B3	DQ8B1			DQS11B	DQ9B3		
B7	VREFB7N1	IO			Y10				DM9B				DQ11B2			
B7	VREFB7N1	IO	DQ3B		AF6	U8	DQ0B	DQ0B	DQ10B0	DQS8B	DQ3B3		DQ11B3	DQ10B0	DQ3B3	
B7	VREFB7N1	IO	DQSn3B		AE6	V7	DQSn0B	DQ0B	DQ10B1	DQ8B2	DQSB3B		DQ12B0	DQ10B1	DQSB3B	
B7	VREFB7N1	VREFB7N1	VREFB7N1		AC5	W6										
B7	VREFB7N1	IO	DQ3B		AC6		DQ0B	DQ0B	DQS10B		DQ3B2		DQ12B1		DQ3B2	
B7	VREFB7N1	IO	DQ3B		AE5		DQ0B	DQ0B	DQ10B2		DQ3B1		DQS12B		DQ3B1	
B7	VREFB7N1	IO	DQ3B		AF5	W7	DQ0B	DQ0B	DQ10B3	DQ8B3	DQ3B0		DQ12B2	DQS10B	DQ3B0	

B7	VREFB7N1	IO	DQS3B		AD6	U6	DQS0B		DM10B	DM8B	DQS3B		DQ12B3	DQ10B2	DQS3B	
B7	VREFB7N1	IO	RDN7		AB9	U7										
B7	VREFB7N1	IO	RUP7		AB10	W5										
B7	VREFB7N1	IO	DQ1B		AD5	AA4			DQ11B0		DQ1B3		DQ13B0	DQ10B3	DQ1B3	
B7	VREFB7N1	IO	DQSn1B		AE4				DQ11B1		DQSB1B		DQ13B1		DQSB1B	
B7	VREFB7N1	IO	DQ1B		AD3	Y3			DQS11B		DQ1B2		DQS13B		DQ1B2	
B7	VREFB7N1	IO	DQ1B		AD4	T7			DQ11B2		DQ1B1		DQ13B2		DQ1B1	
B7	VREFB7N1	IO	DQ1B		AF3	V6			DQ11B3		DQ1B0		DQ13B3		DQ1B0	
B7	VREFB7N1	IO	DQS1B		AE3				DM11B		DQS1B				DQS1B	
B7	VREFB7N1	PORSEL		PORSEL	Y8	V5										
B7	VREFB7N1	nIO_PULLUP		nIO_PULLUP	AE2	AB2										
B7	VREFB7N1	PLL_ENA		PLL_ENA	AB6	Y4										
		GND			AA7	AB4										
B7	VREFB7N1	nCEO		nCEO	AB5	AA3										
B6	VREFB6N0	IO	DIFFIO_TX37n		V8	W4			DM11R	DM11R	DM21R					
B6	VREFB6N0	IO	DIFFIO_TX37p		V7	W3			DQ11R3	DQ11R3	DQ21R3					
B6	VREFB6N0	IO	DIFFIO_RX37n		Y4	Y2			DM5R	DM5R	DM8R					
B6	VREFB6N0	IO	DIFFIO_RX37p		Y3	Y1			DQ5R3	DQ5R3	DQ8R3					
B6	VREFB6N0	IO	DIFFIO_TX36n		V6	V4			DQ11R2	DQ11R2	DQ21R2					
B6	VREFB6N0	IO	DIFFIO_TX36p		V5	V3			DQS11R	DQS11R	DQS21R		DQ13R3	DQ13R3		
B6	VREFB6N0	IO	DIFFIO_RX36n		W4	W2			DQ5R2	DQ5R2	DQ8R2					
B6	VREFB6N0	IO	DIFFIO_RX36p		W3	W1			DQS5R	DQS5R	DQS8R		DQ6R3	DQ6R3		
B6	VREFB6N0	IO	DIFFIO_TX35n		U8	R8			DQ11R1	DQ11R1	DQ21R1		DQ13R2	DQ13R2		
B6	VREFB6N0	IO	DIFFIO_TX35p		U7	R7			DQ11R0	DQ11R0	DQ21R0		DQS13R	DQS13R		
B6	VREFB6N0	IO	DIFFIO_RX35n		AB2	V2			DQ5R1	DQ5R1	DQ8R1		DQ6R2	DQ6R2		
B6	VREFB6N0	IO	DIFFIO_RX35p		AB1	V1			DQ5R0	DQ5R0	DQ8R0		DQS6R	DQS6R		
B6	VREFB6N0	VREFB6N0	VREFB6N0		Y5	U3										
B6	VREFB6N0	IO	DIFFIO_TX34n		T7	U5			DM10R	DM10R	DM20R		DQ13R1	DQ13R1		
B6	VREFB6N0	IO	DIFFIO_TX34p		T6	U4			DQ10R3	DQ10R3	DQ20R3		DQ13R0	DQ13R0		
B6	VREFB6N0	IO	DIFFIO_RX34n		AA2	T4			DM4R	DM4R	DM7R	DM7R	DQ6R1	DQ6R1		
B6	VREFB6N0	IO	DIFFIO_RX34p		AA1	T3			DQ4R3	DQ4R3	DQ7R3	DQ7R3	DQ6R0	DQ6R0		
B6	VREFB6N0	IO	DIFFIO_TX33n		U6	T6			DQ10R2	DQ10R2	DQ20R2		DQ12R3	DQ12R3		
B6	VREFB6N0	IO	DIFFIO_TX33p		U5	T5			DQS10R	DQS10R	DQS20R		DQ12R2	DQ12R2		
B6	VREFB6N0	IO	DIFFIO_RX33n		Y2	U2			DQ4R2	DQ4R2	DQ7R2	DQ7R2	DQ5R3	DQ5R3	DQ9R3	DQ9R3
B6	VREFB6N0	IO	DIFFIO_RX33p		Y1	U1			DQS4R	DQS4R	DQS7R	DQS7R	DQ5R2	DQ5R2	DQ9R2	DQ9R2
B6	VREFB6N1	IO	DIFFIO_TX32n		V4	R6			DQ10R1	DQ10R1	DQ20R1		DQS12R	DQS12R		
B6	VREFB6N1	IO	DIFFIO_TX32p		V3	R5			DQ10R0	DQ10R0	DQ20R0		DQ12R1	DQ12R1		
B6	VREFB6N1	IO	DIFFIO_RX32n		W2	R4			DQ4R1	DQ4R1	DQ7R1	DQ7R1	DQS5R	DQS5R	DQS9R	DQS9R
B6	VREFB6N1	IO	DIFFIO_RX32p		W1	R3			DQ4R0	DQ4R0	DQ7R0	DQ7R0	DQ5R1	DQ5R1	DQ9R1	DQ9R1
B6	VREFB6N1	IO	DIFFIO_TX31n		T9	P8			DM9R	DM9R	DM19R		DQ12R0	DQ12R0		
B6	VREFB6N1	IO	DIFFIO_TX31p		T8	P7			DQ9R3	DQ9R3	DQ19R3		DQ11R3	DQ11R3		
B6	VREFB6N1	IO	DIFFIO_RX31n		V2	T2			DM3R	DM3R	DM6R	DM6R	DQ5R0	DQ5R0	DQ9R0	DQ9R0
B6	VREFB6N1	IO	DIFFIO_RX31p		V1	T1			DQ3R3	DQ3R3	DQ6R3	DQ6R3	DQ4R3	DQ4R3	DQ8R3	DQ8R3
B6	VREFB6N1	IO	DIFFIO_TX30n		U4	P6			DQ9R2	DQ9R2	DQ19R2		DQ11R2	DQ11R2		
B6	VREFB6N1	IO	DIFFIO_TX30p		U3	P5			DQS9R	DQS9R	DQS19R		DQS11R	DQS11R		
B6	VREFB6N1	IO	DIFFIO_RX30n		U2	R2			DQ3R2	DQ3R2	DQ6R2	DQ6R2	DQ4R2	DQ4R2	DQ8R2	DQ8R2
B6	VREFB6N1	IO	DIFFIO_RX30p		U1	R1			DQS3R	DQS3R	DQS6R	DQS6R	DQS4R	DQS4R	DQS8R	DQS8R
B6	VREFB6N1	VREFB6N1	VREFB6N1		R5	P4										
B6	VREFB6N1	IO	DIFFIO_TX29n		T5	N8			DQ9R1	DQ9R1	DQ19R1		DQ11R1	DQ11R1		
B6	VREFB6N1	IO	DIFFIO_TX29p		T4	N7			DQ9R0	DQ9R0	DQ19R0		DQ11R0	DQ11R0		
B6	VREFB6N1	IO	DIFFIO_RX29n		T3	P3			DQ3R1	DQ3R1	DQ6R1	DQ6R1	DQ4R1	DQ4R1	DQ8R1	DQ8R1
B6	VREFB6N1	IO	DIFFIO_RX29p		T2	P2			DQ3R0	DQ3R0	DQ6R0	DQ6R0	DQ4R0	DQ4R0	DQ8R0	DQ8R0
B6	VREFB6N1	CLK9n	INPUT		R4	N4										

B6	VREFB6N1	CLK9p	INPUT		R3	N3											
B6	VREFB6N1	IO	CLK8n/DIFFIO_RX_C2n		R2	N2											
B6	VREFB6N1	IO	CLK8p/DIFFIO_RX_C2p		R1	N1											
		VCCD_PLL3			P7	M5											
		VCCA_PLL3			R6	M4											
		GNDA_PLL3			R7	N5											
		GNDA_PLL3			R8	N6											
		GNDA_PLL4			N8	L4											
		GNDA_PLL4			N9	L5											
		VCCA_PLL4			P8	M6											
		VCCD_PLL4			P9	L6											
B5	VREFB5N0	CLK11p	INPUT		N2	M2											
B5	VREFB5N0	CLK11n	INPUT		N3	M3											
B5	VREFB5N0	IO	CLK10p/DIFFIO_RX_C3p		P2	L2											
B5	VREFB5N0	IO	CLK10n/DIFFIO_RX_C3n		P3	L3											
B5	VREFB5N0	IO	DIFFIO_TX28n		N7	L8					DM18R	DM18R	DQ10R3	DQ10R3	DQ19R3	DQ19R3	
B5	VREFB5N0	IO	DIFFIO_TX28p		N6	L7					DQ18R3	DQ18R3	DQ10R2	DQ10R2	DQ19R2	DQ19R2	
B5	VREFB5N0	IO	DIFFIO_RX28n		M2	K2					DQ18R2	DQ18R2	DQ3R3	DQ3R3	DQ7R3	DQ7R3	
B5	VREFB5N0	IO	DIFFIO_RX28p		M1	K1					DQS18R	DQS18R	DQ3R2	DQ3R2	DQ7R2	DQ7R2	
B5	VREFB5N0	IO	DIFFIO_TX27n		P5	K8			DM8R	DM8R	DQ18R1	DQ18R1	DQS10R	DQS10R	DQS19R	DQS19R	
B5	VREFB5N0	IO	DIFFIO_TX27p		P4	K7			DQ8R3	DQ8R3	DQ18R0	DQ18R0	DQ10R1	DQ10R1	DQ19R1	DQ19R1	
B5	VREFB5N0	IO	DIFFIO_RX27n		L3	K4			DM2R	DM2R	DM5R	DM5R	DQS3R	DQS3R	DQS7R	DQS7R	
B5	VREFB5N0	IO	DIFFIO_RX27p		L2	K3			DQ2R3	DQ2R3	DQ5R3	DQ5R3	DQ3R1	DQ3R1	DQ7R1	DQ7R1	
B5	VREFB5N0	VREFB5N0	VREFB5N0		K5	J4											
B5	VREFB5N0	IO	DIFFIO_TX26n		N5	K6			DQ8R2	DQ8R2	DM17R		DQ10R0	DQ10R0	DQ19R0	DQ19R0	
B5	VREFB5N0	IO	DIFFIO_TX26p		N4	K5			DQS8R	DQS8R	DQ17R3		DQ9R3	DQ9R3			
B5	VREFB5N0	IO	DIFFIO_RX26n		K2	J3			DQ2R2	DQ2R2	DQ5R2	DQ5R2	DQ3R0	DQ3R0	DQ7R0	DQ7R0	
B5	VREFB5N0	IO	DIFFIO_RX26p		K1	J2			DQS2R	DQS2R	DQS5R	DQS5R	DQ2R3	DQ2R3	DQ6R3	DQ6R3	
B5	VREFB5N0	IO	DIFFIO_TX25n		M6	J6			DQ8R1	DQ8R1	DQ17R2		DQ9R2	DQ9R2			
B5	VREFB5N0	IO	DIFFIO_TX25p		M5	J5			DQ8R0	DQ8R0	DQS17R		DQS9R	DQS9R			
B5	VREFB5N0	IO	DIFFIO_RX25n		J2	H2			DQ2R1	DQ2R1	DQ5R1	DQ5R1	DQ2R2	DQ2R2	DQ6R2	DQ6R2	
B5	VREFB5N0	IO	DIFFIO_RX25p		J1	H1			DQ2R0	DQ2R0	DQ5R0	DQ5R0	DQS2R	DQS2R	DQS6R	DQS6R	
B5	VREFB5N0	IO	DIFFIO_TX24n		M8	H6			DM7R	DM7R	DQ17R1		DQ9R1	DQ9R1			
B5	VREFB5N0	IO	DIFFIO_TX24p		M7	H5			DQ7R3	DQ7R3	DQ17R0		DQ9R0	DQ9R0			
B5	VREFB5N0	IO	DIFFIO_RX24n		K4	G2			DM1R	DM1R	DM4R	DM4R	DQ2R1	DQ2R1	DQ6R1	DQ6R1	
B5	VREFB5N0	IO	DIFFIO_RX24p		K3	G1			DQ1R3	DQ1R3	DQ4R3	DQ4R3	DQ2R0	DQ2R0	DQ6R0	DQ6R0	
B5	VREFB5N1	IO	DIFFIO_TX23n		L9	J8			DQ7R2	DQ7R2			DQ8R3	DQ8R3			
B5	VREFB5N1	IO	DIFFIO_TX23p		L8	J7			DQS7R	DQS7R			DQ8R2	DQ8R2			
B5	VREFB5N1	IO	DIFFIO_RX23n		H2	H4			DQ1R2	DQ1R2	DQ4R2	DQ4R2	DQ1R3	DQ1R3	DQ5R3	DQ5R3	
B5	VREFB5N1	IO	DIFFIO_RX23p		H1	H3			DQS1R	DQS1R	DQS4R	DQS4R	DQ1R2	DQ1R2	DQ5R2	DQ5R2	
B5	VREFB5N1	IO	DIFFIO_TX22n		L7	G4			DQ7R1	DQ7R1			DQS8R	DQS8R			
B5	VREFB5N1	IO	DIFFIO_TX22p		L6	G3			DQ7R0	DQ7R0			DQ8R1	DQ8R1			
B5	VREFB5N1	IO	DIFFIO_RX22n		G2	F2			DQ1R1	DQ1R1	DQ4R1	DQ4R1	DQS1R	DQS1R	DQS5R	DQS5R	
B5	VREFB5N1	IO	DIFFIO_RX22p		G1	F1			DQ1R0	DQ1R0	DQ4R0	DQ4R0	DQ1R1	DQ1R1	DQ5R1	DQ5R1	
B5	VREFB5N1	IO	DIFFIO_TX21n		M4	G6			DM6R	DM6R	DM16R		DQ8R0	DQ8R0			
B5	VREFB5N1	IO	DIFFIO_TX21p		M3	G5			DQ6R3	DQ6R3	DQ16R3		DQ7R3	DQ7R3			
B5	VREFB5N1	IO	DIFFIO_RX21n		J4	E2			DM0R	DM0R	DM3R	DM3R	DQ1R0	DQ1R0	DQ5R0	DQ5R0	
B5	VREFB5N1	IO	DIFFIO_RX21p		J3	E1			DQ0R3	DQ0R3	DQ3R3	DQ3R3	DQ0R3	DQ0R3	DQ4R3	DQ4R3	
B5	VREFB5N1	VREFB5N1	VREFB5N1		G5	F3											
B5	VREFB5N1	IO	DIFFIO_TX20n		L5	F5			DQ6R2	DQ6R2	DQ16R2		DQ7R2	DQ7R2			
B5	VREFB5N1	IO	DIFFIO_TX20p		L4	F4			DQS6R	DQS6R	DQS16R		DQS7R	DQS7R	DQ18R3		
B5	VREFB5N1	IO	DIFFIO_RX20n		H4	D2			DQ0R2	DQ0R2	DQ3R2	DQ3R2	DQ0R2	DQ0R2	DQ4R2	DQ4R2	
B5	VREFB5N1	IO	DIFFIO_RX20p		H3	D1			DQS0R	DQS0R	DQS3R	DQS3R	DQS0R	DQS0R	DQS4R	DQS4R	

B5	VREFB5N1	IO	DIFFIO_TX19n		K9	E4			DQ6R1	DQ6R1	DQ16R1		DQ7R1	DQ7R1	DQ18R2	
B5	VREFB5N1	IO	DIFFIO_TX19p		K8	E3			DQ6R0	DQ6R0	DQ16R0		DQ7R0	DQ7R0	DQS18R	
B5	VREFB5N1	IO	DIFFIO_RX19n		G4	C2			DQ0R1	DQ0R1	DQ3R1	DQ3R1	DQ0R1	DQ0R1	DQ4R1	DQ4R1
B5	VREFB5N1	IO	DIFFIO_RX19p		G3	C1			DQ0R0	DQ0R0	DQ3R0	DQ3R0	DQ0R0	DQ0R0	DQ4R0	DQ4R0
		TEMPDIODEp			E5	A2										
		TEMPDIODEn			F5	C3										
B4	VREFB4N0	TDO		TDO	F6	B3										
B4	VREFB4N0	MSEL3		MSEL3	F7	A4										
B4	VREFB4N0	MSEL2		MSEL2	E6	B4										
B4	VREFB4N0	MSEL1		MSEL1	B2	D4										
B4	VREFB4N0	MSEL0		MSEL0	G8	E5										
B4	VREFB4N0	IO	DQS1T		B3	E6			DM10T		DQS1T				DQS1T	
B4	VREFB4N0	IO	DQ1T		A3	D5			DQ10T3		DQ1T0		DQ12T3		DQ1T0	
B4	VREFB4N0	IO	DQ1T		C4				DQ10T2		DQ1T1		DQ12T2		DQ1T1	
B4	VREFB4N0	IO	DQ1T		C3	H7			DQS10T		DQ1T2		DQS12T		DQ1T2	
B4	VREFB4N0	IO	DQSn1T		B4	C4			DQ10T1		DQSB1T		DQ12T1		DQSB1T	
B4	VREFB4N0	IO	DQ1T		C5	D3			DQ10T0		DQ1T3		DQ12T0	DQ10T3	DQ1T3	
B4	VREFB4N0	IO	RUP4		E7	G7										
B4	VREFB4N0	IO	RDN4		E8	F6										
B4	VREFB4N0	IO	DQS3T		C6	E7	DQS0T		DM9T	DM8T	DQS3T		DQ11T3	DQ10T2	DQS3T	
B4	VREFB4N0	IO	DQ3T		A5	G8	DQ0T	DQ0T	DQ9T3	DQ8T3	DQ3T0		DQ11T2	DQS10T	DQ3T0	
B4	VREFB4N0	IO	DQ3T		B5		DQ0T	DQ0T	DQ9T2		DQ3T1		DQS11T		DQ3T1	
B4	VREFB4N0	IO	DQ3T		D6		DQ0T	DQ0T	DQS9T		DQ3T2		DQ11T1		DQ3T2	
B4	VREFB4N0	VREFB4N0	VREFB4N0		D5	D7										
B4	VREFB4N0	IO	DQSn3T		B6	D6	DQSn0T	DQ0T	DQ9T1	DQ8T2	DQSB3T		DQ11T0	DQ10T1	DQSB3T	
B4	VREFB4N0	IO	DQ3T		A6		DQ0T	DQ0T	DQ9T0		DQ3T3		DQ10T3		DQ3T3	
B4	VREFB4N0	IO			F10	F8			DM8T	DQS8T			DQ10T2	DQ10T0		
B4	VREFB4N0	IO			E9	F7			DQ8T3	DQ8T1			DQS10T	DQ9T3		
B4	VREFB4N0	IO	DQS5T		B7	D8	DQVLD0T	DQS0T	DQ8T2	DQ8T0	DQS5T		DQ10T1	DQ9T2	DQS5T	
B4	VREFB4N0	IO	DQ5T		A7		DQ0T	DQ0T	DQS8T		DQ5T0		DQ10T0		DQ5T0	
B4	VREFB4N0	IO	DQ5T		C7	E8	DQ0T	DQ0T	DQ8T1	DM7T	DQ5T1		DQ9T3	DQS9T	DQ5T1	
B4	VREFB4N0	IO	DQ5T		D7	F9	DQ0T	DQ0T	DQ8T0	DQ7T3	DQ5T2		DQ9T2	DQ9T1	DQ5T2	
B4	VREFB4N0	IO	DQSn5T		B8	E9	DQ0T	DQSn0T	DM7T	DQ7T2	DQSB5T		DQS9T	DQ9T0	DQSB5T	
B4	VREFB4N0	IO	DQ5T		A8		DQ0T	DQ0T	DQ7T3		DQ5T3		DQ9T1		DQ5T3	
B4	VREFB4N0	IO			F11	G9			DQ7T2	DQS7T			DQ9T0	DQ8T3		
B4	VREFB4N0	IO			E10	H9			DQS7T	DQ7T1			DQ8T3	DQ8T2		
B4	VREFB4N1	IO	DQS7T		C9	B5	DQS1T	DQVLD0T	DQ7T1	DQ7T0	DQS7T	DQS7T	DQ8T2	DQS8T	DQS7T	DQS7T
B4	VREFB4N1	IO	DQ7T		D9	A5	DQ1T	DQ0T	DQ7T0	DM6T	DQ7T0	DQ7T0	DQS8T	DQ8T1	DQ7T0	DQ7T0
B4	VREFB4N1	IO	DQ7T		D8	C5	DQ1T	DQ0T	DM6T	DQ6T3	DQ7T1	DQ7T1	DQ8T1	DQ8T0	DQ7T1	DQ7T1
B4	VREFB4N1	IO	DQ7T		C8	C6	DQ1T	DQ0T	DQ6T3	DQ6T2	DQ7T2	DQ7T2	DQ8T0	DQ7T3	DQ7T2	DQ7T2
B4	VREFB4N1	IO	DQSn7T		B9	B6	DQSn1T	DQ0T	DQ6T2	DQS6T	DQSB7T	DQSB7T	DQ7T3	DQ7T2	DQSB7T	DQSB7T
B4	VREFB4N1	IO	DQ7T		A9	A6	DQ1T	DQ0T	DQS6T	DQ6T1	DQ7T3	DQ7T3	DQ7T2	DQS7T	DQ7T3	DQ7T3
B4	VREFB4N1	IO			E11				DQ6T1				DQS7T			
B4	VREFB4N1	IO			E12	E10			DQ6T0	DQ6T0			DQ7T1	DQ7T1		
B4	VREFB4N1	VREFB4N1	VREFB4N1		D11	D9										
B4	VREFB4N1	IO	DQS9T		C10	B7	DQVLD1T		DM5T	DM5T	DQS9T	DQS9T	DQ7T0	DQ7T0	DQS9T	DQS9T
B4	VREFB4N1	IO	DQ9T		C11	A7	DQ1T	DQ0T	DQ5T3	DQ5T3	DQ9T0	DQ9T0	DQ6T3	DQ6T3	DQ9T0	DQ9T0
B4	VREFB4N1	IO	DQ9T		A10	C8	DQ1T	DQ0T	DQ5T2	DQ5T2	DQ9T1	DQ9T1	DQ6T2	DQ6T2	DQ9T1	DQ9T1
B4	VREFB4N1	IO	DQ9T		D10	C7	DQ1T	DQ0T	DQS5T	DQS5T	DQ9T2	DQ9T2	DQS6T	DQS6T	DQ9T2	DQ9T2
B4	VREFB4N1	IO	DQSn9T		B10	B8	DQ1T	DQ0T	DQ5T1	DQ5T1	DQSB9T	DQSB9T	DQ6T1	DQ6T1	DQSB9T	DQSB9T
B4	VREFB4N1	IO	DQ9T		B11	A8	DQ1T		DQ5T0	DQ5T0	DQ9T3	DQ9T3	DQ6T0	DQ6T0	DQ9T3	DQ9T3
B9	VREFB4N1	IO	PLL5_FBn/OUT2n		D12	C9										
B9	VREFB4N1	IO	PLL5_FBp/OUT2p		C12	B9										

B9	VREFB4N1	IO	PLL5_OUT0n		B12	B10										
B9	VREFB4N1	IO	PLL5_OUT0p		A12	A10										
B9	VREFB4N1	IO	PLL5_OUT1n		E13	D10										
B9	VREFB4N1	IO	PLL5_OUT1p		D13	C10										
B4	VREFB4N1	IO	CLK12n		C13	C11										
B4	VREFB4N1	IO	CLK12p		B13	B11										
B4	VREFB4N1	IO	CLK13n		C14	C12										
B4	VREFB4N1	IO	CLK13p		B14	B12										
B9		VCC_PLL5_OUT			H12	G10										
		VCCD_PLL5			H14	G11										
		VCCA_PLL5			G12	F12										
		GNDA_PLL5			H13	F10										
		GNDA_PLL5			J13	F11										
B3	VREFB3N0	IO	CLK14p		A15	A13										
B3	VREFB3N0	IO	CLK14n		B15	B13										
B3	VREFB3N0	IO	CLK15p		C15	C13										
B3	VREFB3N0	IO	CLK15n		D15	D13										
B3	VREFB3N0	IO		PGM2	E15	D12										
B3	VREFB3N0	IO		PGM1	F15	E11										
B3	VREFB3N0	IO		PGM0	F14	H11										
B3	VREFB3N0	IO		ASDO	G14	G12										
B3	VREFB3N0	IO		nCSO	E14	D11										
B3	VREFB3N0	IO		CRC_ERROR	F16	E12										
B3	VREFB3N0	IO		DATA0	E16	E13										
B3	VREFB3N0	IO		DATA1	G15	H12										
B3	VREFB3N0	IO	DQS11T		B16	B15	DQS2T			DM4T	DQS11T	DQS11T		DQ5T3	DQS11T	DQS11T
B3	VREFB3N0	IO	DQ11T		C16	A15	DQ2T	DQ1T		DQ4T3	DQ11T0	DQ11T0		DQ5T2	DQ11T0	DQ11T0
B3	VREFB3N0	IO	DQ11T		A17	C15	DQ2T	DQ1T	DM4T	DQ4T2	DQ11T1	DQ11T1	DQ5T3	DQS5T	DQ11T1	DQ11T1
B3	VREFB3N0	IO	DQ11T		C17	C16	DQ2T	DQ1T	DQ4T3	DQS4T	DQ11T2	DQ11T2	DQ5T2	DQ5T1	DQ11T2	DQ11T2
B3	VREFB3N0	VREFB3N0	VREFB3N0		D16	B14										
B3	VREFB3N0	IO	DQSn11T		B17	B16	DQSn2T	DQ1T	DQ4T2	DQ4T1	DQSB11T	DQSB11T	DQS5T	DQ5T0	DQSB11T	DQSB11T
B3	VREFB3N0	IO	DQ11T		A18	A16	DQ2T	DQ1T	DQS4T	DQ4T0	DQ11T3	DQ11T3	DQ5T1	DQ4T3	DQ11T3	DQ11T3
B3	VREFB3N0	IO			D17	F13			DQ4T1	DM3T			DQ5T0	DQ4T2		
B3	VREFB3N0	IO			G16	G13			DQ4T0	DQ3T3			DQ4T3	DQS4T		
B3	VREFB3N0	IO	DQS13T		B18	B17	DQVLD2T	DQS1T	DM3T	DQ3T2	DQS13T	DQS13T	DQ4T2	DQ4T1	DQS13T	DQS13T
B3	VREFB3N0	IO	DQ13T		A19	A17	DQ2T	DQ1T	DQ3T3	DQS3T	DQ13T0	DQ13T0	DQS4T	DQ4T0	DQ13T0	DQ13T0
B3	VREFB3N0	IO	DQ13T		C18	A18	DQ2T	DQ1T	DQ3T2	DQ3T1	DQ13T1	DQ13T1	DQ4T1	DQ3T3	DQ13T1	DQ13T1
B3	VREFB3N0	IO	DQ13T		C19	C17	DQ2T	DQ1T	DQS3T	DQ3T0	DQ13T2	DQ13T2	DQ4T0	DQ3T2	DQ13T2	DQ13T2
B3	VREFB3N0	IO	DQSn13T		B19	B18	DQ2T	DQSn1T	DQ3T1	DM2T	DQSB13T	DQSB13T	DQ3T3	DQS3T	DQSB13T	DQSB13T
B3	VREFB3N0	IO	DQ13T		A20	C18	DQ2T	DQ1T	DQ3T0	DQ2T3	DQ13T3	DQ13T3	DQ3T2	DQ3T1	DQ13T3	DQ13T3
B3	VREFB3N0	IO			E17	C14			DM2T	DQ2T2			DQS3T	DQ3T0		
B3	VREFB3N0	IO			F17	D14			DQ2T3	DQS2T			DQ3T1	DQ2T3		
B3	VREFB3N1	IO	DQS15T		B20	E14	DQS3T	DQVLD1T	DQ2T2	DQ2T1	DQS15T		DQ3T0	DQ2T2	DQS15T	
B3	VREFB3N1	IO	DQ15T		A21	G14	DQ3T	DQ1T	DQS2T	DQ2T0	DQ15T0		DQ2T3	DQS2T	DQ15T0	
B3	VREFB3N1	IO	DQ15T		C20	F14	DQ3T	DQ1T	DQ2T1	DM1T	DQ15T1		DQ2T2	DQ2T1	DQ15T1	
B3	VREFB3N1	IO	DQ15T		C21	H14	DQ3T	DQ1T	DQ2T0	DQ1T3	DQ15T2		DQS2T	DQ2T0	DQ15T2	
B3	VREFB3N1	IO	DQSn15T		B21	D15	DQSn3T	DQ1T	DM1T	DQ1T2	DQSB15T		DQ2T1	DQ1T3	DQSB15T	
B3	VREFB3N1	IO	DQ15T		A22		DQ3T	DQ1T	DQ1T3		DQ15T3		DQ2T0		DQ15T3	
B3	VREFB3N1	IO			D18	F16			DQ1T2	DQS1T			DQ1T3	DQ1T2		
B3	VREFB3N1	IO			G17	J15			DQS1T	DQ1T1			DQ1T2	DQS1T		
B3	VREFB3N1	IO	DQS17T		B23	E15	DQVLD3T		DQ1T1	DQ1T0	DQS17T	DQS17T	DQS1T	DQ1T1	DQS17T	DQS17T
B3	VREFB3N1	IO	DQ17T		C22	F15	DQ3T	DQ1T	DQ1T0	DM0T	DQ17T0	DQ17T0	DQ1T1	DQ1T0	DQ17T0	DQ17T0
B3	VREFB3N1	IO	DQ17T		B22	G15	DQ3T	DQ1T	DM0T	DQ0T3	DQ17T1	DQ17T1	DQ1T0	DQ0T3	DQ17T1	DQ17T1

B3	VREFB3N1	IO	DQ17T		A24	H16	DQ3T	DQ1T	DQ0T3	DQ0T2	DQ17T2	DQ17T2	DQ0T3	DQ0T2	DQ17T2	DQ17T2
B3	VREFB3N1	VREFB3N1	VREFB3N1		D22	D16										
B3	VREFB3N1	IO	DQSn17T		C23	C19	DQ3T	DQ1T	DQ0T2	DQS0T	DQSB17T	DQSB17T	DQ0T2	DQS0T	DQSB17T	DQSB17T
B3	VREFB3N1	IO	DQ17T		B24	D20	DQ3T		DQS0T	DQ0T1	DQ17T3	DQ17T3	DQS0T	DQ0T1	DQ17T3	DQ17T3
B3	VREFB3N1	IO			E18	G16			DQ0T1	DQ0T0			DQ0T1	DQ0T0		
B3	VREFB3N1	IO			G18				DQ0T0				DQ0T0			
B3	VREFB3N1	IO		DATA2	E19	D17										
B3	VREFB3N1	IO		DATA3	D20	A19										
B3	VREFB3N1	IO		DATA4	G19	E16										
B3	VREFB3N1	IO		DATA5	D19	E17										
B3	VREFB3N1	IO		DATA6	E20	B19										
B3	VREFB3N1	IO		DATA7	F20	D18										
B3	VREFB3N1	IO		RDYnBSY	F19	F17										
B3	VREFB3N1	IO		INIT_DONE	D21	E18										
B3	VREFB3N1	nSTATUS		nSTATUS	E21	B20										
B3	VREFB3N1	nCE		nCE	E22	A21										
B3	VREFB3N1	DCLK		DCLK	C24	D19										
B3	VREFB3N1	CONF_DONE		CONF_DONE	B25	C20										
		VCCIO2			D26	B22										
		VCCIO2			L26	L22										
		VCCIO2			M17											
		VCCIO1			AC26	AA22										
		VCCIO1			P17	M22										
		VCCIO1			T26											
		VCCIO8			AF16	AB12										
		VCCIO8			AF23	AB20										
		VCCIO8			U14											
		VCCIO7			AF4	AB3										
		VCCIO7			AF11	AB11										
		VCCIO7			U12											
		VCCIO6			AC1	AA1										
		VCCIO6			R10	M1										
		VCCIO6			T1											
		VCCIO5			D1	B1										
		VCCIO5			L1	L1										
		VCCIO5			N10											
		VCCIO4			A4	A3										
		VCCIO4			A11	A11										
		VCCIO4			K13											
		VCCIO3			A16	A12										
		VCCIO3			A23	A20										
		VCCIO3			K15											
		VCCINT			L10	H8										
		VCCINT			L12	J9										
		VCCINT			L14	J11										
		VCCINT			L16	J13										
		VCCINT			M11	K10										
		VCCINT			M13	K12										
		VCCINT			M15	L11										
		VCCINT			N12	L13										
		VCCINT			N14	M8										
		VCCINT			N16	M10										
		VCCINT			P11	M12										

		VCCINT			P13	M14										
		VCCINT			P15	N11										
		VCCINT			R12	N13										
		VCCINT			R14	P9										
		VCCINT			R16	P12										
		VCCINT			T11	P14										
		VCCINT			T13											
		VCCINT			T15											
		VCCINT			T17											
		VCCINT			U10											
		VCCINT			U16											
		VCCINT			U18											
		VCCINT			V9											
		GND			A2	A1										
		GND			A13	A9										
		GND			A14											
		GND			A25	A14										
		GND			AA13	A22										
		GND			AE1											
		GND			AE26	AA2										
		GND			AF2	AA21										
		GND			AF13											
		GND			AF14	AB1										
		GND			AF25	AB9										
		GND			B1											
		GND			B26	AB14										
		GND			G13	AB22										
		GND			K12											
		GND			K14	B2										
		GND			L11	B21										
		GND			L13											
		GND			L15	H15										
		GND			L17	J1										
		GND			M10											
		GND			M12	J10										
		GND			M14	J12										
		GND			M16											
		GND			N1	J14										
		GND			N11	J22										
		GND			N13	K9										
		GND			N15	K11										
		GND			N17	K13										
		GND			N26	L10										
		GND			P1	L12										
		GND			P6	L14										
		GND			P10	M7										
		GND			P12	M9										
		GND			P14	M11										
		GND			P16	M13										
		GND			P26	M15										
		GND			R11	N10										
		GND			R13	N12										
		GND			R15	N14										

		GND			R17	P1										
		GND			R22	P11										
		GND			T10	P13										
		GND			T12	P22										
		GND			T14	R10										
		GND			T16											
		GND			T18											
		GND			U9											
		GND			U11											
		GND			U13											
		GND			U15											
		GND			U17											
		VCCPD2			M18	K14										
		VCCPD1			R18	P15										
		VCCPD8			V15	R13										
		VCCPD7			V11	P10										
		VCCPD6			R9	N9										
		VCCPD5			M9	L9										
		VCCPD4			J12	H10										
		VCCPD3			J16	H13										
		NC			AA3											
		NC			AA4											
		NC			AA5											
		NC			AA6											
		NC			AA8											
		NC			AA9											
		NC			AA18											
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		NC			AA22											
		NC			AB3											
		NC			AB4											
		NC			AB7											
		NC			AB8											
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		NC			AC2											
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		NC			AC15											
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		NC			AC24											
		NC			AC25											
		NC			AD1											
		NC			AD2											
		NC			AD15											
		NC			AD25											
		NC			AD26											
		NC			C1											
		NC			C2											
		NC			C25											
		NC			C26											

		NC			D2											
		NC			D3											
		NC			D4											
		NC			D14											
		NC			D23											
		NC			D24											
		NC			D25											
		NC			E1											
		NC			E2											
		NC			E3											
		NC			E4											
		NC			E23											
		NC			E24											
		NC			E25											
		NC			E26											
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		NC			F2											
		NC			F3											
		NC			F4											
		NC			F8											
		NC			F9											
		NC			F12											
		NC			F13											
		NC			F18											
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		NC			F22											
		NC			F23											
		NC			F24											
		NC			F25											
		NC			F26											
		NC			G6											
		NC			G7											
		NC			G9											
		NC			G10											
		NC			G11											
		NC			G20											
		NC			G21											
		NC			H5											
		NC			H6											
		NC			H7											
		NC			H8											
		NC			H9											
		NC			H10											
		NC			H11											
		NC			H15											
		NC			H16											
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		NC			H18											
		NC			H19											
		NC			H20											
		NC			H21											
		NC			H22											
		NC			J5											

		NC			J6											
		NC			J7											
		NC			J8											
		NC			J9											
		NC			J10											
		NC			J11											
		NC			J14											
		NC			J15											
		NC			J17											
		NC			J18											
		NC			J19											
		NC			J20											
		NC			J21											
		NC			J22											
		NC			K6											
		NC			K7											
		NC			K10											
		NC			K11											
		NC			K16											
		NC			K17											
		NC			K18											
		NC			V10											
		NC			V12											
		NC			V14											
		NC			V16											
		NC			V17											
		NC			V18											
		NC			V19											
		NC			V20											
		NC			W5											
		NC			W6											
		NC			W7											
		NC			W8											
		NC			W9											
		NC			W10											
		NC			W11											
		NC			W12											
		NC			W15											
		NC			W16											
		NC			W19											
		NC			W20											
		NC			Y6											
		NC			Y7											
		NC			Y9											
		NC			Y11											
		NC			Y12											
		NC			Y20											
		NC			Y21											

(1) Optional Functions (LVDS, DDR, etc) are not available for some pins in certain packages; e.g., for EP2S15, DQ3B group is available for package F672 but not for F484.

(2) The DQS/DQ mode shown in this column applies to the largest device package in the pin list. Smaller packages may not have the pins to support some of the DQS groups. To determine the supported DQS/DQ groups, check the corresponding pin availability for the targeted device package. For e.g. in EP2S15F484 package, only two x16 groups and no x18 groups are available.

(3) This mode is used for x4 DDR2 SDRAM (with DM support) devices and x9 RLDRAM II devices

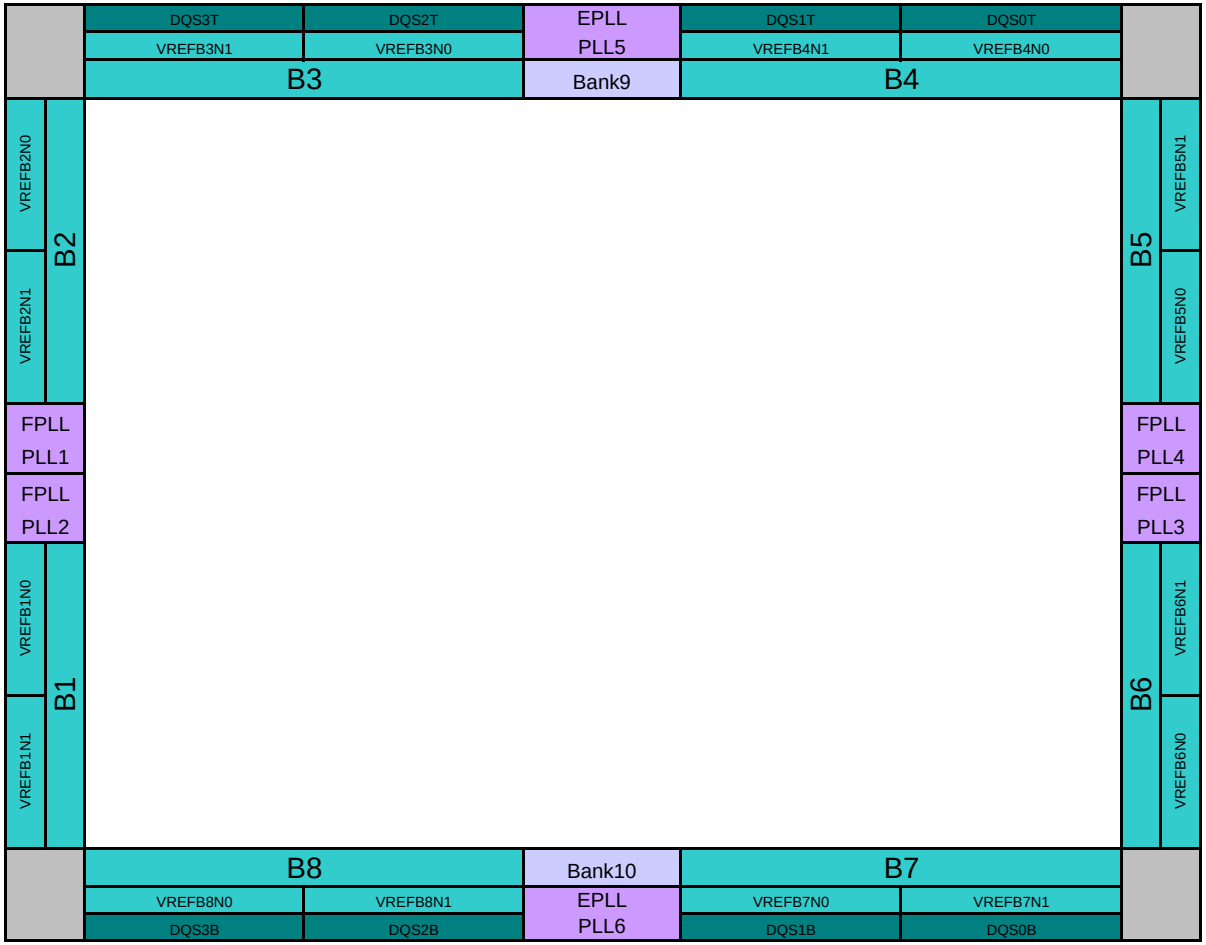
(4) This mode is used for DDR/DDR2 SDRAM, RLDRAM II, and QDRII SRAM interfaces, except for x9 RLDRAM II devices. This mode can support x4 DDR2 SDRAM devices if the DM pins are not used.			
(5) Vref pins are required when using DDR, DDR2, and QDR2 pins. For more information about the value of the Vref pins, refer to *Selectable I/O Standards in Stratix II & Stratix II GX Devices* chapter in volume 2 of the Stratix II Handbook.			

Pin Name	Pin Type (1st, 2nd, and 3rd Function)	Pin Description
		Supply and Reference Pins
VCCINT	Power	These are internal logic array voltage supply pins. VCCINT also supplies power to the input buffers used for the LVDS, LVPECL, HyperTransport™ technology, differential HSTL, differential SSTL, HSTL, and SSTL I/O standards. All VCCINT pins must be connected to 1.2 V.
VCCIO[1..8]	Power	These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all I/O standards. VCCIO also supplies power to the input buffers used for the LVTTL, LVCMOS, 1.5 V, 1.8 V, 2.5 V, 3.3-V PCI, and 3.3-V PCI-X I/O standards.
VCCPD[1..8]	Power	Dedicated power pins. This supply is used to power the I/O pre-drivers and the 3.3-V/2.5-V buffers of the configuration input pins and the JTAG pins. VCCPD powers the JTAG pins (TCK, TMS, TDI, and TRST) and the following configuration pins: nCONFIG, DCLK (when used as an input), nIO_Pullup, DATA[7..0], RUnLU, nCE, nWS, nRS, CS, nCS, and CLKUSR. The VCCPD pins must be connected to 3.3 V and must ramp-up from 0 V to 3.3 V within 100 ms to ensure successful configuration. If you use the AES key programming feature of the device, VCCPD8 powers the circuitry enabling the key to be programmed in non-volatile memory. During key programming, apply 3.7 V to VCCPD8. Refer to AN341-Using the Design Security Feature in Stratix II and Stratix II GX devices for more information.
GND	Ground	Device ground pins. All GND pins should be connected to the board GND plane.
VREFB[1..8]N[0..1]	Input	Input reference voltage for each I/O bank. If a bank is used for a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for that bank. All the VREF pins within a bank are shorted togetherIf VREF pins are not used, designers should connect them to either VCC or GND.
VCC_PLL5_OUT	Power	External clock output VCCIO power for PLL5 clock outputs PLL5_OUT[1..0]p, PLL5_OUT[1..0]n, PLL5_FBp/OUT2p, and PLL5_FBn/OUT2n. This pin is the VCCIO pin for bank 9.
VCC_PLL6_OUT	Power	External clock output VCCIO power for PLL6 clock outputs PLL6_OUT[1..0]p, PLL6_OUT[1..0]n, PLL6_FBp/OUT2p, and PLL6_FBn/OUT2n. This pin is the VCCIO pin for bank 10.
VCCA_PLL[1..6]	Power	Analog power for PLLs[1..6]. The designer must connect these pins to 1.2 V, even if the PLL is not used.
VCCD_PLL[1..6]	Power	Digital power for PLLs[1..6]. The designer must connect these pins to 1.2 V, even if the PLL is not used.
GNDA_PLL[1..6]	Ground	Analog ground for PLLs[1..6].
NC	No Connect	Do not drive signals into these pins.
RUP4	I/O, Input	Reference pin for banks 3 and 4. The external precision resistor Rup must be connected to the designated RUP pin within bank 4. If not required, this pin is a regular I/O pin.
RDN4	I/O, Input	Reference pin for banks 3 and 4. The external precision resistor Rdn must be connected to the designated RDN pin within bank 4. If not required, this pin is a regular I/O pin.
RUP7	I/O, Input	Reference pin for banks 7 and 8. The external precision resistor Rup must be connected to the designated RUP pin within bank 7. If not required, this pin is a regular I/O pin.
RDN7	I/O, Input	Reference pin for banks 7 and 8. The external precision resistor Rdn must be connected to the designated RDN pin within bank 7. If not required, this pin is a regular I/O pin.
		Dedicated Configuration/JTAG Pins
nIO_PULLUP	Input	Dedicated input that chooses whether the internal pull-ups on the user I/O pins and dual-purpose I/O pins (nCSO ASDO, DATA[7..0], nWS, nRS, RDYnBSY, nCS, CS, RUnLU, PGM[], CLKUSR, INIT_DONE, DEV_OE, DEV_CLRn) are on or off before and during configuration. A logic high (1.5 V, 1.8 V, 2.5 V, or 3.3 V) turns off the weak pull-up, while a logic low turns them on.
VCCSEL	Input	Dedicated input that selects which input buffer is used on configuration input pins: nCONFIG, DCLK (when used as an input), DATA[7..0], RUnLU, nCE, nWS, nRS, CS, nCS, and CLKUSR. The 3.3-V/2.5-V input buffer is powered by VCCPD, while the 1.8-V/1.5-V input buffer is powered by VCCIO. The VCCSEL input buffer is powered by VCCPD and must be hardwired to VCCPD or ground. A logic high (VCCPD) selects the 1.8-V/1.5-V input buffer, while a logic low selects the 3.3-V/2.5-V input buffer. VCCSEL should be set to comply with the logi levels driven out of the configuration device or MAX II device/microprocessor with flash memory.
TEMPDIODEp	Input	Pin used in conjunction with the temperature sensing diode (bias-high input) inside the Stratix II device. If the temperature sensing diode is not used then connect this pin to GND.

Pin Name	Pin Type (1st, 2nd, and 3rd Function)	Pin Description
TEMPDIODEn	Input	Pin used in conjunction with the temperature sensing diode (bias-low input) inside the Stratix II device. If the temperature sensing diode is not used then connect this pin to GND.
DCLK	Input (PS, FPP) Output (AS)	Dedicated configuration clock pin. In PS and FPP configuration, DCLK is used to clock configuration data from an external source into the Stratix II device. In AS mode, DCLK is an output from the Stratix II device that provides timing for the configuration interface. In PPA mode, DCLK should be tied to VCC to prevent this pin from floating.
MSEL[0..3]	Input	Configuration input pins that set the Stratix II device configuration scheme. These pins must be hardwired to VCCPD or GND.
nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled. In multi-device configuration, nCE of the first device is tied low while its nCEO pin drives the nCE of the next device in the chain. In single device configuration, nCE is tied low.
nCONFIG	Input	Dedicated configuration control input. Pulling this pin low during user-mode will cause the FPGA to lose its configuration data, enter a reset state, and tri-state all I/O pins. Returning this pin to a logic high level will initiate reconfiguration. If the configuration scheme uses an enhanced configuration device or EPC2, nCONFIG can be tied directly to VCC or to the configuration device's nINIT_CONF pin.
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration status pin. As a status output, the CONF_DONE pin drives low before and during configuration. Once all configuration data is received without error and the initialization cycle starts, CONF_DONE is released. As a status input, CONF_DONE goes high after all data is received. Then the device initializes and enters user mode. It is not available as a user I/O pin.
nCEO	Output	Output that drives low when device configuration is complete. During multi-device configuration, this pin feeds a subsequent device's nCE pin. During single device configuration, this pin is left floating.
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin. The FPGA drives nSTATUS low immediately after power-up and releases it after POR time. As a status output, the nSTATUS is pulled low if an error occurs during configuration. As a status input, the device enters an error state when nSTATUS is driven low by an external source during configuration or initialization. It is not available as a user I/O pin.
PORSEL	Input	Dedicated input which selects between a POR time of 12 ms or 100 ms. A logic high (1.5-V, 1.8-V, 2.5-V, 3.3-V) selects a POR time of about 12 ms and a logic low selects POR time of about 100 ms.
TCK	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TCK to GND.
TMS	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TMS to VCC.
TDI	Input	Dedicated JTAG input pin. The JTAG circuitry can be disabled by connecting TDI to VCC
TDO	Output	Dedicated JTAG output pin. The JTAG circuitry can be disabled by leaving TDO unconnected
TRST	Input	Dedicated active low JTAG input pin. TRST is used to asynchronously reset the JTAG boundary-scan circuit. The JTAG circuitry can be disabled by connecting TRST to GND.
		Clock and PLL Pins
CLK[1,3,9,11]p	Clock, Input	Dedicated clock input pins 1, 3, 9, and 11 that can also be used for data inputs
CLK[1,3,9,11]n	Clock, Input	Dedicated negative terminal clock input pins for differential clock input that can also be used for data inputs.
CLK[0,2,8,10]p/DIFFIO_RX_C[0..3]p	I/O, Clock, RX channel	These pins can be used as I/O pins, clock input pins, or the positive terminal data pins of differential receiver channels.
CLK[0,2,8,10]n/DIFFIO_RX_C[0..3]n	I/O, Clock, RX channel	These pins can be used as I/O pins, the negative terminal clock input pins for differential clock input, or the negative terminal data pins of differential receiver channels.
CLK[4-7,12-15]p	I/O, Clock	These pins can be used as I/O pins or clock input pins
CLK[4-7,12-15]n	I/O, Clock	These pins can be used as I/O pins or negative terminal clock input pins for differential clock input
PLL_ENA	Input	Dedicated input pin that drives the optional pllena port of all or a set of PLLs. If a PLL uses the pllena port, drive the PLL_ENA pin low to reset all PLLs including the counters to their default state. If VCCSEL = 0, then you mus drive the PLL_ENA with a 3.3/2.5 V signal to enable the PLLs. If VCCSEL = 1, connect PLL_ENA to 1.8/1.5 V to enable the PLLs.
PLL5_OUT[0..1]p	I/O, Output	Optional external clock outputs [0..1] from enhanced PLL 5. These pins can be differential (two output pin pairs) or single ended (four clock outputs from PLL5). When not used as PLL output, these pins can be used as I/O with single ended inputs only. They cannot be used as differential input.

Pin Name	Pin Type (1st, 2nd, and 3rd Function)	Pin Description
PLL5_OUT[0..1]n	I/O, Output	Optional negative terminal for external clock outputs [0..1] from PLL5. If the clock outputs are single ended, then each pair of pins (i.e., PLL5_OUT0p and PLL5_OUT0n are considered one pair) can be either in phase or 180 degrees out of phase.
PLL6_OUT[0..1]p	I/O, Output	Optional external clock outputs [0..1] from enhanced PLL 6. These pins can be differential (two output pin pairs) or single ended (four clock outputs from PLL6). When not used as PLL output, these pins can be used as I/O with single ended inputs only. They cannot be used as differential input.
PLL6_OUT[0..1]n	I/O, Output	Optional negative terminal for external clock outputs [0..1] from PLL6. If the clock outputs are single ended, then each pair of pins (i.e., PLL6_OUT0p and PLL6_OUT0n are considered one pair) can be either in phase or 180 degrees out of phase.
PLL[5..6]_FBp/OUT2p	I/O, Input, Output	These pins can be used as I/O pins, external feedback input pins or external clock outputs for PLL[5..6].
PLL[5..6]_FBn/OUT2n	I/O, Input, Output	These pins can be used as I/O pins, negative terminal input for external feedback input PLL[5..6]_FBp or negative terminal clock output pins for differential clock output.
Optional/Dual-Purpose Configuration Pins		
nCSO	I/O (non-AS mode), Output	Output control signal from the Stratix II FPGA to the serial configuration device in AS mode that enables the configuration device.
ASDO	I/O (non-AS mode), Output	Control signal from the Stratix II FPGA to the serial configuration device in AS mode used to read out configuration data.
CRC_ERROR	I/O, Output	Active high signal that indicates that the error detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error detection circuit is enabled.
DEV_CLRn	I/O, Input	Optional pin that allows you to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high, all registers behave as programmed.
DEV_OE	I/O, Input	Optional pin that allows you to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high, all I/O pins behave as defined in the design.
DATA0	I/O, Input	Dual-purpose configuration data input pin. Can be used as an I/O pin after configuration is complete
DATA[1..7]	I/O, Input	Dual-purpose configuration input data pins. These pins can be used for configuration or as regular I/O pins. These pins can also be used as user I/O pins after configuration.
DATA7	I/O, Bidirectional	In the PPA configuration scheme, the DATA7 pin presents the RDYnBSY signal after the nRS signal has been strobed low.
INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high at the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration.
nCS, CS	I/O, Input	These are chip-select inputs that enable the Stratix II device in the passive parallel asynchronous configuration mode. Drive nCS low and CS high to target a device for configuration. If a design requires an active high enable, use the CS pin and drive the nCS pin low. If a design requires an active low enable, use the nCS pin and drive the CS pin high. Configuration will be paused when either signal is inactive. Hold the nCS and CS pins active during configuration and initialization. The design can use these pins as user I/O pins after configuration.
nRS	I/O, Input	Read strobe input pin. A low input directs the device to drive the RDYnBSY signal on the DATA7 pin. If the nRS pin is not used in PPA mode, it should be tied high. In non-PPA schemes, it functions as a user I/O during configuration, which means it is tri-stated. This pin can be used as a user I/O pin after configuration.
nWS	I/O, Input	Active-low write strobe input to latch a byte of data on the DATA pins. This pin can be used as a user I/O pin after configuration.
CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. If this pin is not enable for use as a user-supplied configuration clock, it can be used as a user I/O pin.
RDYnBSY	I/O, Output	Ready not busy output. A high output indicates that the target device is ready to accept another data byte. A low output indicates that the target device is not ready to receive another data byte. This pin can be used as a user I/O pin after configuration.
PGM[0..2]	I/O, Output	These output pins control one of eight pages in the memory (either flash or enhanced configuration device) when using a remote system update mode. When not using remote update or local update configuration modes, these pins are user I/O pins.

Pin Name	Pin Type (1st, 2nd, and 3rd Function)	Pin Description
RUnLU	I/O, Input	Input that selects between remote update and local update. A logic high (1.5 V, 1.8 V, 2.5 V, 3.3 V) selects remote update and a logic low selects local update. When not using remote update or local update configuration modes, this pin is available as general-purpose user I/O pin.
Dual-Purpose Differential and External Memory Interface Pins		
DIFFIO_RX[0..37]p/n	I/O, RX channel	Dual-purpose differential receiver channels 0 to 37. These channels can be used for receiving LVDS or HyperTransport compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. Pin with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFIO_TX[0..37]p/n	I/O, TX channel	Dual-purpose differential transmitter channels 0 to 37. These channels can be used for transmitting LVDS or HyperTransport compatible signals. Pins with a "p" suffix carry the positive signal for the differential channel. Pin with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DQS[T,B]	I/O, DQS	Optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry. The shifted DQS signal can also drive to internal logic.
DQS[L,R]	I/O, DQS	Optional data strobe signal for use in external memory interfacing. These pins do not drive to dedicated DQS phase shift circuitry and are only used as write data strobe or write data clock.
DQSn[T,B]	I/O, DQSn	Optional complementary data strobe signal for use in QDRII SRAM. These pins drive to dedicated DQS phase shift circuitry.
DQ[T,B,L,R]	I/O, DQ	Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important; however, use caution when making pin assignments if you plan on migrating to a different memory interface that has a different DQ bus width. Analyze the available DQ pins across all pertinent DQS columns in the pin list.
DM[L,R]	I/O, DM	Optional data mask signal for use in external memory interfacing. You can also use this pin as a DQ pin.
DQVLD[0..3][T,B]	I/O, DQVLD	Optional data valid signal for use in external memory interfacing.



Notes:

1. This is a top view of the silicon die. For flip chip packages, the die is mounted upside down in the package; therefore, to obtain the top package view, flip this diagram on its vertical axis.
2. This is only a pictorial representation to provide an idea of placement on the device. Refer to the pin list and the Quartus® II software for exact locations.
3. The DQ/DQS groups depicted above are in x8/x9 mode for the top and bottom I/O banks where there is dedicated circuitry. DQ/DQS groups on the side I/O banks are not shown here. DQ/DQS support differs across the package offerings.

Version Number	Date	Changes Made
1.0	2/18/2004	Initial revision
1.1	3/31/2004	Changed pin name from CLK[10,8,2,0]p to CLK[10,8,2,0]p/DIFFIO_RX_C[3..0]p & CLK[10,8,2,0]n to CLK[10,8,2,0]n/DIFFIO_RX_C[3..0]n in Pin List
1.2	4/21/2004	Added the dual-purpose RUP[4,7] and RDN[4,7] signals to the pin list and the pin definitions sheet
1.3	7/14/2004	Added CRC_ERROR pin to pin list and pin definitions sheet
1.4	9/10/2004	Removed DQ bit indices
		Updated DQ and NC definitions
1.5	10/6/2004	File status changed to Final
1.6	6/27/2005	Updated Pin List to include DQS for x4
		Updated Pin Description for VCCPD
1.7	9/29/2005	Added DQ group for non-DQS mode columns in pin list:
		Added footnote for pins that do not support Optional Functions (LVDS, DDR, etc)
		Added footnote to explain x5 Mode and x4 Mode in non-DQS Mode
1.8	2/10/2006	Added footnote to address usage of Vref pins in external memory interface usage
1.9	6/16/2006	Changed VCC_PLLx_out definitions from "This pin should be connected to the VCCIO level of bank x" to "This pin is the VCCIO pin for bank x".
		Added input usage informations for PLLx_OUT[0..1]p
2.0	2/13/2007	Removed redundant rows and updated the description for VCCPD8 during key programming.
2.1	6/11/2007	Added footnote for x8/x9 and x16/x18 modes on the availabilty of DQ group in smaller package.