Pin Information for the Stratix® IV E EP4SE360 Device
Version 1.2

Bank Number	VREF	Pin Name/ Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	Dynamic OCT Support	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780
1A		TDI		TDI			F24	No			
1A		TMS		TMS			H22	No			
1A		TRST		TRST			D26	No			
1A		TCK		TCK			C26	No			
1A		TDO		TDO			G24	No			
1A	VREFB1AN0	IO	PLL_L1_CLKOUT0n		DIFFIO_TX_L1n	DIFFOUT_L1n	F26	Yes			
1A	VREFB1AN0	IO	PLL_L1_FB_CLKOUT0p		DIFFIO_TX_L1p	DIFFOUT_L1p	F25	Yes			
1A	VREFB1AN0	IO	RDN1A		DIFFIO_RX_L1n	DIFFOUT_L2n	C28	Yes			
1A	VREFB1AN0	IO	RUP1A		DIFFIO_RX_L1p	DIFFOUT_L2p	D27	Yes			
1A	VREFB1AN0	IO			DIFFIO_TX_L2n	DIFFOUT_L3n	G26	Yes	DQ1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L2p	DIFFOUT_L3p	G25	Yes	DQ1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L2n	DIFFOUT_L4n	B28	Yes	DQSn1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L2p	DIFFOUT_L4p	C27	Yes	DQS1L	DQ1L/CQn1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L3n	DIFFOUT_L5n	H25	Yes	DQ1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L3p	DIFFOUT_L5p	J24	Yes	DQ1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L3n	DIFFOUT_L6n	D28	Yes	DQSn2L	DQSn1L/DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L3p	DIFFOUT_L6p	E28	Yes	DQS2L	DQS1L/CQ1L	DQ1L/CQn1L
1A	VREFB1AN0	IO			DIFFIO_TX_L4n	DIFFOUT_L7n	J23	Yes	DQ2L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L4p	DIFFOUT_L7p	J22	Yes	DQ2L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L4n	DIFFOUT_L8n	F28	Yes	DQ2L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L4p	DIFFOUT_L8p	F27	Yes	DQ2L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L5n	DIFFOUT_L9n	K21	Yes	DQ3L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L5p	DIFFOUT_L9p	K20	Yes	DQ3L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L5n	DIFFOUT_L10n	G28	Yes	DQSn3L	DQ2L	DQSn1L/DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L5p	DIFFOUT_L10p	G27	Yes	DQS3L	DQ2L/CQn2L	DQS1L/CQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L6n	DIFFOUT_L11n	K26	Yes	DQ3L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L6p	DIFFOUT_L11p	K25	Yes	DQ3L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L6n	DIFFOUT_L12n	J26	Yes	DQSn4L	DQSn2L/DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L6p	DIFFOUT_L12p	J25	Yes	DQS4L	DQS2L/CQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L7n	DIFFOUT_L13n	K24	Yes	DQ4L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L7p	DIFFOUT_L13p	K23	Yes	DQ4L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L7n	DIFFOUT_L14n	H28	Yes	DQ4L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L7p	DIFFOUT_L14p	J27	Yes	DQ4L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L8n	DIFFOUT_L15n	L23	Yes			
1A	VREFB1AN0	IO			DIFFIO_TX_L8p	DIFFOUT_L15p	L22	Yes			
1A	VREFB1AN0	IO			DIFFIO_RX_L8n	DIFFOUT_L16n	J28	Yes			
1A	VREFB1AN0	IO			DIFFIO_RX_L8p	DIFFOUT_L16p	K27	Yes			
1C	VREFB1CN0	IO			DIFFIO_TX_L17n	DIFFOUT_L33n	M23	Yes			
1C	VREFB1CN0	IO			DIFFIO_TX_L17p	DIFFOUT_L33p	M22	Yes			
1C	VREFB1CN0	IO			DIFFIO_RX_L17n	DIFFOUT_L34n	L26	Yes	DQSn8L		
1C	VREFB1CN0	IO			DIFFIO_RX_L17p	DIFFOUT_L34p	L25	Yes	DQS8L		
1C	VREFB1CN0	IO		CLKUSR	DIFFIO_TX_L18n	DIFFOUT_L35n	M21	Yes	DQ8L		
1C	VREFB1CN0	IO			DIFFIO_TX_L18p	DIFFOUT_L35p	M20	Yes	DQ8L		
1C	VREFB1CN0	IO			DIFFIO_RX_L18n	DIFFOUT_L36n	K28	Yes	DQ8L		
1C	VREFB1CN0	IO			DIFFIO_RX_L18p	DIFFOUT_L36p	L28	Yes	DQ8L		
1C	VREFB1CN0	IO		DATA0	DIFFIO_TX_L19n	DIFFOUT_L37n	N21	Yes	DQ9L	DQ8L	
1C	VREFB1CN0	IO		DATA1	DIFFIO_TX_L19p	DIFFOUT_L37p	N20	Yes	DQ9L	DQ8L	
1C	VREFB1CN0	IO		DATA2	DIFFIO_RX_L19n	DIFFOUT_L38n	M26	Yes	DQSn9L	DQ8L	
1C	VREFB1CN0	IO		DATA3	DIFFIO_RX_L19p	DIFFOUT_L38p	M25	Yes	DQS9L	DQ8L/CQn8L	
1C	VREFB1CN0	IO		DATA4	DIFFIO_TX_L20n	DIFFOUT_L39n	N25	Yes	DQ9L	DQ8L	
1C	VREFB1CN0	IO		DATA5	DIFFIO_TX_L20p	DIFFOUT_L39p	M24	Yes	DQ9L	DQ8L	
1C	VREFB1CN0	IO		DATA6	DIFFIO_RX_L20n	DIFFOUT_L40n	M28	Yes	DQSn10L	DQSn8L/DQ8L	
1C	VREFB1CN0	IO		DATA7	DIFFIO_RX_L20p	DIFFOUT_L40p	M27	Yes	DQS10L	DQS8L/CQ8L	
1C	VREFB1CN0	IO		INIT_DONE	DIFFIO_TX_L21n	DIFFOUT_L41n	N23	Yes	DQ10L	DQ8L	
1C	VREFB1CN0	IO		CRC_ERROR	DIFFIO_TX_L21p	DIFFOUT_L41p	P23	Yes	DQ10L	DQ8L	
1C	VREFB1CN0	IO		DEV_OE	DIFFIO_RX_L21n	DIFFOUT_L42n	P25	Yes	DQ10L	DQ8L	
1C	VREFB1CN0	IO		DEV_CLRn	DIFFIO_RX_L21p	DIFFOUT_L42p	N24	Yes	DQ10L	DQ8L	
1C	VREFB1CN0	IO	PLL_L2_CLKOUT0n		DIFFIO_TX_L22n	DIFFOUT_L43n	P20	No			
1C	VREFB1CN0	IO	PLL_L2_FB_CLKOUT0p		DIFFIO_TX_L22p	DIFFOUT_L43p	P19	No			
1C	VREFB1CN0	IO	CLK0n		DIFFIO_RX_L22n	DIFFOUT_L44n	N27	No			

Bank Number	VREF	Pin Name/ Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	Dynamic OCT Support	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780
1C	VREFB1CN0	IO	CLK0p		DIFFIO_RX_L22p	DIFFOUT_L44p	N26	No			
1C	VREFB1CN0	CLK1n	CLK1n				N28	No			
1C	VREFB1CN0	CLK1p	CLK1p				P28	No			
2C	VREFB2CN0	CLK3p	CLK3p				R27	No			
2C	VREFB2CN0	CLK3n	CLK3n				R28	No			
2C	VREFB2CN0	IO	CLK2p		DIFFIO_RX_L23p	DIFFOUT_L45p	U28	No			
2C	VREFB2CN0	IO	CLK2n		DIFFIO_RX_L23n	DIFFOUT_L45n	T28	No			
2C	VREFB2CN0	IO	PLL_L3_FB_CLKOUT0p		DIFFIO_TX_L23p	DIFFOUT_L46p	R20	No			
2C	VREFB2CN0	IO	PLL_L3_CLKOUT0n		DIFFIO_TX_L23n	DIFFOUT_L46n	R21	No			
2C	VREFB2CN0	IO			DIFFIO_RX_L24p	DIFFOUT_L47p	R26	Yes	DQ17L	DQ19L	
2C	VREFB2CN0	IO			DIFFIO_RX_L24n	DIFFOUT_L47n	T27	Yes	DQ17L	DQ19L	
2C	VREFB2CN0	IO			DIFFIO_TX_L24p	DIFFOUT_L48p	T25	Yes	DQ17L	DQ19L	
2C	VREFB2CN0	IO			DIFFIO_TX_L24n	DIFFOUT_L48n	R25	Yes	DQ17L	DQ19L	
2C	VREFB2CN0	IO			DIFFIO_RX_L25p	DIFFOUT_L49p	V27	Yes	DQS17L	DQS19L/CQ19L	
2C	VREFB2CN0	IO			DIFFIO_RX_L25n	DIFFOUT_L49n	V28	Yes	DQSn17L	DQSn19L/DQ19L	
2C	VREFB2CN0	IO			DIFFIO_TX_L25p	DIFFOUT_L50p	T20	Yes	DQ18L	DQ19L	
2C	VREFB2CN0	IO			DIFFIO_TX_L25n	DIFFOUT_L50n	T21	Yes	DQ18L	DQ19L	
2C	VREFB2CN0	IO			DIFFIO_RX_L26p	DIFFOUT_L51p	V26	Yes	DQS18L	DQ19L/CQn19L	
2C	VREFB2CN0	IO			DIFFIO_RX_L26n	DIFFOUT_L51n	U26	Yes	DQSn18L	DQ19L	
2C	VREFB2CN0	IO			DIFFIO_TX_L26p	DIFFOUT_L52p	T24	Yes	DQ18L	DQ19L	
2C	VREFB2CN0	IO			DIFFIO_TX_L26n	DIFFOUT_L52n	U25	Yes	DQ18L	DQ19L	
2C	VREFB2CN0	IO			DIFFIO_RX_L27p	DIFFOUT_L53p	W27	Yes	DQ19L		
2C	VREFB2CN0	IO			DIFFIO_RX_L27n	DIFFOUT_L53n	W28	Yes	DQ19L		
2C	VREFB2CN0	IO			DIFFIO_TX_L27p	DIFFOUT_L54p	T22	Yes	DQ19L		
2C	VREFB2CN0	IO			DIFFIO_TX_L27n	DIFFOUT_L54n	T23	Yes	DQ19L		
2C	VREFB2CN0	IO			DIFFIO_RX_L28p	DIFFOUT_L55p	V24	Yes	DQS19L		
2C	VREFB2CN0	IO			DIFFIO_RX_L28n	DIFFOUT_L55n	V25	Yes	DQSn19L		
2C	VREFB2CN0	IO			DIFFIO_TX_L28p	DIFFOUT_L56p	V23	Yes			
2C	VREFB2CN0	IO			DIFFIO_TX_L28n	DIFFOUT_L56n	U23	Yes			
2A	VREFB2AN0	IO			DIFFIO_RX_L37p	DIFFOUT_L73p	AA27	Yes			
2A	VREFB2AN0	IO			DIFFIO_RX_L37n	DIFFOUT_L73n	Y28	Yes			
2A	VREFB2AN0	IO			DIFFIO_TX_L37p	DIFFOUT_L74p	W22	Yes			
2A	VREFB2AN0	IO			DIFFIO_TX_L37n	DIFFOUT_L74n	W23	Yes			
2A	VREFB2AN0	IO			DIFFIO_RX_L38p	DIFFOUT_L75p	AB27	Yes	DQ23L	DQ25L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_RX_L38n	DIFFOUT_L75n	AA28	Yes	DQ23L	DQ25L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L38p	DIFFOUT_L76p	W24	Yes	DQ23L	DQ25L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L38n	DIFFOUT_L76n	W25	Yes	DQ23L	DQ25L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_RX_L39p	DIFFOUT_L77p	Y25	Yes	DQS23L	DQS25L/CQ25L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_RX_L39n	DIFFOUT_L77n	Y26	Yes	DQSn23L	DQSn25L/DQ25L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L39p	DIFFOUT_L78p	V20	Yes	DQ24L	DQ25L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L39n	DIFFOUT_L78n	V21	Yes	DQ24L	DQ25L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_RX_L40p	DIFFOUT_L79p	AC28	Yes	DQS24L	DQ25L/CQn25L	DQS26L/CQ26L
2A	VREFB2AN0	IO			DIFFIO_RX_L40n	DIFFOUT_L79n	AB28	Yes	DQSn24L	DQ25L	DQSn26L/DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L40p	DIFFOUT_L80p	AA25	Yes	DQ24L	DQ25L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L40n	DIFFOUT_L80n	AA26	Yes	DQ24L	DQ25L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_RX_L41p	DIFFOUT_L81p	AB25	Yes	DQ25L	DQ26L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_RX_L41n	DIFFOUT_L81n	AB26	Yes	DQ25L	DQ26L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L41p	DIFFOUT_L82p	AC25	Yes	DQ25L	DQ26L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L41n	DIFFOUT_L82n	AC26	Yes	DQ25L	DQ26L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_RX_L42p	DIFFOUT_L83p	AD27	Yes	DQS25L	DQS26L/CQ26L	DQ26L/CQn26L
2A	VREFB2AN0	IO			DIFFIO_RX_L42n	DIFFOUT_L83n	AD28	Yes	DQSn25L	DQSn26L/DQ26L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L42p	DIFFOUT_L84p	W20	Yes	DQ26L	DQ26L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L42n	DIFFOUT_L84n	W21	Yes	DQ26L	DQ26L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_RX_L43p	DIFFOUT_L85p	AG28	Yes	DQS26L	DQ26L/CQn26L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_RX_L43n	DIFFOUT_L85n	AF28	Yes	DQSn26L	DQ26L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L43p	DIFFOUT_L86p	Y23	Yes	DQ26L	DQ26L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L43n	DIFFOUT_L86n	AA24	Yes	DQ26L	DQ26L	DQ26L
2A	VREFB2AN0	IO	RUP2A		DIFFIO_RX_L44p	DIFFOUT_L87p	AE27	Yes			
2A	VREFB2AN0	IO	RDN2A		DIFFIO_RX_L44n	DIFFOUT_L87n	AE28	Yes			
2A	VREFB2AN0	IO	PLL_L4_FB_CLKOUT0p		DIFFIO_TX_L44p	DIFFOUT_L88p	AA23	Yes			

Bank Number	VREF	Pin Name/ Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	Dynamic OCT Support	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780
2A	VREFB2AN0	IO	PLL_L4_CLKOUT0n		DIFFIO_TX_L44n	DIFFOUT_L88n	AB24	Yes			
		nCONFIG		nCONFIG			W19	No			
		nSTATUS		nSTATUS			AD25	No			
		CONF_DONE		CONF_DONE			AE26	No			
		PORSEL					AB23	No			
		nCE		nCE			Y20	No			
3A	VREFB3AN0	IO				DIFFOUT_B1n	AF26	Yes	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B1p	AH27	Yes	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO	RDN3A		DIFFIO_RX_B1n	DIFFOUT_B2n	AH25	Yes	DQSn1B	DQ1B	DQ1B
3A	VREFB3AN0	IO	RUP3A		DIFFIO_RX_B1p	DIFFOUT_B2p	AG25	Yes	DQS1B	DQ1B/CQn1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B3n	AG27	Yes	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B3p	AH26	Yes	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B2n	DIFFOUT_B4n	AE22	Yes	DQSn2B	DQSn1B/DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B2p	DIFFOUT_B4p	AD22	Yes	DQS2B	DQS1B/CQ1B	DQ1B/CQn1B
3A	VREFB3AN0	IO				DIFFOUT_B5n	AB20	Yes	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B5p	AB21	Yes	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B3n	DIFFOUT_B6n	AD21	Yes	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B3p	DIFFOUT_B6p	AC21	Yes	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B7n	AD24	Yes	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B7p	AE23	Yes	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B4n	DIFFOUT_B8n	AF24	Yes	DQSn3B	DQ2B	DQSn1B/DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B4p	DIFFOUT_B8p	AE24	Yes	DQS3B	DQ2B/CQn2B	DQS1B/CQ1B
3A	VREFB3AN0	IO				DIFFOUT_B9n	AF23	Yes	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B9p	AG24	Yes	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B5n	DIFFOUT_B10n	AH24	Yes	DQSn4B	DQSn2B/DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B5p	DIFFOUT_B10p	AH23	Yes	DQS4B	DQS2B/CQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B11n	AH20	Yes	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B11p	AH21	Yes	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B6n	DIFFOUT_B12n	AH22	Yes	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B6p	DIFFOUT_B12p	AG22	Yes	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B13n	AC20	Yes	DQ5B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B13p	AG21	Yes	DQ5B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B7n	DIFFOUT_B14n	AF21	Yes	DQSn5B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B7p	DIFFOUT_B14p	AE21	Yes	DQS5B	DQ3B/CQn3B	
3A	VREFB3AN0	IO				DIFFOUT_B15n	AF20	Yes	DQ5B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B15p	AE20	Yes	DQ5B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B8n	DIFFOUT_B16n	AD19	Yes	DQSn6B	DQSn3B/DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B8p	DIFFOUT_B16p	AC19	Yes	DQS6B	DQS3B/CQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B17n	AB19	Yes	DQ6B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B17p	AA19	Yes	DQ6B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B9n	DIFFOUT_B18n	AE19	Yes	DQ6B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B9p	DIFFOUT_B18p	AD18	Yes	DQ6B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B19n	Y19	Yes			
3A	VREFB3AN0	IO				DIFFOUT_B19p	AA18	Yes			
3A	VREFB3AN0	IO			DIFFIO_RX_B10n	DIFFOUT_B20n	Y18	Yes			
3A	VREFB3AN0	IO			DIFFIO_RX_B10p	DIFFOUT_B20p	Y17	Yes			
3C	VREFB3CN0	IO				DIFFOUT_B49n	AF19	Yes	DQ17B	DQ17B	
3C	VREFB3CN0	IO				DIFFOUT_B49p	AG19	Yes	DQ17B	DQ17B	
3C	VREFB3CN0	IO			DIFFIO_RX_B25n	DIFFOUT_B50n	AH19	Yes	DQSn17B	DQ17B	
3C	VREFB3CN0	IO			DIFFIO_RX_B25p	DIFFOUT_B50p	AG18	Yes	DQS17B	DQ17B/CQn17B	
3C	VREFB3CN0	IO				DIFFOUT_B51n	AH17	Yes	DQ17B	DQ17B	
3C	VREFB3CN0	IO				DIFFOUT_B51p	AH18	Yes	DQ17B	DQ17B	
3C	VREFB3CN0	IO			DIFFIO_RX_B26n	DIFFOUT_B52n	AF17	Yes	DQSn18B	DQSn17B/DQ17B	
3C	VREFB3CN0	IO			DIFFIO_RX_B26p	DIFFOUT_B52p	AE18	Yes	DQS18B	DQS17B/CQ17B	
3C	VREFB3CN0	IO				DIFFOUT_B53n	AE16	Yes	DQ18B	DQ17B	
3C	VREFB3CN0	IO				DIFFOUT_B53p	AD16	Yes	DQ18B	DQ17B	
3C	VREFB3CN0	IO			DIFFIO_RX_B27n	DIFFOUT_B54n	AF16	Yes	DQ18B	DQ17B	
3C	VREFB3CN0	IO			DIFFIO_RX_B27p	DIFFOUT_B54p	AE17	Yes	DQ18B	DQ17B	
3C	VREFB3CN0	IO	PLL_B1_CLKOUT4			DIFFOUT_B59n	AC17	No			
3C	VREFB3CN0	IO	PLL_B1_CLKOUT3			DIFFOUT_B59p	AB17	No			

Bank Number	VREF	Pin Name/ Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	Dynamic OCT Support	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780
3C	VREFB3CN0	IO			DIFFIO_RX_B30n	DIFFOUT_B60n	AC16	No			
3C	VREFB3CN0	IO			DIFFIO_RX_B30p	DIFFOUT_B60p	AB16	No			
3C	VREFB3CN0	IO	PLL_B1_CLKOUT0n			DIFFOUT_B61n	AA15	No			
3C	VREFB3CN0	IO	PLL_B1_CLKOUT0p			DIFFOUT_B61p	Y15	No			
3C	VREFB3CN0	IO	PLL_B1_FBn/CLKOUT2		DIFFIO_RX_B31n	DIFFOUT_B62n	AH16	No			
3C	VREFB3CN0	IO	PLL_B1_FBp/CLKOUT1		DIFFIO_RX_B31p	DIFFOUT_B62p	AG16	No			
3C	VREFB3CN0	IO	CLK5n			DIFFOUT_B63n	AH15	No			
3C	VREFB3CN0	IO	CLK5p			DIFFOUT_B63p	AG15	No			
3C	VREFB3CN0	IO	CLK4n		DIFFIO_RX_B32n	DIFFOUT_B64n	AF15	No			
3C	VREFB3CN0	IO	CLK4p		DIFFIO_RX_B32p	DIFFOUT_B64p	AE15	No			
4C	VREFB4CN0	IO	CLK6p		DIFFIO_RX_B33p	DIFFOUT_B65p	AE14	No			
4C	VREFB4CN0	IO	CLK6n		DIFFIO_RX_B33n	DIFFOUT_B65n	AF14	No			
4C	VREFB4CN0	IO	CLK7p			DIFFOUT_B66p	AG13	No			
4C	VREFB4CN0	IO	CLK7n			DIFFOUT_B66n	AH14	No			
4C	VREFB4CN0	IO			DIFFIO_RX_B36p	DIFFOUT_B71p	AG12	Yes			
4C	VREFB4CN0	IO			DIFFIO_RX_B36n	DIFFOUT_B71n	AH13	Yes			
4C	VREFB4CN0	IO				DIFFOUT_B72p	Y13	Yes	DQ20B		
4C	VREFB4CN0	IO				DIFFOUT_B72n	Y14	Yes	DQ20B		
4C	VREFB4CN0	IO			DIFFIO_RX_B37p	DIFFOUT_B73p	AD13	Yes	DQS20B		
4C	VREFB4CN0	IO			DIFFIO_RX_B37n	DIFFOUT_B73n	AE13	Yes	DQSn20B		
4C	VREFB4CN0	IO				DIFFOUT_B74p	AA13	Yes	DQ20B		
4C	VREFB4CN0	IO				DIFFOUT_B74n	AB13	Yes	DQ20B		
4C	VREFB4CN0	IO			DIFFIO_RX_B38p	DIFFOUT_B75p	AG10	Yes	DQ21B	DQ22B	
4C	VREFB4CN0	IO			DIFFIO_RX_B38n	DIFFOUT_B75n	AH10	Yes	DQ21B	DQ22B	
4C	VREFB4CN0	IO				DIFFOUT_B76p	AH11	Yes	DQ21B	DQ22B	
4C	VREFB4CN0	IO				DIFFOUT_B76n	AH12	Yes	DQ21B	DQ22B	
4C	VREFB4CN0	IO			DIFFIO_RX_B39p	DIFFOUT_B77p	AF10	Yes	DQS21B	DQS22B/CQ22B	
4C	VREFB4CN0	IO			DIFFIO_RX_B39n	DIFFOUT_B77n	AF11	Yes	DQSn21B	DQSn22B/DQ22B	
4C	VREFB4CN0	IO				DIFFOUT_B78p	AF12	Yes	DQ22B	DQ22B	
4C	VREFB4CN0	IO				DIFFOUT_B78n	AC12	Yes	DQ22B	DQ22B	
4C	VREFB4CN0	IO			DIFFIO_RX_B40p	DIFFOUT_B79p	AD12	Yes	DQS22B	DQ22B/CQn22B	
4C	VREFB4CN0	IO			DIFFIO_RX_B40n	DIFFOUT_B79n	AE12	Yes	DQSn22B	DQ22B	
4C	VREFB4CN0	IO				DIFFOUT_B80p	AC11	Yes	DQ22B	DQ22B	
4C	VREFB4CN0	IO				DIFFOUT_B80n	AE11	Yes	DQ22B	DQ22B	
4A	VREFB4AN0	IO			DIFFIO_RX_B55p	DIFFOUT_B109p	AB11	Yes			
4A	VREFB4AN0	IO			DIFFIO_RX_B55n	DIFFOUT_B109n	AC10	Yes			
4A	VREFB4AN0	IO				DIFFOUT_B110p	Y10	Yes			
4A	VREFB4AN0	IO				DIFFOUT_B110n	Y11	Yes			
4A	VREFB4AN0	IO			DIFFIO_RX_B56p	DIFFOUT_B111p	AG9	Yes	DQ33B	DQ36B	
4A	VREFB4AN0	IO			DIFFIO_RX_B56n	DIFFOUT_B111n	AH8	Yes	DQ33B	DQ36B	
4A	VREFB4AN0	IO				DIFFOUT_B112p	AE10	Yes	DQ33B	DQ36B	
4A	VREFB4AN0	IO				DIFFOUT_B112n	AH9	Yes	DQ33B	DQ36B	
4A	VREFB4AN0	IO			DIFFIO_RX_B57p	DIFFOUT_B113p	AE9	Yes	DQS33B	DQS36B/CQ36B	
4A	VREFB4AN0	IO			DIFFIO_RX_B57n	DIFFOUT_B113n	AF9	Yes	DQSn33B	DQSn36B/DQ36B	
4A	VREFB4AN0	IO				DIFFOUT_B114p	AF8	Yes	DQ34B	DQ36B	
4A	VREFB4AN0	IO				DIFFOUT_B114n	AE8	Yes	DQ34B	DQ36B	
4A	VREFB4AN0	IO			DIFFIO_RX_B58p	DIFFOUT_B115p	AG7	Yes	DQS34B	DQ36B/CQn36B	
4A	VREFB4AN0	IO			DIFFIO_RX_B58n	DIFFOUT_B115n	AH7	Yes	DQSn34B	DQ36B	
4A	VREFB4AN0	IO				DIFFOUT_B116p	AG6	Yes	DQ34B	DQ36B	
4A	VREFB4AN0	IO				DIFFOUT_B116n	AH6	Yes	DQ34B	DQ36B	
4A	VREFB4AN0	IO			DIFFIO_RX_B59p	DIFFOUT_B117p	AG4	Yes	DQ35B	DQ37B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B59n	DIFFOUT_B117n	AH3	Yes	DQ35B	DQ37B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B118p	AH4	Yes	DQ35B	DQ37B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B118n	AH5	Yes	DQ35B	DQ37B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B60p	DIFFOUT_B119p	AG3	Yes	DQS35B	DQS37B/CQ37B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B60n	DIFFOUT_B119n	AH2	Yes	DQSn35B	DQSn37B/DQ37B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B120p	AD9	Yes	DQ36B	DQ37B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B120n	AC9	Yes	DQ36B	DQ37B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B61p	DIFFOUT_B121p	AA9	Yes	DQS36B	DQ37B/CQn37B	DQS38B/CQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B61n	DIFFOUT_B121n	AB9	Yes	DQSn36B	DQ37B	DQSn38B/DQ38B

Bank Number	VREF	Pin Name/ Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	Dynamic OCT Support	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780
4A	VREFB4AN0	IO				DIFFOUT_B122p	Y9	Yes	DQ36B	DQ37B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B122n	AA10	Yes	DQ36B	DQ37B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B62p	DIFFOUT_B123p	AE6	Yes	DQ37B	DQ38B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B62n	DIFFOUT_B123n	AF6	Yes	DQ37B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B124p	AE4	Yes	DQ37B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B124n	AE7	Yes	DQ37B	DQ38B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B63p	DIFFOUT_B125p	AE5	Yes	DQS37B	DQS38B/CQ38B	DQ38B/CQn38B
4A	VREFB4AN0	IO			DIFFIO_RX_B63n	DIFFOUT_B125n	AF5	Yes	DQSn37B	DQSn38B/DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B126p	AB8	Yes	DQ38B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B126n	AC8	Yes	DQ38B	DQ38B	DQ38B
4A	VREFB4AN0	IO	RUP4A		DIFFIO_RX_B64p	DIFFOUT_B127p	AC7	Yes	DQS38B	DQ38B/CQn38B	DQ38B
4A	VREFB4AN0	IO	RDN4A		DIFFIO_RX_B64n	DIFFOUT_B127n	AD7	Yes	DQSn38B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B128p	AB7	Yes	DQ38B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B128n	AD6	Yes	DQ38B	DQ38B	DQ38B
		nIO_PULLUP		nIO_PULLUP			AE3	No			
		nCEO		nCEO			AB5	No			
		DCLK		DCLK			AC5	No			
		nCSO		nCSO			AD4	No			
		ASDO		ASDO			AA6	No			
5A	VREFB5AN0	IO	PLL_R4_CLKOUT0n		DIFFIO_TX_R1n	DIFFOUT_R1n	AC3	Yes			
5A	VREFB5AN0	IO	PLL_R4_FB_CLKOUT0p		DIFFIO_TX_R1p	DIFFOUT_R1p	AC4	Yes			
5A	VREFB5AN0	IO	RDN5A		DIFFIO_RX_R1n	DIFFOUT_R2n	AF1	Yes			
5A	VREFB5AN0	IO	RUP5A		DIFFIO_RX_R1p	DIFFOUT_R2p	AE2	Yes			
5A	VREFB5AN0	IO			DIFFIO_TX_R2n	DIFFOUT_R3n	AB3	Yes	DQ1R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R2p	DIFFOUT_R3p	AB4	Yes	DQ1R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R2n	DIFFOUT_R4n	AG1	Yes	DQSn1R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R2p	DIFFOUT_R4p	AF2	Yes	DQS1R	DQ1R/CQn1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R3n	DIFFOUT_R5n	Y6	Yes	DQ1R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R3p	DIFFOUT_R5p	Y7	Yes	DQ1R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R3n	DIFFOUT_R6n	AE1	Yes	DQSn2R	DQSn1R/DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R3p	DIFFOUT_R6p	AD1	Yes	DQS2R	DQS1R/CQ1R	DQ1R/CQn1R
5A	VREFB5AN0	IO			DIFFIO_TX_R4n	DIFFOUT_R7n	AA4	Yes	DQ2R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R4p	DIFFOUT_R7p	Y5	Yes	DQ2R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R4n	DIFFOUT_R8n	AC1	Yes	DQ2R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R4p	DIFFOUT_R8p	AC2	Yes	DQ2R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R5n	DIFFOUT_R9n	Y3	Yes	DQ3R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R5p	DIFFOUT_R9p	Y4	Yes	DQ3R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R5n	DIFFOUT_R10n	AB1	Yes	DQSn3R	DQ2R	DQSn1R/DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R5p	DIFFOUT_R10p	AB2	Yes	DQS3R	DQ2R/CQn2R	DQS1R/CQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R6n	DIFFOUT_R11n	W8	Yes	DQ3R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R6p	DIFFOUT_R11p	W9	Yes	DQ3R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R6n	DIFFOUT_R12n	AA1	Yes	DQSn4R	DQSn2R/DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R6p	DIFFOUT_R12p	Y2	Yes	DQS4R	DQS2R/CQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R7n	DIFFOUT_R13n	W5	Yes	DQ4R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R7p	DIFFOUT_R13p	W6	Yes	DQ4R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R7n	DIFFOUT_R14n	Y1	Yes	DQ4R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R7p	DIFFOUT_R14p	W2	Yes	DQ4R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R8n	DIFFOUT_R15n	V6	Yes			
5A	VREFB5AN0	IO			DIFFIO_TX_R8p	DIFFOUT_R15p	V7	Yes			
5A	VREFB5AN0	IO			DIFFIO_RX_R8n	DIFFOUT_R16n	W3	Yes			
5A	VREFB5AN0	IO			DIFFIO_RX_R8p	DIFFOUT_R16p	W4	Yes			
5C	VREFB5CN0	IO			DIFFIO_TX_R17n	DIFFOUT_R33n	U6	Yes			
5C	VREFB5CN0	IO			DIFFIO_TX_R17p	DIFFOUT_R33p	U7	Yes			
5C	VREFB5CN0	IO			DIFFIO_RX_R17n	DIFFOUT_R34n	V3	Yes	DQSn8R		
5C	VREFB5CN0	IO			DIFFIO_RX_R17p	DIFFOUT_R34p	V4	Yes	DQS8R		
5C	VREFB5CN0	IO			DIFFIO_TX_R18n	DIFFOUT_R35n	U8	Yes	DQ8R		
5C	VREFB5CN0	IO			DIFFIO_TX_R18p	DIFFOUT_R35p	U9	Yes	DQ8R		
5C	VREFB5CN0	IO			DIFFIO_RX_R18n	DIFFOUT_R36n	W1	Yes	DQ8R		
5C	VREFB5CN0	IO			DIFFIO_RX_R18p	DIFFOUT_R36p	V1	Yes	DQ8R		
5C	VREFB5CN0	IO			DIFFIO_TX_R19n	DIFFOUT_R37n	T4	Yes	DQ9R	DQ8R	

Bank Number	VREF	Pin Name/ Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	Dynamic OCT Support	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780
5C	VREFB5CN0	IO			DIFFIO_TX_R19p	DIFFOUT_R37p	U5	Yes	DQ9R	DQ8R	
5C	VREFB5CN0	IO			DIFFIO_RX_R19n	DIFFOUT_R38n	U3	Yes	DQSn9R	DQ8R	
5C	VREFB5CN0	IO			DIFFIO_RX_R19p	DIFFOUT_R38p	U4	Yes	DQS9R	DQ8R/CQn8R	
5C	VREFB5CN0	IO			DIFFIO_TX_R20n	DIFFOUT_R39n	T8	Yes	DQ9R	DQ8R	
5C	VREFB5CN0	IO			DIFFIO_TX_R20p	DIFFOUT_R39p	T9	Yes	DQ9R	DQ8R	
5C	VREFB5CN0	IO			DIFFIO_RX_R20n	DIFFOUT_R40n	T2	Yes	DQSn10R	DQSn8R/DQ8R	
5C	VREFB5CN0	IO			DIFFIO_RX_R20p	DIFFOUT_R40p	T3	Yes	DQS10R	DQS8R/CQ8R	
5C	VREFB5CN0	IO			DIFFIO_TX_R21n	DIFFOUT_R41n	T6	Yes	DQ10R	DQ8R	
5C	VREFB5CN0	IO			DIFFIO_TX_R21p	DIFFOUT_R41p	R6	Yes	DQ10R	DQ8R	
5C	VREFB5CN0	IO			DIFFIO_RX_R21n	DIFFOUT_R42n	R4	Yes	DQ10R	DQ8R	
5C	VREFB5CN0	IO			DIFFIO_RX_R21p	DIFFOUT_R42p	T5	Yes	DQ10R	DQ8R	
5C	VREFB5CN0	IO	PLL_R3_CLKOUT0n		DIFFIO_TX_R22n	DIFFOUT_R43n	R9	No			
5C	VREFB5CN0	IO	PLL_R3_FB_CLKOUT0p		DIFFIO_TX_R22p	DIFFOUT_R43p	R10	No			
5C	VREFB5CN0	IO	CLK9n		DIFFIO_RX_R22n	DIFFOUT_R44n	U1	No			
5C	VREFB5CN0	IO	CLK9p		DIFFIO_RX_R22p	DIFFOUT_R44p	U2	No			
5C	VREFB5CN0	CLK8n	CLK8n				T1	No			
5C	VREFB5CN0	CLK8p	CLK8p				R1	No			
6C	VREFB6CN0	CLK10p	CLK10p				P2	No			
6C	VREFB6CN0	CLK10n	CLK10n				P1	No			
6C	VREFB6CN0	IO	CLK11p		DIFFIO_RX_R23p	DIFFOUT_R45p	M1	No			
6C	VREFB6CN0	IO	CLK11n		DIFFIO_RX_R23n	DIFFOUT_R45n	N1	No			
6C	VREFB6CN0	IO	PLL_R2_FB_CLKOUT0p		DIFFIO_TX_R23p	DIFFOUT_R46p	P9	No			
6C	VREFB6CN0	IO	PLL_R2_CLKOUT0n		DIFFIO_TX_R23n	DIFFOUT_R46n	P8	No			
6C	VREFB6CN0	IO			DIFFIO_RX_R24p	DIFFOUT_R47p	N4	Yes	DQ17R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_RX_R24n	DIFFOUT_R47n	P4	Yes	DQ17R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_TX_R24p	DIFFOUT_R48p	N7	Yes	DQ17R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_TX_R24n	DIFFOUT_R48n	N6	Yes	DQ17R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_RX_R25p	DIFFOUT_R49p	P3	Yes	DQS17R	DQS19R/CQ19R	
6C	VREFB6CN0	IO			DIFFIO_RX_R25n	DIFFOUT_R49n	N2	Yes	DQSn17R	DQSn19R/DQ19R	
6C	VREFB6CN0	IO			DIFFIO_TX_R25p	DIFFOUT_R50p	N5	Yes	DQ18R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_TX_R25n	DIFFOUT_R50n	M4	Yes	DQ18R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_RX_R26p	DIFFOUT_R51p	L2	Yes	DQS18R	DQ19R/CQn19R	
6C	VREFB6CN0	IO			DIFFIO_RX_R26n	DIFFOUT_R51n	L1	Yes	DQSn18R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_TX_R26p	DIFFOUT_R52p	N9	Yes	DQ18R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_TX_R26n	DIFFOUT_R52n	N8	Yes	DQ18R	DQ19R	
6C	VREFB6CN0	IO			DIFFIO_RX_R27p	DIFFOUT_R53p	L3	Yes	DQ19R		
6C	VREFB6CN0	IO			DIFFIO_RX_R27n	DIFFOUT_R53n	M3	Yes	DQ19R		
6C	VREFB6CN0	IO			DIFFIO_TX_R27p	DIFFOUT_R54p	L5	Yes	DQ19R		
6C	VREFB6CN0	IO			DIFFIO_TX_R27n	DIFFOUT_R54n	L4	Yes	DQ19R		
6C	VREFB6CN0	IO			DIFFIO_RX_R28p	DIFFOUT_R55p	K2	Yes	DQS19R		
6C	VREFB6CN0	IO			DIFFIO_RX_R28n	DIFFOUT_R55n	K1	Yes	DQSn19R		
6C	VREFB6CN0	IO			DIFFIO_TX_R28p	DIFFOUT_R56p	L6	Yes			
6C	VREFB6CN0	IO			DIFFIO_TX_R28n	DIFFOUT_R56n	M6	Yes			
6A	VREFB6AN0	IO			DIFFIO_RX_R37p	DIFFOUT_R73p	H2	Yes			
6A	VREFB6AN0	IO			DIFFIO_RX_R37n	DIFFOUT_R73n	J1	Yes			
6A	VREFB6AN0	IO			DIFFIO_TX_R37p	DIFFOUT_R74p	K7	Yes			
6A	VREFB6AN0	IO			DIFFIO_TX_R37n	DIFFOUT_R74n	K6	Yes			
6A	VREFB6AN0	IO			DIFFIO_RX_R38p	DIFFOUT_R75p	G2	Yes	DQ23R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R38n	DIFFOUT_R75n	H1	Yes	DQ23R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R38p	DIFFOUT_R76p	K5	Yes	DQ23R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R38n	DIFFOUT_R76n	K4	Yes	DQ23R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R39p	DIFFOUT_R77p	F1	Yes	DQS23R	DQS25R/CQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R39n	DIFFOUT_R77n	G1	Yes	DQSn23R	DQSn25R/DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R39p	DIFFOUT_R78p	J4	Yes	DQ24R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R39n	DIFFOUT_R78n	J3	Yes	DQ24R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R40p	DIFFOUT_R79p	E2	Yes	DQS24R	DQ25R/CQn25R	DQS26R/CQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R40n	DIFFOUT_R79n	E1	Yes	DQSn24R	DQ25R	DQSn26R/DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R40p	DIFFOUT_R80p	L9	Yes	DQ24R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R40n	DIFFOUT_R80n	L8	Yes	DQ24R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R41p	DIFFOUT_R81p	H4	Yes	DQ25R	DQ26R	DQ26R

Bank Number	VREF	Pin Name/ Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	Dynamic OCT Support	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780
6A	VREFB6AN0	IO			DIFFIO_RX_R41n	DIFFOUT_R81n	H3	Yes	DQ25R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R41p	DIFFOUT_R82p	K9	Yes	DQ25R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R41n	DIFFOUT_R82n	K8	Yes	DQ25R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R42p	DIFFOUT_R83p	D2	Yes	DQS25R	DQS26R/CQ26R	DQ26R/CQn26R
6A	VREFB6AN0	IO			DIFFIO_RX_R42n	DIFFOUT_R83n	D1	Yes	DQSn25R	DQSn26R/DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R42p	DIFFOUT_R84p	J6	Yes	DQ26R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R42n	DIFFOUT_R84n	H5	Yes	DQ26R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R43p	DIFFOUT_R85p	F4	Yes	DQS26R	DQ26R/CQn26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R43n	DIFFOUT_R85n	F3	Yes	DQSn26R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R43p	DIFFOUT_R86p	G4	Yes	DQ26R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R43n	DIFFOUT_R86n	G3	Yes	DQ26R	DQ26R	DQ26R
6A	VREFB6AN0	IO	RUP6A		DIFFIO_RX_R44p	DIFFOUT_R87p	B1	Yes			
6A	VREFB6AN0	IO	RDN6A		DIFFIO_RX_R44n	DIFFOUT_R87n	C1	Yes			
6A	VREFB6AN0	IO	PLL_R1_FB_CLKOUT0p		DIFFIO_TX_R44p	DIFFOUT_R88p	H6	Yes			
6A	VREFB6AN0	IO	PLL_R1_CLKOUT0n		DIFFIO_TX_R44n	DIFFOUT_R88n	G5	Yes			
		MSEL2		MSEL2			G7	No			
		MSEL1		MSEL1			J9	No			
		MSEL0		MSEL0			H8	No			
7A	VREFB7AN0	IO				DIFFOUT_T1n	A2	Yes	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T1p	C3	Yes	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO	RDN7A		DIFFIO_RX_T1n	DIFFOUT_T2n	A4	Yes	DQSn1T	DQ1T	DQ1T
7A	VREFB7AN0	IO	RUP7A		DIFFIO_RX_T1p	DIFFOUT_T2p	B4	Yes	DQS1T	DQ1T/CQn1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T3n	A3	Yes	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T3p	B2	Yes	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T2n	DIFFOUT_T4n	D7	Yes	DQSn2T	DQSn1T/DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T2p	DIFFOUT_T4p	E7	Yes	DQS2T	DQS1T/CQ1T	DQ1T/CQn1T
7A	VREFB7AN0	IO				DIFFOUT_T5n	G8	Yes	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T5p	G9	Yes	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T3n	DIFFOUT_T6n	E8	Yes	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T3p	DIFFOUT_T6p	F8	Yes	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T7n	D6	Yes	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T7p	E5	Yes	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T4n	DIFFOUT_T8n	C5	Yes	DQSn3T	DQ2T	DQSn1T/DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T4p	DIFFOUT_T8p	D5	Yes	DQS3T	DQ2T/CQn2T	DQS1T/CQ1T
7A	VREFB7AN0	IO				DIFFOUT_T9n	B5	Yes	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T9p	C6	Yes	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T5n	DIFFOUT_T10n	A5	Yes	DQSn4T	DQSn2T/DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T5p	DIFFOUT_T10p	A6	Yes	DQS4T	DQS2T/CQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T11n	A8	Yes	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T11p	A9	Yes	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T6n	DIFFOUT_T12n	A7	Yes	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T6p	DIFFOUT_T12p	B7	Yes	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T13n	B8	Yes	DQ5T	DQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T13p	F9	Yes	DQ5T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T7n	DIFFOUT_T14n	C8	Yes	DQSn5T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T7p	DIFFOUT_T14p	D8	Yes	DQS5T	DQ3T/CQn3T	
7A	VREFB7AN0	IO				DIFFOUT_T15n	D9	Yes	DQ5T	DQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T15p	C9	Yes	DQ5T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T8n	DIFFOUT_T16n	E10	Yes	DQSn6T	DQSn3T/DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T8p	DIFFOUT_T16p	F10	Yes	DQS6T	DQS3T/CQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T17n	H10	Yes	DQ6T	DQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T17p	G10	Yes	DQ6T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T9n	DIFFOUT_T18n	D10	Yes	DQ6T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T9p	DIFFOUT_T18p	E11	Yes	DQ6T	DQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T19n	H11	Yes			
7A	VREFB7AN0	IO				DIFFOUT_T19p	J10	Yes			
7A	VREFB7AN0	IO			DIFFIO_RX_T10n	DIFFOUT_T20n	J11	Yes			
7A	VREFB7AN0	IO			DIFFIO_RX_T10p	DIFFOUT_T20p	J12	Yes			
7C	VREFB7CN0	IO				DIFFOUT_T49n	B10	Yes	DQ17T	DQ17T	
7C	VREFB7CN0	IO				DIFFOUT_T49p	C10	Yes	DQ17T	DQ17T	

Bank Number	VREF	Pin Name/ Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	Dynamic OCT Support	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780
7C	VREFB7CN0	IO			DIFFIO_RX_T25n	DIFFOUT_T50n	A10	Yes	DQSn17T	DQ17T	
7C	VREFB7CN0	IO			DIFFIO_RX_T25p	DIFFOUT_T50p	B11	Yes	DQS17T	DQ17T/CQn17T	
7C	VREFB7CN0	IO				DIFFOUT_T51n	A11	Yes	DQ17T	DQ17T	
7C	VREFB7CN0	IO				DIFFOUT_T51p	A12	Yes	DQ17T	DQ17T	
7C	VREFB7CN0	IO			DIFFIO_RX_T26n	DIFFOUT_T52n	C12	Yes	DQSn18T	DQSn17T/DQ17T	
7C	VREFB7CN0	IO			DIFFIO_RX_T26p	DIFFOUT_T52p	D11	Yes	DQS18T	DQS17T/CQ17T	
7C	VREFB7CN0	IO				DIFFOUT_T53n	E13	Yes	DQ18T	DQ17T	
7C	VREFB7CN0	IO				DIFFOUT_T53p	D13	Yes	DQ18T	DQ17T	
7C	VREFB7CN0	IO			DIFFIO_RX_T27n	DIFFOUT_T54n	C13	Yes	DQ18T	DQ17T	
7C	VREFB7CN0	IO			DIFFIO_RX_T27p	DIFFOUT_T54p	D12	Yes	DQ18T	DQ17T	
7C	VREFB7CN0	IO				DIFFOUT_T55n	G12	Yes	DQ19T		
7C	VREFB7CN0	IO				DIFFOUT_T55p	F12	Yes	DQ19T		
7C	VREFB7CN0	IO			DIFFIO_RX_T28n	DIFFOUT_T56n	F13	Yes	DQSn19T		
7C	VREFB7CN0	IO			DIFFIO_RX_T28p	DIFFOUT_T56p	G13	Yes	DQS19T		
7C	VREFB7CN0	IO				DIFFOUT_T57n	H14	Yes	DQ19T		
7C	VREFB7CN0	IO				DIFFOUT_T57p	J14	Yes	DQ19T		
7C	VREFB7CN0	IO			DIFFIO_RX_T29n	DIFFOUT_T58n	A13	Yes			
7C	VREFB7CN0	IO			DIFFIO_RX_T29p	DIFFOUT_T58p	B13	Yes			
7C	VREFB7CN0	IO	CLK13n			DIFFOUT_T63n	A14	No			
7C	VREFB7CN0	IO	CLK13p			DIFFOUT_T63p	B14	No			
7C	VREFB7CN0	IO	CLK12n		DIFFIO_RX_T32n	DIFFOUT_T64n	C14	No			
7C	VREFB7CN0	IO	CLK12p		DIFFIO_RX_T32p	DIFFOUT_T64p	D14	No			
8C	VREFB8CN0	IO	CLK14p		DIFFIO_RX_T33p	DIFFOUT_T65p	D15	No			
8C	VREFB8CN0	IO	CLK14n		DIFFIO_RX_T33n	DIFFOUT_T65n	C15	No			
8C	VREFB8CN0	IO	CLK15p			DIFFOUT_T66p	B16	No			
8C	VREFB8CN0	IO	CLK15n			DIFFOUT_T66n	A15	No			
8C	VREFB8CN0	IO	PLL_T1_FBp/CLKOUT1		DIFFIO_RX_T34p	DIFFOUT_T67p	B17	No			
8C	VREFB8CN0	IO	PLL_T1_FBn/CLKOUT2		DIFFIO_RX_T34n	DIFFOUT_T67n	A16	No			
8C	VREFB8CN0	IO	PLL_T1_CLKOUT0p			DIFFOUT_T68p	J16	No			
8C	VREFB8CN0	IO	PLL_T1_CLKOUT0n			DIFFOUT_T68n	J15	No			
8C	VREFB8CN0	IO			DIFFIO_RX_T35p	DIFFOUT_T69p	E16	No			
8C	VREFB8CN0	IO			DIFFIO_RX_T35n	DIFFOUT_T69n	D16	No			
8C	VREFB8CN0	IO	PLL_T1_CLKOUT3			DIFFOUT_T70p	G16	No			
8C	VREFB8CN0	IO	PLL_T1_CLKOUT4			DIFFOUT_T70n	H16	No			
8C	VREFB8CN0	IO			DIFFIO_RX_T38p	DIFFOUT_T75p	B19	Yes	DQ21T	DQ22T	
8C	VREFB8CN0	IO			DIFFIO_RX_T38n	DIFFOUT_T75n	A19	Yes	DQ21T	DQ22T	
8C	VREFB8CN0	IO				DIFFOUT_T76p	A17	Yes	DQ21T	DQ22T	
8C	VREFB8CN0	IO				DIFFOUT_T76n	A18	Yes	DQ21T	DQ22T	
8C	VREFB8CN0	IO			DIFFIO_RX_T39p	DIFFOUT_T77p	C19	Yes	DQS21T	DQS22T/CQ22T	
8C	VREFB8CN0	IO			DIFFIO_RX_T39n	DIFFOUT_T77n	C18	Yes	DQSn21T	DQSn22T/DQ22T	
8C	VREFB8CN0	IO				DIFFOUT_T78p	F17	Yes	DQ22T	DQ22T	
8C	VREFB8CN0	IO				DIFFOUT_T78n	C17	Yes	DQ22T	DQ22T	
8C	VREFB8CN0	IO			DIFFIO_RX_T40p	DIFFOUT_T79p	E17	Yes	DQS22T	DQ22T/CQn22T	
8C	VREFB8CN0	IO			DIFFIO_RX_T40n	DIFFOUT_T79n	D17	Yes	DQSn22T	DQ22T	
8C	VREFB8CN0	IO				DIFFOUT_T80p	D18	Yes	DQ22T	DQ22T	
8C	VREFB8CN0	IO				DIFFOUT_T80n	F18	Yes	DQ22T	DQ22T	
8A	VREFB8AN0	IO			DIFFIO_RX_T55p	DIFFOUT_T109p	G18	Yes			
8A	VREFB8AN0	IO			DIFFIO_RX_T55n	DIFFOUT_T109n	F19	Yes			
8A	VREFB8AN0	IO				DIFFOUT_T110p	J18	Yes			
8A	VREFB8AN0	IO				DIFFOUT_T110n	J19	Yes			
8A	VREFB8AN0	IO			DIFFIO_RX_T56p	DIFFOUT_T111p	B20	Yes	DQ33T	DQ36T	
8A	VREFB8AN0	IO			DIFFIO_RX_T56n	DIFFOUT_T111n	A21	Yes	DQ33T	DQ36T	
8A	VREFB8AN0	IO				DIFFOUT_T112p	A20	Yes	DQ33T	DQ36T	
8A	VREFB8AN0	IO				DIFFOUT_T112n	D19	Yes	DQ33T	DQ36T	
8A	VREFB8AN0	IO			DIFFIO_RX_T57p	DIFFOUT_T113p	D20	Yes	DQS33T	DQS36T/CQ36T	
8A	VREFB8AN0	IO			DIFFIO_RX_T57n	DIFFOUT_T113n	C20	Yes	DQSn33T	DQSn36T/DQ36T	
8A	VREFB8AN0	IO				DIFFOUT_T114p	D21	Yes	DQ34T	DQ36T	
8A	VREFB8AN0	IO				DIFFOUT_T114n	C21	Yes	DQ34T	DQ36T	
8A	VREFB8AN0	IO			DIFFIO_RX_T58p	DIFFOUT_T115p	B22	Yes	DQS34T	DQ36T/CQn36T	
8A	VREFB8AN0	IO			DIFFIO_RX_T58n	DIFFOUT_T115n	A22	Yes	DQSn34T	DQ36T	

Bank Number	VREF	Pin Name/ Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	Dynamic OCT Support	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780
8A	VREFB8AN0	IO				DIFFOUT_T116p	A23	Yes	DQ34T	DQ36T	
8A	VREFB8AN0	IO				DIFFOUT_T116n	B23	Yes	DQ34T	DQ36T	
8A	VREFB8AN0	IO			DIFFIO_RX_T59p	DIFFOUT_T117p	B25	Yes	DQ35T	DQ37T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T59n	DIFFOUT_T117n	A26	Yes	DQ35T	DQ37T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T118p	A24	Yes	DQ35T	DQ37T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T118n	A25	Yes	DQ35T	DQ37T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T60p	DIFFOUT_T119p	B26	Yes	DQS35T	DQS37T/CQ37T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T60n	DIFFOUT_T119n	A27	Yes	DQSn35T	DQSn37T/DQ37T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T120p	F20	Yes	DQ36T	DQ37T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T120n	E20	Yes	DQ36T	DQ37T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T61p	DIFFOUT_T121p	H20	Yes	DQS36T	DQ37T/CQn37T	DQS38T/CQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T61n	DIFFOUT_T121n	G20	Yes	DQSn36T	DQ37T	DQSn38T/DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T122p	H19	Yes	DQ36T	DQ37T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T122n	J20	Yes	DQ36T	DQ37T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T62p	DIFFOUT_T123p	D23	Yes	DQ37T	DQ38T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T62n	DIFFOUT_T123n	C23	Yes	DQ37T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T124p	D22	Yes	DQ37T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T124n	D25	Yes	DQ37T	DQ38T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T63p	DIFFOUT_T125p	D24	Yes	DQS37T	DQS38T/CQ38T	DQ38T/CQn38T
8A	VREFB8AN0	IO			DIFFIO_RX_T63n	DIFFOUT_T125n	C24	Yes	DQSn37T	DQSn38T/DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T126p	F21	Yes	DQ38T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T126n	G21	Yes	DQ38T	DQ38T	DQ38T
8A	VREFB8AN0	IO	RUP8A		DIFFIO_RX_T64p	DIFFOUT_T127p	F22	Yes	DQS38T	DQ38T/CQn38T	DQ38T
8A	VREFB8AN0	IO	RDN8A		DIFFIO_RX_T64n	DIFFOUT_T127n	E22	Yes	DQSn38T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T128p	E23	Yes	DQ38T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T128n	G22	Yes	DQ38T	DQ38T	DQ38T
		GND					AF3	No			
		GND					R14	No			
		GND					K11	No			
		GND					B27	No			
		GND					AG2	No			
		GND					AG5	No			
		GND					AG8	No			
		GND					AG11	No			
		GND					AG14	No			
		GND					AG17	No			
		GND					AG20	No			
		GND					AG23	No			
		GND					AG26	No			
		GND					AF27	No			
		GND					AD2	No			
		GND					AD5	No			
		GND					AD8	No			
		GND					AD11	No			
		GND					AD14	No			
		GND					AD17	No			
		GND					AD20	No			
		GND					AD23	No			
		GND					AC24	No			
		GND					AC27	No			
		GND					AA2	No			
		GND					AA5	No			
		GND					AA8	No			
		GND					AA11	No			
		GND					AA14	No			
		GND					AA17	No			
		GND					AA20	No			
		GND					Y12	No			
		GND					Y16	No			
		GND					Y21	No			

Bank Number	VREF	Pin Name/ Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	Dynamic OCT Support	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780
		GND					Y24	No			
		GND					Y27	No			
		GND					W12	No			
		GND					W14	No			
		GND					W16	No			
		GND					W18	No			
		GND					V2	No			
		GND					V5	No			
		GND					V8	No			
		GND					V11	No			
		GND					V13	No			
		GND					V15	No			
		GND					V17	No			
		GND					V19	No			
		GND					U10	No			
		GND					U12	No			
		GND					U14	No			
		GND					U16	No			
		GND					U18	No			
		GND					U21	No			
		GND					U24	No			
		GND					U27	No			
		GND					T11	No			
		GND					T13	No			
		GND					T15	No			
		GND					T17	No			
		GND					T19	No			
		GND					R2	No			
		GND					R5	No			
		GND					R8	No			
		GND					R12	No			
		GND					R16	No			
		GND					R18	No			
		GND					P11	No			
		GND					P13	No			
		GND					P17	No			
		GND					P21	No			
		GND					P24	No			
		GND					P27	No			
		GND					N10	No			
		GND					N12	No			
		GND					N14	No			
		GND					N16	No			
		GND					N18	No			
		GND					M2	No			
		GND					M5	No			
		GND					M8	No			
		GND					M11	No			
		GND					M13	No			
		GND					M15	No			
		GND					M17	No			
		GND					M19	No			
		GND					L10	No			
		GND					L12	No			
		GND					L14	No			
		GND					L16	No			
		GND					L18	No			
		GND					L21	No			
		GND					L24	No			
		GND					L27	No			

Bank Number	VREF	Pin Name/ Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	Dynamic OCT Support	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780
		GND					K13	No			
		GND					K15	No			
		GND					K17	No			
		GND					K19	No			
		GND					J2	No			
		GND					J5	No			
		GND					J8	No			
		GND					J13	No			
		GND					J17	No			
		GND					H9	No			
		GND					H12	No			
		GND					H15	No			
		GND					H18	No			
		GND					H21	No			
		GND					H24	No			
		GND					H27	No			
		GND					F2	No			
		GND					F5	No			
		GND					E6	No			
		GND					E9	No			
		GND					E12	No			
		GND					E15	No			
		GND					E18	No			
		GND					E21	No			
		GND					E24	No			
		GND					E27	No			
		GND					C2	No			
		GND					B3	No			
		GND					B6	No			
		GND					B9	No			
		GND					B12	No			
		GND					B15	No			
		GND					B18	No			
		GND					B21	No			
		GND					B24	No			
		VCC					R15	No			
		VCC					L17	No			
		VCC					V14	No			
		VCC					V18	No			
		VCC					U11	No			
		VCC					U13	No			
		VCC					U15	No			
		VCC					U17	No			
		VCC					T12	No			
		VCC					T14	No			
		VCC					T16	No			
		VCC					R13	No			
		VCC					R17	No			
		VCC					P12	No			
		VCC					P14	No			
		VCC					P16	No			
		VCC					P18	No			
		VCC					N13	No			
		VCC					N15	No			
		VCC					N17	No			
		VCC					M12	No			
		VCC					M14	No			
		VCC					M16	No			
		VCC					L11	No			
		VCC					V12	No			

Bank Number	VREF	Pin Name/ Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	Dynamic OCT Support	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780
		VCC					V16	No			
		VCC					T18	No			
		VCC					R11	No			
		VCC					N11	No			
		VCC					M18	No			
		VCC					L13	No			
		VCC					L15	No			
		VCCPT					R24	No			
		VCCPT					U20	No			
		VCCPT					AD15	No			
		VCCPT					P5	No			
		VCCPT					M9	No			
		VCCPT					E14	No			
		DNU					P15	No			
		VCCPGM					AA21	No			
		VCCPGM					Y8	No			
		TEMPDIODEn					D4	No			
		TEMPDIODEp					D3	No			
		VCC_CLKIN3C					AB14	No			
		VCC_CLKIN4C					AC13	No			
		VCC_CLKIN7C					F14	No			
		VCC_CLKIN8C					F16	No			
		VCCBAT					F6	No			
		VCCA_PLL_B1					AC14	No			
		VCCA_PLL_L2					R22	No			
		VCCA_PLL_R2					R7	No			
		VCCA_PLL_T1					F15	No			
		VCCD_PLL_B1					AB15	No			
		VCCD_PLL_L2					P22	No			
		VCCD_PLL_R2					P7	No			
		VCCD_PLL_T1					G15	No			
		VCCIO1A					E26	No			
		VCCIO1A					H23	No			
		VCCIO1A					H26	No			
		VCCIO1C					R23	No			
		VCCIO1C					P26	No			
		VCCIO2A					W26	No			
		VCCIO2A					AD26	No			
		VCCIO2A					AA22	No			
		VCCIO2C					T26	No			
		VCCIO2C					V22	No			
		VCCIO3A					AC22	No			
		VCCIO3A					AF22	No			
		VCCIO3A					AF25	No			
		VCCIO3A					AC18	No			
		VCCIO3C					AC15	No			
		VCCIO3C					AF18	No			
		VCCIO4A					AC6	No			
		VCCIO4A					AF4	No			
		VCCIO4A					AF7	No			
		VCCIO4A					AD10	No			
		VCCIO4C					AB12	No			
		VCCIO4C					AF13	No			
		VCCIO5A					AA7	No			
		VCCIO5A					AD3	No			
		VCCIO5A					AA3	No			
		VCCIO5C					P6	No			
		VCCIO5C					R3	No			
		VCCIO6A					E3	No			
		VCCIO6A					K3	No			

Bank Number	VREF	Pin Name/ Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F780	Dynamic OCT Support	DQS for X4 for F780	DQS for X8/X9 for F780	DQS for X16/X18 for F780
		VCCIO6A					H7	No			
		VCCIO6C					L7	No			
		VCCIO6C					N3	No			
		VCCIO7A					C7	No			
		VCCIO7A					F7	No			
		VCCIO7A					F11	No			
		VCCIO7A					C4	No			
		VCCIO7C					C11	No			
		VCCIO7C					G14	No			
		VCCIO8A					C25	No			
		VCCIO8A					F23	No			
		VCCIO8A					E19	No			
		VCCIO8A					C22	No			
		VCCIO8C					C16	No			
		VCCIO8C					G17	No			
		VCCPD1A					L19	No			
		VCCPD1C					N19	No			
		VCCPD2A					U19	No			
		VCCPD2C					R19	No			
		VCCPD3A					W17	No			
		VCCPD3C					W15	No			
		VCCPD4A					W11	No			
		VCCPD4C					W13	No			
		VCCPD5A					V10	No			
		VCCPD5C					T10	No			
		VCCPD6A					M10	No			
		VCCPD6C					P10	No			
		VCCPD7A					K12	No			
		VCCPD7C					K14	No			
		VCCPD8A					K18	No			
		VCCPD8C					K16	No			
1A	VREFB1AN0	VREFB1AN0	VREFB1AN0				K22	No			
1C	VREFB1CN0	VREFB1CN0	VREFB1CN0				N22	No			
2A	VREFB2AN0	VREFB2AN0	VREFB2AN0				Y22	No			
2C	VREFB2CN0	VREFB2CN0	VREFB2CN0				U22	No			
3A	VREFB3AN0	VREFB3AN0	VREFB3AN0				AB18	No			
3C	VREFB3CN0	VREFB3CN0	VREFB3CN0				AA16	No			
4A	VREFB4AN0	VREFB4AN0	VREFB4AN0				AB10	No			
4C	VREFB4CN0	VREFB4CN0	VREFB4CN0				AA12	No			
5A	VREFB5AN0	VREFB5AN0	VREFB5AN0				W7	No			
5C	VREFB5CN0	VREFB5CN0	VREFB5CN0				T7	No			
6A	VREFB6AN0	VREFB6AN0	VREFB6AN0				J7	No			
6C	VREFB6CN0	VREFB6CN0	VREFB6CN0				M7	No			
7A	VREFB7AN0	VREFB7AN0	VREFB7AN0				G11	No			
7C	VREFB7CN0	VREFB7CN0	VREFB7CN0				H13	No			
8A	VREFB8AN0	VREFB8AN0	VREFB8AN0				G19	No			
8C	VREFB8CN0	VREFB8CN0	VREFB8CN0				H17	No			
		NC					E25	No			
		NC					AB22	No			
		NC					W10	No			
		NC					E4	No			
		NC					AE25	No			
		NC					V9	No			
		NC					L20	No			
		NC					K10	No			
		NC					J21	No			
		VCCAUX					G23	No			
		VCCAUX					AC23	No			
		VCCAUX					AB6	No			
		VCCAUX					G6	No			

Bank Number	VREF	Pin Name/ Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
1A		TDI		TDI			G28	No			
1A		TMS		TMS			H28	No			
1A		TRST		TRST			J28	No			
1A		TCK		TCK			F30	No			
1A		TDO		TDO			G29	No			
1A	VREFB1AN0	IO	PLL_L1_CLKOUT0n		DIFFIO_TX_L1n	DIFFOUT_L1n	G31	Yes			
1A	VREFB1AN0	IO	PLL_L1_FB_CLKOUT0p		DIFFIO_TX_L1p	DIFFOUT_L1p	G30	Yes			
1A	VREFB1AN0	IO	RDN1A		DIFFIO_RX_L1n	DIFFOUT_L2n	E32	Yes			
1A	VREFB1AN0	IO	RUP1A		DIFFIO_RX_L1p	DIFFOUT_L2p	E31	Yes			
1A	VREFB1AN0	IO			DIFFIO_TX_L2n	DIFFOUT_L3n	J30	Yes	DQ1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L2p	DIFFOUT_L3p	J29	Yes	DQ1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L2n	DIFFOUT_L4n	F32	Yes	DQSn1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L2p	DIFFOUT_L4p	F31	Yes	DQS1L	DQ1L/CQn1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L3n	DIFFOUT_L5n	K28	Yes	DQ1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L3p	DIFFOUT_L5p	K27	Yes	DQ1L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L3n	DIFFOUT_L6n	C34	Yes	DQSn2L	DQSn1L/DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L3p	DIFFOUT_L6p	C33	Yes	DQS2L	DQS1L/CQ1L	DQ1L/CQn1L
1A	VREFB1AN0	IO			DIFFIO_TX_L4n	DIFFOUT_L7n	N25	Yes	DQ2L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L4p	DIFFOUT_L7p	M24	Yes	DQ2L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L4n	DIFFOUT_L8n	H32	Yes	DQ2L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L4p	DIFFOUT_L8p	H31	Yes	DQ2L	DQ1L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L5n	DIFFOUT_L9n	M27	Yes	DQ3L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L5p	DIFFOUT_L9p	M26	Yes	DQ3L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L5n	DIFFOUT_L10n	D34	Yes	DQSn3L	DQ2L	DQSn1L/DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L5p	DIFFOUT_L10p	D33	Yes	DQS3L	DQ2L/CQn2L	DQS1L/CQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L6n	DIFFOUT_L11n	K30	Yes	DQ3L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L6p	DIFFOUT_L11p	K29	Yes	DQ3L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L6n	DIFFOUT_L12n	J32	Yes	DQSn4L	DQSn2L/DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L6p	DIFFOUT_L12p	J31	Yes	DQS4L	DQS2L/CQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L7n	DIFFOUT_L13n	L29	Yes	DQ4L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L7p	DIFFOUT_L13p	L28	Yes	DQ4L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L7n	DIFFOUT_L14n	E34	Yes	DQ4L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_RX_L7p	DIFFOUT_L14p	F33	Yes	DQ4L	DQ2L	DQ1L
1A	VREFB1AN0	IO			DIFFIO_TX_L8n	DIFFOUT_L15n	M28	Yes	DQ5L	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_TX_L8p	DIFFOUT_L15p	N27	Yes	DQ5L	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_RX_L8n	DIFFOUT_L16n	F34	Yes	DQSn5L	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_RX_L8p	DIFFOUT_L16p	G33	Yes	DQS5L	DQ3L/CQn3L	
1A	VREFB1AN0	IO			DIFFIO_TX_L9n	DIFFOUT_L17n	N26	Yes	DQ5L	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_TX_L9p	DIFFOUT_L17p	P25	Yes	DQ5L	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_RX_L9n	DIFFOUT_L18n	K32	Yes	DQSn6L	DQSn3L/DQ3L	
1A	VREFB1AN0	IO			DIFFIO_RX_L9p	DIFFOUT_L18p	K31	Yes	DQS6L	DQS3L/CQ3L	
1A	VREFB1AN0	IO			DIFFIO_TX_L10n	DIFFOUT_L19n	L32	Yes	DQ6L	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_TX_L10p	DIFFOUT_L19p	L31	Yes	DQ6L	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_RX_L10n	DIFFOUT_L20n	G34	Yes	DQ6L	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_RX_L10p	DIFFOUT_L20p	H34	Yes	DQ6L	DQ3L	
1A	VREFB1AN0	IO			DIFFIO_TX_L11n	DIFFOUT_L21n	N24	Yes	DQ7L		
1A	VREFB1AN0	IO			DIFFIO_TX_L11p	DIFFOUT_L21p	P23	Yes	DQ7L		
1A	VREFB1AN0	IO			DIFFIO_RX_L11n	DIFFOUT_L22n	J34	Yes	DQSn7L		
1A	VREFB1AN0	IO			DIFFIO_RX_L11p	DIFFOUT_L22p	J33	Yes	DQS7L		
1A	VREFB1AN0	IO			DIFFIO_TX_L12n	DIFFOUT_L23n	M30	Yes	DQ7L		
1A	VREFB1AN0	IO			DIFFIO_TX_L12p	DIFFOUT_L23p	M29	Yes	DQ7L		
1A	VREFB1AN0	IO			DIFFIO_RX_L12n	DIFFOUT_L24n	K34	Yes			
1A	VREFB1AN0	IO			DIFFIO_RX_L12p	DIFFOUT_L24p	K33	Yes			
1C	VREFB1CN0	IO			DIFFIO_TX_L13n	DIFFOUT_L25n	N30	Yes	DQ8L	DQ8L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_TX_L13p	DIFFOUT_L25p	N29	Yes	DQ8L	DQ8L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_RX_L13n	DIFFOUT_L26n	N32	Yes	DQSn8L	DQ8L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_RX_L13p	DIFFOUT_L26p	M31	Yes	DQS8L	DQ8L/CQn8L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_TX_L14n	DIFFOUT_L27n	P29	Yes	DQ8L	DQ8L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_TX_L14p	DIFFOUT_L27p	P28	Yes	DQ8L	DQ8L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_RX_L14n	DIFFOUT_L28n	L34	Yes	DQSn9L	DQSn8L/DQ8L	DQ8L

Bank Number	VREF	Pin Name/ Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
1C	VREFB1CN0	IO			DIFFIO_RX_L14p	DIFFOUT_L28p	M33	Yes	DQS9L	DQS8L/CQ8L	DQ8L/CQn8L
1C	VREFB1CN0	IO			DIFFIO_TX_L15n	DIFFOUT_L29n	R26	Yes	DQ9L	DQ8L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_TX_L15p	DIFFOUT_L29p	R25	Yes	DQ9L	DQ8L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_RX_L15n	DIFFOUT_L30n	P32	Yes	DQ9L	DQ8L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_RX_L15p	DIFFOUT_L30p	N31	Yes	DQ9L	DQ8L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_TX_L16n	DIFFOUT_L31n	R24	Yes	DQ10L	DQ9L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_TX_L16p	DIFFOUT_L31p	T23	Yes	DQ10L	DQ9L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_RX_L16n	DIFFOUT_L32n	M34	Yes	DQSn10L	DQ9L	DQSn8L/DQ8L
1C	VREFB1CN0	IO			DIFFIO_RX_L16p	DIFFOUT_L32p	N33	Yes	DQS10L	DQ9L/CQn9L	DQS8L/CQ8L
1C	VREFB1CN0	IO			DIFFIO_TX_L17n	DIFFOUT_L33n	R28	Yes	DQ10L	DQ9L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_TX_L17p	DIFFOUT_L33p	R27	Yes	DQ10L	DQ9L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_RX_L17n	DIFFOUT_L34n	R32	Yes	DQSn11L	DQSn9L/DQ9L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_RX_L17p	DIFFOUT_L34p	P31	Yes	DQS11L	DQS9L/CQ9L	DQ8L
1C	VREFB1CN0	IO		CLKUSR	DIFFIO_TX_L18n	DIFFOUT_L35n	R30	Yes	DQ11L	DQ9L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_TX_L18p	DIFFOUT_L35p	R29	Yes	DQ11L	DQ9L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_RX_L18n	DIFFOUT_L36n	N34	Yes	DQ11L	DQ9L	DQ8L
1C	VREFB1CN0	IO			DIFFIO_RX_L18p	DIFFOUT_L36p	P34	Yes	DQ11L	DQ9L	DQ8L
1C	VREFB1CN0	IO		DATA0	DIFFIO_TX_L19n	DIFFOUT_L37n	T28	Yes	DQ12L	DQ10L	
1C	VREFB1CN0	IO		DATA1	DIFFIO_TX_L19p	DIFFOUT_L37p	T27	Yes	DQ12L	DQ10L	
1C	VREFB1CN0	IO		DATA2	DIFFIO_RX_L19n	DIFFOUT_L38n	R34	Yes	DQSn12L	DQ10L	
1C	VREFB1CN0	IO		DATA3	DIFFIO_RX_L19p	DIFFOUT_L38p	R33	Yes	DQS12L	DQ10L/CQn10L	
1C	VREFB1CN0	IO		DATA4	DIFFIO_TX_L20n	DIFFOUT_L39n	T25	Yes	DQ12L	DQ10L	
1C	VREFB1CN0	IO		DATA5	DIFFIO_TX_L20p	DIFFOUT_L39p	T24	Yes	DQ12L	DQ10L	
1C	VREFB1CN0	IO		DATA6	DIFFIO_RX_L20n	DIFFOUT_L40n	T32	Yes	DQSn13L	DQSn10L/DQ10L	
1C	VREFB1CN0	IO		DATA7	DIFFIO_RX_L20p	DIFFOUT_L40p	R31	Yes	DQS13L	DQS10L/CQ10L	
1C	VREFB1CN0	IO		INIT_DONE	DIFFIO_TX_L21n	DIFFOUT_L41n	T26	Yes	DQ13L	DQ10L	
1C	VREFB1CN0	IO		CRC_ERROR	DIFFIO_TX_L21p	DIFFOUT_L41p	U25	Yes	DQ13L	DQ10L	
1C	VREFB1CN0	IO		DEV_OE	DIFFIO_RX_L21n	DIFFOUT_L42n	U32	Yes	DQ13L	DQ10L	
1C	VREFB1CN0	IO		DEV_CLRn	DIFFIO_RX_L21p	DIFFOUT_L42p	U31	Yes	DQ13L	DQ10L	
1C	VREFB1CN0	IO	PLL_L2_CLKOUT0n		DIFFIO_TX_L22n	DIFFOUT_L43n	T30	No			
1C	VREFB1CN0	IO	PLL_L2_FB_CLKOUT0p		DIFFIO_TX_L22p	DIFFOUT_L43p	T29	No			
1C	VREFB1CN0	IO	CLK0n		DIFFIO_RX_L22n	DIFFOUT_L44n	V32	No			
1C	VREFB1CN0	IO	CLK0p		DIFFIO_RX_L22p	DIFFOUT_L44p	V31	No			
1C	VREFB1CN0	CLK1n	CLK1n				T34	No			
1C	VREFB1CN0	CLK1p	CLK1p				T33	No			
2C	VREFB2CN0	CLK3p	CLK3p				V33	No			
2C	VREFB2CN0	CLK3n	CLK3n				V34	No			
2C	VREFB2CN0	IO	CLK2p		DIFFIO_RX_L23p	DIFFOUT_L45p	W33	No			
2C	VREFB2CN0	IO	CLK2n		DIFFIO_RX_L23n	DIFFOUT_L45n	W34	No			
2C	VREFB2CN0	IO	PLL_L3_FB_CLKOUT0p		DIFFIO_TX_L23p	DIFFOUT_L46p	W28	No			
2C	VREFB2CN0	IO	PLL_L3_CLKOUT0n		DIFFIO_TX_L23n	DIFFOUT_L46n	V29	No			
2C	VREFB2CN0	IO			DIFFIO_RX_L24p	DIFFOUT_L47p	AA33	Yes	DQ14L	DQ17L	
2C	VREFB2CN0	IO			DIFFIO_RX_L24n	DIFFOUT_L47n	Y34	Yes	DQ14L	DQ17L	
2C	VREFB2CN0	IO			DIFFIO_TX_L24p	DIFFOUT_L48p	W26	Yes	DQ14L	DQ17L	
2C	VREFB2CN0	IO			DIFFIO_TX_L24n	DIFFOUT_L48n	W27	Yes	DQ14L	DQ17L	
2C	VREFB2CN0	IO			DIFFIO_RX_L25p	DIFFOUT_L49p	Y31	Yes	DQS14L	DQS17L/CQ17L	
2C	VREFB2CN0	IO			DIFFIO_RX_L25n	DIFFOUT_L49n	Y32	Yes	DQSn14L	DQSn17L/DQ17L	
2C	VREFB2CN0	IO			DIFFIO_TX_L25p	DIFFOUT_L50p	V24	Yes	DQ15L	DQ17L	
2C	VREFB2CN0	IO			DIFFIO_TX_L25n	DIFFOUT_L50n	V25	Yes	DQ15L	DQ17L	
2C	VREFB2CN0	IO			DIFFIO_RX_L26p	DIFFOUT_L51p	AB33	Yes	DQS15L	DQ17L/CQn17L	
2C	VREFB2CN0	IO			DIFFIO_RX_L26n	DIFFOUT_L51n	AA34	Yes	DQSn15L	DQ17L	
2C	VREFB2CN0	IO			DIFFIO_TX_L26p	DIFFOUT_L52p	W30	Yes	DQ15L	DQ17L	
2C	VREFB2CN0	IO			DIFFIO_TX_L26n	DIFFOUT_L52n	W31	Yes	DQ15L	DQ17L	
2C	VREFB2CN0	IO			DIFFIO_RX_L27p	DIFFOUT_L53p	AA31	Yes	DQ16L	DQ18L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_RX_L27n	DIFFOUT_L53n	AA32	Yes	DQ16L	DQ18L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_TX_L27p	DIFFOUT_L54p	Y28	Yes	DQ16L	DQ18L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_TX_L27n	DIFFOUT_L54n	Y29	Yes	DQ16L	DQ18L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_RX_L28p	DIFFOUT_L55p	AC34	Yes	DQS16L	DQS18L/CQ18L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_RX_L28n	DIFFOUT_L55n	AB34	Yes	DQSn16L	DQSn18L/DQ18L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_TX_L28p	DIFFOUT_L56p	Y23	Yes	DQ17L	DQ18L	DQ19L

Bank Number	VREF	Pin Name/ Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
2C	VREFB2CN0	IO			DIFFIO_TX_L28n	DIFFOUT_L56n	W24	Yes	DQ17L	DQ18L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_RX_L29p	DIFFOUT_L57p	AB31	Yes	DQS17L	DQ18L/CQn18L	DQS19L/CQ19L
2C	VREFB2CN0	IO			DIFFIO_RX_L29n	DIFFOUT_L57n	AB32	Yes	DQSn17L	DQ18L	DQSn19L/DQ19L
2C	VREFB2CN0	IO			DIFFIO_TX_L29p	DIFFOUT_L58p	AA29	Yes	DQ17L	DQ18L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_TX_L29n	DIFFOUT_L58n	AA30	Yes	DQ17L	DQ18L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_RX_L30p	DIFFOUT_L59p	AD33	Yes	DQ18L	DQ19L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_RX_L30n	DIFFOUT_L59n	AD34	Yes	DQ18L	DQ19L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_TX_L30p	DIFFOUT_L60p	Y25	Yes	DQ18L	DQ19L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_TX_L30n	DIFFOUT_L60n	Y26	Yes	DQ18L	DQ19L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_RX_L31p	DIFFOUT_L61p	AC31	Yes	DQS18L	DQS19L/CQ19L	DQ19L/CQn19L
2C	VREFB2CN0	IO			DIFFIO_RX_L31n	DIFFOUT_L61n	AC32	Yes	DQSn18L	DQSn19L/DQ19L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_TX_L31p	DIFFOUT_L62p	AA27	Yes	DQ19L	DQ19L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_TX_L31n	DIFFOUT_L62n	AA28	Yes	DQ19L	DQ19L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_RX_L32p	DIFFOUT_L63p	AE33	Yes	DQS19L	DQ19L/CQn19L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_RX_L32n	DIFFOUT_L63n	AE34	Yes	DQSn19L	DQ19L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_TX_L32p	DIFFOUT_L64p	AB29	Yes	DQ19L	DQ19L	DQ19L
2C	VREFB2CN0	IO			DIFFIO_TX_L32n	DIFFOUT_L64n	AB30	Yes	DQ19L	DQ19L	DQ19L
2A	VREFB2AN0	IO			DIFFIO_RX_L33p	DIFFOUT_L65p	AG33	Yes			
2A	VREFB2AN0	IO			DIFFIO_RX_L33n	DIFFOUT_L65n	AF34	Yes			
2A	VREFB2AN0	IO			DIFFIO_TX_L33p	DIFFOUT_L66p	AA24	Yes	DQ20L		
2A	VREFB2AN0	IO			DIFFIO_TX_L33n	DIFFOUT_L66n	AA25	Yes	DQ20L		
2A	VREFB2AN0	IO			DIFFIO_RX_L34p	DIFFOUT_L67p	AE31	Yes	DQS20L		
2A	VREFB2AN0	IO			DIFFIO_RX_L34n	DIFFOUT_L67n	AE32	Yes	DQSn20L		
2A	VREFB2AN0	IO			DIFFIO_TX_L34p	DIFFOUT_L68p	AC28	Yes	DQ20L		
2A	VREFB2AN0	IO			DIFFIO_TX_L34n	DIFFOUT_L68n	AC29	Yes	DQ20L		
2A	VREFB2AN0	IO			DIFFIO_RX_L35p	DIFFOUT_L69p	AH33	Yes	DQ21L	DQ24L	
2A	VREFB2AN0	IO			DIFFIO_RX_L35n	DIFFOUT_L69n	AG34	Yes	DQ21L	DQ24L	
2A	VREFB2AN0	IO			DIFFIO_TX_L35p	DIFFOUT_L70p	AD30	Yes	DQ21L	DQ24L	
2A	VREFB2AN0	IO			DIFFIO_TX_L35n	DIFFOUT_L70n	AD31	Yes	DQ21L	DQ24L	
2A	VREFB2AN0	IO			DIFFIO_RX_L36p	DIFFOUT_L71p	AF31	Yes	DQS21L	DQS24L/CQ24L	
2A	VREFB2AN0	IO			DIFFIO_RX_L36n	DIFFOUT_L71n	AF32	Yes	DQSn21L	DQSn24L/DQ24L	
2A	VREFB2AN0	IO			DIFFIO_TX_L36p	DIFFOUT_L72p	AB24	Yes	DQ22L	DQ24L	
2A	VREFB2AN0	IO			DIFFIO_TX_L36n	DIFFOUT_L72n	AB25	Yes	DQ22L	DQ24L	
2A	VREFB2AN0	IO			DIFFIO_RX_L37p	DIFFOUT_L73p	AJ34	Yes	DQS22L	DQ24L/CQn24L	
2A	VREFB2AN0	IO			DIFFIO_RX_L37n	DIFFOUT_L73n	AH34	Yes	DQSn22L	DQ24L	
2A	VREFB2AN0	IO			DIFFIO_TX_L37p	DIFFOUT_L74p	AB26	Yes	DQ22L	DQ24L	
2A	VREFB2AN0	IO			DIFFIO_TX_L37n	DIFFOUT_L74n	AB27	Yes	DQ22L	DQ24L	
2A	VREFB2AN0	IO			DIFFIO_RX_L38p	DIFFOUT_L75p	AG31	Yes	DQ23L	DQ25L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_RX_L38n	DIFFOUT_L75n	AG32	Yes	DQ23L	DQ25L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L38p	DIFFOUT_L76p	AE29	Yes	DQ23L	DQ25L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L38n	DIFFOUT_L76n	AE30	Yes	DQ23L	DQ25L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_RX_L39p	DIFFOUT_L77p	AK33	Yes	DQS23L	DQS25L/CQ25L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_RX_L39n	DIFFOUT_L77n	AK34	Yes	DQSn23L	DQSn25L/DQ25L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L39p	DIFFOUT_L78p	AD28	Yes	DQ24L	DQ25L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L39n	DIFFOUT_L78n	AD29	Yes	DQ24L	DQ25L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_RX_L40p	DIFFOUT_L79p	AJ31	Yes	DQS24L	DQ25L/CQn25L	DQS26L/CQ26L
2A	VREFB2AN0	IO			DIFFIO_RX_L40n	DIFFOUT_L79n	AJ32	Yes	DQSn24L	DQ25L	DQSn26L/DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L40p	DIFFOUT_L80p	AF28	Yes	DQ24L	DQ25L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L40n	DIFFOUT_L80n	AF29	Yes	DQ24L	DQ25L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_RX_L41p	DIFFOUT_L81p	AM34	Yes	DQ25L	DQ26L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_RX_L41n	DIFFOUT_L81n	AL34	Yes	DQ25L	DQ26L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L41p	DIFFOUT_L82p	AE27	Yes	DQ25L	DQ26L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L41n	DIFFOUT_L82n	AE28	Yes	DQ25L	DQ26L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_RX_L42p	DIFFOUT_L83p	AH30	Yes	DQS25L	DQS26L/CQ26L	DQ26L/CQn26L
2A	VREFB2AN0	IO			DIFFIO_RX_L42n	DIFFOUT_L83n	AH31	Yes	DQSn25L	DQSn26L/DQ26L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L42p	DIFFOUT_L84p	AD26	Yes	DQ26L	DQ26L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L42n	DIFFOUT_L84n	AD27	Yes	DQ26L	DQ26L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_RX_L43p	DIFFOUT_L85p	AL32	Yes	DQS26L	DQ26L/CQn26L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_RX_L43n	DIFFOUT_L85n	AL33	Yes	DQSn26L	DQ26L	DQ26L
2A	VREFB2AN0	IO			DIFFIO_TX_L43p	DIFFOUT_L86p	AC25	Yes	DQ26L	DQ26L	DQ26L

Bank Number	VREF	Pin Name/ Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
2A	VREFB2AN0	IO			DIFFIO_TX_L43n	DIFFOUT_L86n	AC26	Yes	DQ26L	DQ26L	DQ26L
2A	VREFB2AN0	IO	RUP2A		DIFFIO_RX_L44p	DIFFOUT_L87p	AK31	Yes			
2A	VREFB2AN0	IO	RDN2A		DIFFIO_RX_L44n	DIFFOUT_L87n	AK32	Yes			
2A	VREFB2AN0	IO	PLL_L4_FB_CLKOUT0p		DIFFIO_TX_L44p	DIFFOUT_L88p	AG29	Yes			
2A	VREFB2AN0	IO	PLL_L4_CLKOUT0n		DIFFIO_TX_L44n	DIFFOUT_L88n	AG30	Yes			
		nCONFIG		nCONFIG			AE25	No			
		nSTATUS		nSTATUS			AH28	No			
		CONF_DONE		CONF_DONE			AH29	No			
		PORSEL					AF26	No			
		nCE		nCE			AE26	No			
3A	VREFB3AN0	IO				DIFFOUT_B1n	AH27	Yes	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B1p	AJ27	Yes	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO	RDN3A		DIFFIO_RX_B1n	DIFFOUT_B2n	AK28	Yes	DQSn1B	DQ1B	DQ1B
3A	VREFB3AN0	IO	RUP3A		DIFFIO_RX_B1p	DIFFOUT_B2p	AJ28	Yes	DQS1B	DQ1B/CQn1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B3n	AJ29	Yes	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B3p	AJ26	Yes	DQ1B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B2n	DIFFOUT_B4n	AM32	Yes	DQSn2B	DQSn1B/DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B2p	DIFFOUT_B4p	AM31	Yes	DQS2B	DQS1B/CQ1B	DQ1B/CQn1B
3A	VREFB3AN0	IO				DIFFOUT_B5n	AL29	Yes	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B5p	AM29	Yes	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B3n	DIFFOUT_B6n	AN30	Yes	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B3p	DIFFOUT_B6p	AM30	Yes	DQ2B	DQ1B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B7n	AH26	Yes	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B7p	AF24	Yes	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B4n	DIFFOUT_B8n	AH24	Yes	DQSn3B	DQ2B	DQSn1B/DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B4p	DIFFOUT_B8p	AG24	Yes	DQS3B	DQ2B/CQn2B	DQS1B/CQ1B
3A	VREFB3AN0	IO				DIFFOUT_B9n	AH25	Yes	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B9p	AF23	Yes	DQ3B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B5n	DIFFOUT_B10n	AP33	Yes	DQSn4B	DQSn2B/DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B5p	DIFFOUT_B10p	AN33	Yes	DQS4B	DQS2B/CQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B11n	AP32	Yes	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B11p	AP30	Yes	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B6n	DIFFOUT_B12n	AP31	Yes	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO			DIFFIO_RX_B6p	DIFFOUT_B12p	AN31	Yes	DQ4B	DQ2B	DQ1B
3A	VREFB3AN0	IO				DIFFOUT_B13n	AK27	Yes	DQ5B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B13p	AL28	Yes	DQ5B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B7n	DIFFOUT_B14n	AL27	Yes	DQSn5B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B7p	DIFFOUT_B14p	AL26	Yes	DQS5B	DQ3B/CQn3B	
3A	VREFB3AN0	IO				DIFFOUT_B15n	AK25	Yes	DQ5B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B15p	AM26	Yes	DQ5B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B8n	DIFFOUT_B16n	AP28	Yes	DQSn6B	DQSn3B/DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B8p	DIFFOUT_B16p	AN28	Yes	DQS6B	DQS3B/CQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B17n	AM28	Yes	DQ6B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B17p	AP29	Yes	DQ6B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B9n	DIFFOUT_B18n	AP27	Yes	DQ6B	DQ3B	
3A	VREFB3AN0	IO			DIFFIO_RX_B9p	DIFFOUT_B18p	AN27	Yes	DQ6B	DQ3B	
3A	VREFB3AN0	IO				DIFFOUT_B19n	AE24	Yes			
3A	VREFB3AN0	IO				DIFFOUT_B19p	AE23	Yes			
3A	VREFB3AN0	IO			DIFFIO_RX_B10n	DIFFOUT_B20n	AD22	Yes			
3A	VREFB3AN0	IO			DIFFIO_RX_B10p	DIFFOUT_B20p	AC22	Yes			
3B	VREFB3BN0	IO				DIFFOUT_B25n	AH23	Yes	DQ9B	DQ9B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B25p	AJ24	Yes	DQ9B	DQ9B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B13n	DIFFOUT_B26n	AJ22	Yes	DQSn9B	DQ9B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B13p	DIFFOUT_B26p	AH22	Yes	DQS9B	DQ9B/CQn9B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B27n	AJ23	Yes	DQ9B	DQ9B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B27p	AK22	Yes	DQ9B	DQ9B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B14n	DIFFOUT_B28n	AM24	Yes	DQSn10B	DQSn9B/DQ9B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B14p	DIFFOUT_B28p	AL24	Yes	DQS10B	DQS9B/CQ9B	DQ9B/CQn9B
3B	VREFB3BN0	IO				DIFFOUT_B29n	AK24	Yes	DQ10B	DQ9B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B29p	AL25	Yes	DQ10B	DQ9B	DQ9B

Bank Number	VREF	Pin Name/ Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
3B	VREFB3BN0	IO			DIFFIO_RX_B15n	DIFFOUT_B30n	AM23	Yes	DQ10B	DQ9B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B15p	DIFFOUT_B30p	AL23	Yes	DQ10B	DQ9B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B31n	AE22	Yes	DQ11B	DQ10B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B31p	AE21	Yes	DQ11B	DQ10B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B16n	DIFFOUT_B32n	AG21	Yes	DQSn11B	DQ10B	DQSn9B/DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B16p	DIFFOUT_B32p	AF21	Yes	DQS11B	DQ10B/CQn10B	DQS9B/CQ9B
3B	VREFB3BN0	IO				DIFFOUT_B33n	AD21	Yes	DQ11B	DQ10B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B33p	AE20	Yes	DQ11B	DQ10B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B17n	DIFFOUT_B34n	AP25	Yes	DQSn12B	DQSn10B/DQ10B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B17p	DIFFOUT_B34p	AN25	Yes	DQS12B	DQS10B/CQ10B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B35n	AP26	Yes	DQ12B	DQ10B	DQ9B
3B	VREFB3BN0	IO				DIFFOUT_B35p	AP23	Yes	DQ12B	DQ10B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B18n	DIFFOUT_B36n	AP24	Yes	DQ12B	DQ10B	DQ9B
3B	VREFB3BN0	IO			DIFFIO_RX_B18p	DIFFOUT_B36p	AN24	Yes	DQ12B	DQ10B	DQ9B
3C	VREFB3CN0	IO				DIFFOUT_B49n	AL22	Yes	DQ17B	DQ17B	
3C	VREFB3CN0	IO				DIFFOUT_B49p	AM22	Yes	DQ17B	DQ17B	
3C	VREFB3CN0	IO			DIFFIO_RX_B25n	DIFFOUT_B50n	AL21	Yes	DQSn17B	DQ17B	
3C	VREFB3CN0	IO			DIFFIO_RX_B25p	DIFFOUT_B50p	AK21	Yes	DQS17B	DQ17B/CQn17B	
3C	VREFB3CN0	IO				DIFFOUT_B51n	AJ20	Yes	DQ17B	DQ17B	
3C	VREFB3CN0	IO				DIFFOUT_B51p	AJ21	Yes	DQ17B	DQ17B	
3C	VREFB3CN0	IO			DIFFIO_RX_B26n	DIFFOUT_B52n	AP22	Yes	DQSn18B	DQSn17B/DQ17B	
3C	VREFB3CN0	IO			DIFFIO_RX_B26p	DIFFOUT_B52p	AN22	Yes	DQS18B	DQS17B/CQ17B	
3C	VREFB3CN0	IO				DIFFOUT_B53n	AM21	Yes	DQ18B	DQ17B	
3C	VREFB3CN0	IO				DIFFOUT_B53p	AP20	Yes	DQ18B	DQ17B	
3C	VREFB3CN0	IO			DIFFIO_RX_B27n	DIFFOUT_B54n	AP21	Yes	DQ18B	DQ17B	
3C	VREFB3CN0	IO			DIFFIO_RX_B27p	DIFFOUT_B54p	AN21	Yes	DQ18B	DQ17B	
3C	VREFB3CN0	IO				DIFFOUT_B55n	AL20	Yes	DQ19B		
3C	VREFB3CN0	IO				DIFFOUT_B55p	AM18	Yes	DQ19B		
3C	VREFB3CN0	IO			DIFFIO_RX_B28n	DIFFOUT_B56n	AM19	Yes	DQSn19B		
3C	VREFB3CN0	IO			DIFFIO_RX_B28p	DIFFOUT_B56p	AL19	Yes	DQS19B		
3C	VREFB3CN0	IO				DIFFOUT_B57n	AK18	Yes	DQ19B		
3C	VREFB3CN0	IO				DIFFOUT_B57p	AL18	Yes	DQ19B		
3C	VREFB3CN0	IO			DIFFIO_RX_B29n	DIFFOUT_B58n	AF20	Yes			
3C	VREFB3CN0	IO			DIFFIO_RX_B29p	DIFFOUT_B58p	AF19	Yes			
3C	VREFB3CN0	IO	PLL_B1_CLKOUT4			DIFFOUT_B59n	AE19	No			
3C	VREFB3CN0	IO	PLL_B1_CLKOUT3			DIFFOUT_B59p	AD19	No			
3C	VREFB3CN0	IO			DIFFIO_RX_B30n	DIFFOUT_B60n	AH19	No			
3C	VREFB3CN0	IO			DIFFIO_RX_B30p	DIFFOUT_B60p	AG19	No			
3C	VREFB3CN0	IO	PLL_B1_CLKOUT0n			DIFFOUT_B61n	AE18	No			
3C	VREFB3CN0	IO	PLL_B1_CLKOUT0p			DIFFOUT_B61p	AD18	No			
3C	VREFB3CN0	IO	PLL_B1_FBn/CLKOUT2		DIFFIO_RX_B31n	DIFFOUT_B62n	AK19	No			
3C	VREFB3CN0	IO	PLL_B1_FBp/CLKOUT1		DIFFIO_RX_B31p	DIFFOUT_B62p	AJ19	No			
3C	VREFB3CN0	IO	CLK5n			DIFFOUT_B63n	AP19	No			
3C	VREFB3CN0	IO	CLK5p			DIFFOUT_B63p	AN19	No			
3C	VREFB3CN0	IO	CLK4n		DIFFIO_RX_B32n	DIFFOUT_B64n	AP18	No			
3C	VREFB3CN0	IO	CLK4p		DIFFIO_RX_B32p	DIFFOUT_B64p	AN18	No			
4C	VREFB4CN0	IO	CLK6p		DIFFIO_RX_B33p	DIFFOUT_B65p	AN16	No			
4C	VREFB4CN0	IO	CLK6n		DIFFIO_RX_B33n	DIFFOUT_B65n	AP16	No			
4C	VREFB4CN0	IO	CLK7p			DIFFOUT_B66p	AN15	No			
4C	VREFB4CN0	IO	CLK7n			DIFFOUT_B66n	AP15	No			
4C	VREFB4CN0	IO	PLL_B2_FBp/CLKOUT1		DIFFIO_RX_B34p	DIFFOUT_B67p	AL17	No			
4C	VREFB4CN0	IO	PLL_B2_FBn/CLKOUT2		DIFFIO_RX_B34n	DIFFOUT_B67n	AM17	No			
4C	VREFB4CN0	IO	PLL_B2_CLKOUT0p			DIFFOUT_B68p	AE16	No			
4C	VREFB4CN0	IO	PLL_B2_CLKOUT0n			DIFFOUT_B68n	AF16	No			
4C	VREFB4CN0	IO			DIFFIO_RX_B35p	DIFFOUT_B69p	AL16	No			
4C	VREFB4CN0	IO			DIFFIO_RX_B35n	DIFFOUT_B69n	AM16	No			
4C	VREFB4CN0	IO	PLL_B2_CLKOUT3			DIFFOUT_B70p	AD15	No			
4C	VREFB4CN0	IO	PLL_B2_CLKOUT4			DIFFOUT_B70n	AD16	No			
4C	VREFB4CN0	IO			DIFFIO_RX_B36p	DIFFOUT_B71p	AJ16	Yes			
4C	VREFB4CN0	IO			DIFFIO_RX_B36n	DIFFOUT_B71n	AK16	Yes			

Bank Number	VREF	Pin Name/ Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
4C	VREFB4CN0	IO				DIFFOUT_B72p	AL15	Yes	DQ20B		
4C	VREFB4CN0	IO				DIFFOUT_B72n	AM15	Yes	DQ20B		
4C	VREFB4CN0	IO			DIFFIO_RX_B37p	DIFFOUT_B73p	AL14	Yes	DQS20B		
4C	VREFB4CN0	IO			DIFFIO_RX_B37n	DIFFOUT_B73n	AM14	Yes	DQSn20B		
4C	VREFB4CN0	IO				DIFFOUT_B74p	AK13	Yes	DQ20B		
4C	VREFB4CN0	IO				DIFFOUT_B74n	AL13	Yes	DQ20B		
4C	VREFB4CN0	IO			DIFFIO_RX_B38p	DIFFOUT_B75p	AH15	Yes	DQ21B	DQ22B	
4C	VREFB4CN0	IO			DIFFIO_RX_B38n	DIFFOUT_B75n	AJ15	Yes	DQ21B	DQ22B	
4C	VREFB4CN0	IO				DIFFOUT_B76p	AG15	Yes	DQ21B	DQ22B	
4C	VREFB4CN0	IO				DIFFOUT_B76n	AK15	Yes	DQ21B	DQ22B	
4C	VREFB4CN0	IO			DIFFIO_RX_B39p	DIFFOUT_B77p	AH14	Yes	DQS21B	DQS22B/CQ22B	
4C	VREFB4CN0	IO			DIFFIO_RX_B39n	DIFFOUT_B77n	AJ14	Yes	DQSn21B	DQSn22B/DQ22B	
4C	VREFB4CN0	IO				DIFFOUT_B78p	AP14	Yes	DQ22B	DQ22B	
4C	VREFB4CN0	IO				DIFFOUT_B78n	AN13	Yes	DQ22B	DQ22B	
4C	VREFB4CN0	IO			DIFFIO_RX_B40p	DIFFOUT_B79p	AN12	Yes	DQS22B	DQ22B/CQn22B	
4C	VREFB4CN0	IO			DIFFIO_RX_B40n	DIFFOUT_B79n	AP12	Yes	DQSn22B	DQ22B	
4C	VREFB4CN0	IO				DIFFOUT_B80p	AM12	Yes	DQ22B	DQ22B	
4C	VREFB4CN0	IO				DIFFOUT_B80n	AP13	Yes	DQ22B	DQ22B	
4B	VREFB4BN0	IO			DIFFIO_RX_B47p	DIFFOUT_B93p	AN10	Yes	DQ27B	DQ29B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B47n	DIFFOUT_B93n	AP10	Yes	DQ27B	DQ29B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B94p	AP9	Yes	DQ27B	DQ29B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B94n	AP11	Yes	DQ27B	DQ29B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B48p	DIFFOUT_B95p	AM9	Yes	DQS27B	DQS29B/CQ29B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B48n	DIFFOUT_B95n	AN9	Yes	DQSn27B	DQSn29B/DQ29B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B96p	AE15	Yes	DQ28B	DQ29B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B96n	AF15	Yes	DQ28B	DQ29B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B49p	DIFFOUT_B97p	AF13	Yes	DQS28B	DQ29B/CQn29B	DQS30B/CQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B49n	DIFFOUT_B97n	AF14	Yes	DQSn28B	DQ29B	DQSn30B/DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B98p	AE13	Yes	DQ28B	DQ29B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B98n	AE14	Yes	DQ28B	DQ29B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B50p	DIFFOUT_B99p	AK12	Yes	DQ29B	DQ30B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B50n	DIFFOUT_B99n	AL12	Yes	DQ29B	DQ30B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B100p	AK10	Yes	DQ29B	DQ30B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B100n	AM11	Yes	DQ29B	DQ30B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B51p	DIFFOUT_B101p	AL10	Yes	DQS29B	DQS30B/CQ30B	DQ30B/CQn30B
4B	VREFB4BN0	IO			DIFFIO_RX_B51n	DIFFOUT_B101n	AL11	Yes	DQSn29B	DQSn30B/DQ30B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B102p	AM8	Yes	DQ30B	DQ30B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B102n	AP8	Yes	DQ30B	DQ30B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B52p	DIFFOUT_B103p	AN7	Yes	DQS30B	DQ30B/CQn30B	DQ30B
4B	VREFB4BN0	IO			DIFFIO_RX_B52n	DIFFOUT_B103n	AP7	Yes	DQSn30B	DQ30B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B104p	AP6	Yes	DQ30B	DQ30B	DQ30B
4B	VREFB4BN0	IO				DIFFOUT_B104n	AM7	Yes	DQ30B	DQ30B	DQ30B
4A	VREFB4AN0	IO			DIFFIO_RX_B55p	DIFFOUT_B109p	AC12	Yes			
4A	VREFB4AN0	IO			DIFFIO_RX_B55n	DIFFOUT_B109n	AD12	Yes			
4A	VREFB4AN0	IO				DIFFOUT_B110p	AE12	Yes			
4A	VREFB4AN0	IO				DIFFOUT_B110n	AD13	Yes			
4A	VREFB4AN0	IO			DIFFIO_RX_B56p	DIFFOUT_B111p	AH12	Yes	DQ33B	DQ36B	
4A	VREFB4AN0	IO			DIFFIO_RX_B56n	DIFFOUT_B111n	AJ12	Yes	DQ33B	DQ36B	
4A	VREFB4AN0	IO				DIFFOUT_B112p	AG12	Yes	DQ33B	DQ36B	
4A	VREFB4AN0	IO				DIFFOUT_B112n	AJ13	Yes	DQ33B	DQ36B	
4A	VREFB4AN0	IO			DIFFIO_RX_B57p	DIFFOUT_B113p	AH11	Yes	DQS33B	DQS36B/CQ36B	
4A	VREFB4AN0	IO			DIFFIO_RX_B57n	DIFFOUT_B113n	AJ11	Yes	DQSn33B	DQSn36B/DQ36B	
4A	VREFB4AN0	IO				DIFFOUT_B114p	AJ10	Yes	DQ34B	DQ36B	
4A	VREFB4AN0	IO				DIFFOUT_B114n	AL8	Yes	DQ34B	DQ36B	
4A	VREFB4AN0	IO			DIFFIO_RX_B58p	DIFFOUT_B115p	AK9	Yes	DQS34B	DQ36B/CQn36B	
4A	VREFB4AN0	IO			DIFFIO_RX_B58n	DIFFOUT_B115n	AL9	Yes	DQSn34B	DQ36B	
4A	VREFB4AN0	IO				DIFFOUT_B116p	AL7	Yes	DQ34B	DQ36B	
4A	VREFB4AN0	IO				DIFFOUT_B116n	AJ9	Yes	DQ34B	DQ36B	
4A	VREFB4AN0	IO			DIFFIO_RX_B59p	DIFFOUT_B117p	AN4	Yes	DQ35B	DQ37B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B59n	DIFFOUT_B117n	AP4	Yes	DQ35B	DQ37B	DQ38B

Bank Number	VREF	Pin Name/ Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
4A	VREFB4AN0	IO				DIFFOUT_B118p	AP2	Yes	DQ35B	DQ37B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B118n	AP5	Yes	DQ35B	DQ37B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B60p	DIFFOUT_B119p	AN3	Yes	DQS35B	DQS37B/CQ37B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B60n	DIFFOUT_B119n	AP3	Yes	DQSn35B	DQSn37B/DQ37B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B120p	AM6	Yes	DQ36B	DQ37B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B120n	AN6	Yes	DQ36B	DQ37B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B61p	DIFFOUT_B121p	AL5	Yes	DQS36B	DQ37B/CQn37B	DQS38B/CQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B61n	DIFFOUT_B121n	AM5	Yes	DQSn36B	DQ37B	DQSn38B/DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B122p	AL4	Yes	DQ36B	DQ37B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B122n	AM4	Yes	DQ36B	DQ37B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B62p	DIFFOUT_B123p	AJ7	Yes	DQ37B	DQ38B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B62n	DIFFOUT_B123n	AK7	Yes	DQ37B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B124p	AJ6	Yes	DQ37B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B124n	AK6	Yes	DQ37B	DQ38B	DQ38B
4A	VREFB4AN0	IO			DIFFIO_RX_B63p	DIFFOUT_B125p	AH8	Yes	DQS37B	DQS38B/CQ38B	DQ38B/CQn38B
4A	VREFB4AN0	IO			DIFFIO_RX_B63n	DIFFOUT_B125n	AJ8	Yes	DQSn37B	DQSn38B/DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B126p	AE11	Yes	DQ38B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B126n	AF11	Yes	DQ38B	DQ38B	DQ38B
4A	VREFB4AN0	IO	RUP4A		DIFFIO_RX_B64p	DIFFOUT_B127p	AG9	Yes	DQS38B	DQ38B/CQn38B	DQ38B
4A	VREFB4AN0	IO	RDN4A		DIFFIO_RX_B64n	DIFFOUT_B127n	AH9	Yes	DQSn38B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B128p	AE10	Yes	DQ38B	DQ38B	DQ38B
4A	VREFB4AN0	IO				DIFFOUT_B128n	AF10	Yes	DQ38B	DQ38B	DQ38B
		nIO_PULLUP		nIO_PULLUP			AF8	No			
		nCEO		nCEO			AJ5	No			
		DCLK		DCLK			AL3	No			
		nCSO		nCSO			AE9	No			
		ASDO		ASDO			AH6	No			
5A	VREFB5AN0	IO	PLL_R4_CLKOUT0n		DIFFIO_TX_R1n	DIFFOUT_R1n	AH4	Yes			
5A	VREFB5AN0	IO	PLL_R4_FB_CLKOUT0p		DIFFIO_TX_R1p	DIFFOUT_R1p	AH5	Yes			
5A	VREFB5AN0	IO	RDN5A		DIFFIO_RX_R1n	DIFFOUT_R2n	AK3	Yes			
5A	VREFB5AN0	IO	RUP5A		DIFFIO_RX_R1p	DIFFOUT_R2p	AK4	Yes			
5A	VREFB5AN0	IO			DIFFIO_TX_R2n	DIFFOUT_R3n	AE7	Yes	DQ1R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R2p	DIFFOUT_R3p	AE8	Yes	DQ1R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R2n	DIFFOUT_R4n	AM1	Yes	DQSn1R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R2p	DIFFOUT_R4p	AM2	Yes	DQS1R	DQ1R/CQn1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R3n	DIFFOUT_R5n	AF5	Yes	DQ1R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R3p	DIFFOUT_R5p	AF6	Yes	DQ1R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R3n	DIFFOUT_R6n	AJ3	Yes	DQSn2R	DQSn1R/DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R3p	DIFFOUT_R6p	AJ4	Yes	DQS2R	DQS1R/CQ1R	DQ1R/CQn1R
5A	VREFB5AN0	IO			DIFFIO_TX_R4n	DIFFOUT_R7n	AC8	Yes	DQ2R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R4p	DIFFOUT_R7p	AC9	Yes	DQ2R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R4n	DIFFOUT_R8n	AL1	Yes	DQ2R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R4p	DIFFOUT_R8p	AL2	Yes	DQ2R	DQ1R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R5n	DIFFOUT_R9n	AE5	Yes	DQ3R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R5p	DIFFOUT_R9p	AE6	Yes	DQ3R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R5n	DIFFOUT_R10n	AG3	Yes	DQSn3R	DQ2R	DQSn1R/DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R5p	DIFFOUT_R10p	AG4	Yes	DQS3R	DQ2R/CQn2R	DQS1R/CQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R6n	DIFFOUT_R11n	AB10	Yes	DQ3R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R6p	DIFFOUT_R11p	AC11	Yes	DQ3R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R6n	DIFFOUT_R12n	AK1	Yes	DQSn4R	DQSn2R/DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R6p	DIFFOUT_R12p	AJ2	Yes	DQS4R	DQS2R/CQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R7n	DIFFOUT_R13n	AD6	Yes	DQ4R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R7p	DIFFOUT_R13p	AD7	Yes	DQ4R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R7n	DIFFOUT_R14n	AJ1	Yes	DQ4R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_RX_R7p	DIFFOUT_R14p	AH2	Yes	DQ4R	DQ2R	DQ1R
5A	VREFB5AN0	IO			DIFFIO_TX_R8n	DIFFOUT_R15n	AC7	Yes	DQ5R	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_TX_R8p	DIFFOUT_R15p	AB8	Yes	DQ5R	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_RX_R8n	DIFFOUT_R16n	AF3	Yes	DQSn5R	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_RX_R8p	DIFFOUT_R16p	AF4	Yes	DQS5R	DQ3R/CQn3R	
5A	VREFB5AN0	IO			DIFFIO_TX_R9n	DIFFOUT_R17n	AB9	Yes	DQ5R	DQ3R	

Bank Number	VREF	Pin Name/ Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
5A	VREFB5AN0	IO			DIFFIO_TX_R9p	DIFFOUT_R17p	AA10	Yes	DQ5R	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_RX_R9n	DIFFOUT_R18n	AH1	Yes	DQSn6R	DQSn3R/DQ3R	
5A	VREFB5AN0	IO			DIFFIO_RX_R9p	DIFFOUT_R18p	AG1	Yes	DQS6R	DQS3R/CQ3R	
5A	VREFB5AN0	IO			DIFFIO_TX_R10n	DIFFOUT_R19n	AC5	Yes	DQ6R	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_TX_R10p	DIFFOUT_R19p	AC6	Yes	DQ6R	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_RX_R10n	DIFFOUT_R20n	AF1	Yes	DQ6R	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_RX_R10p	DIFFOUT_R20p	AF2	Yes	DQ6R	DQ3R	
5A	VREFB5AN0	IO			DIFFIO_TX_R11n	DIFFOUT_R21n	AB11	Yes	DQ7R		
5A	VREFB5AN0	IO			DIFFIO_TX_R11p	DIFFOUT_R21p	AA12	Yes	DQ7R		
5A	VREFB5AN0	IO			DIFFIO_RX_R11n	DIFFOUT_R22n	AE3	Yes	DQSn7R		
5A	VREFB5AN0	IO			DIFFIO_RX_R11p	DIFFOUT_R22p	AE4	Yes	DQS7R		
5A	VREFB5AN0	IO			DIFFIO_TX_R12n	DIFFOUT_R23n	AD3	Yes	DQ7R		
5A	VREFB5AN0	IO			DIFFIO_TX_R12p	DIFFOUT_R23p	AD4	Yes	DQ7R		
5A	VREFB5AN0	IO			DIFFIO_RX_R12n	DIFFOUT_R24n	AE1	Yes			
5A	VREFB5AN0	IO			DIFFIO_RX_R12p	DIFFOUT_R24p	AE2	Yes			
5C	VREFB5CN0	IO			DIFFIO_TX_R13n	DIFFOUT_R25n	AB5	Yes	DQ8R	DQ8R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_TX_R13p	DIFFOUT_R25p	AB6	Yes	DQ8R	DQ8R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_RX_R13n	DIFFOUT_R26n	AB3	Yes	DQSn8R	DQ8R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_RX_R13p	DIFFOUT_R26p	AC4	Yes	DQS8R	DQ8R/CQn8R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_TX_R14n	DIFFOUT_R27n	AA6	Yes	DQ8R	DQ8R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_TX_R14p	DIFFOUT_R27p	AA7	Yes	DQ8R	DQ8R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_RX_R14n	DIFFOUT_R28n	AD1	Yes	DQSn9R	DQSn8R/DQ8R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_RX_R14p	DIFFOUT_R28p	AC2	Yes	DQS9R	DQS8R/CQ8R	DQ8R/CQn8R
5C	VREFB5CN0	IO			DIFFIO_TX_R15n	DIFFOUT_R29n	Y9	Yes	DQ9R	DQ8R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_TX_R15p	DIFFOUT_R29p	Y10	Yes	DQ9R	DQ8R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_RX_R15n	DIFFOUT_R30n	AA3	Yes	DQ9R	DQ8R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_RX_R15p	DIFFOUT_R30p	AB4	Yes	DQ9R	DQ8R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_TX_R16n	DIFFOUT_R31n	Y7	Yes	DQ10R	DQ9R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_TX_R16p	DIFFOUT_R31p	Y8	Yes	DQ10R	DQ9R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_RX_R16n	DIFFOUT_R32n	AC1	Yes	DQSn10R	DQ9R	DQSn8R/DQ8R
5C	VREFB5CN0	IO			DIFFIO_RX_R16p	DIFFOUT_R32p	AB2	Yes	DQS10R	DQ9R/CQn9R	DQS8R/CQ8R
5C	VREFB5CN0	IO			DIFFIO_TX_R17n	DIFFOUT_R33n	Y11	Yes	DQ10R	DQ9R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_TX_R17p	DIFFOUT_R33p	W12	Yes	DQ10R	DQ9R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_RX_R17n	DIFFOUT_R34n	Y3	Yes	DQSn11R	DQSn9R/DQ9R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_RX_R17p	DIFFOUT_R34p	AA4	Yes	DQS11R	DQS9R/CQ9R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_TX_R18n	DIFFOUT_R35n	Y5	Yes	DQ11R	DQ9R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_TX_R18p	DIFFOUT_R35p	Y6	Yes	DQ11R	DQ9R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_RX_R18n	DIFFOUT_R36n	AB1	Yes	DQ11R	DQ9R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_RX_R18p	DIFFOUT_R36p	AA1	Yes	DQ11R	DQ9R	DQ8R
5C	VREFB5CN0	IO			DIFFIO_TX_R19n	DIFFOUT_R37n	W7	Yes	DQ12R	DQ10R	
5C	VREFB5CN0	IO			DIFFIO_TX_R19p	DIFFOUT_R37p	W8	Yes	DQ12R	DQ10R	
5C	VREFB5CN0	IO			DIFFIO_RX_R19n	DIFFOUT_R38n	W3	Yes	DQSn12R	DQ10R	
5C	VREFB5CN0	IO			DIFFIO_RX_R19p	DIFFOUT_R38p	Y4	Yes	DQS12R	DQ10R/CQn10R	
5C	VREFB5CN0	IO			DIFFIO_TX_R20n	DIFFOUT_R39n	W10	Yes	DQ12R	DQ10R	
5C	VREFB5CN0	IO			DIFFIO_TX_R20p	DIFFOUT_R39p	W11	Yes	DQ12R	DQ10R	
5C	VREFB5CN0	IO			DIFFIO_RX_R20n	DIFFOUT_R40n	Y1	Yes	DQSn13R	DQSn10R/DQ10R	
5C	VREFB5CN0	IO			DIFFIO_RX_R20p	DIFFOUT_R40p	Y2	Yes	DQS13R	DQS10R/CQ10R	
5C	VREFB5CN0	IO			DIFFIO_TX_R21n	DIFFOUT_R41n	W5	Yes	DQ13R	DQ10R	
5C	VREFB5CN0	IO			DIFFIO_TX_R21p	DIFFOUT_R41p	W6	Yes	DQ13R	DQ10R	
5C	VREFB5CN0	IO			DIFFIO_RX_R21n	DIFFOUT_R42n	V3	Yes	DQ13R	DQ10R	
5C	VREFB5CN0	IO			DIFFIO_RX_R21p	DIFFOUT_R42p	V4	Yes	DQ13R	DQ10R	
5C	VREFB5CN0	IO	PLL_R3_CLKOUT0n		DIFFIO_TX_R22n	DIFFOUT_R43n	W9	No			
5C	VREFB5CN0	IO	PLL_R3_FB_CLKOUT0p		DIFFIO_TX_R22p	DIFFOUT_R43p	V10	No			
5C	VREFB5CN0	IO	CLK9n		DIFFIO_RX_R22n	DIFFOUT_R44n	U3	No			
5C	VREFB5CN0	IO	CLK9p		DIFFIO_RX_R22p	DIFFOUT_R44p	U4	No			
5C	VREFB5CN0	CLK8n	CLK8n				W1	No			
5C	VREFB5CN0	CLK8p	CLK8p				W2	No			
6C	VREFB6CN0	CLK10p	CLK10p				U2	No			
6C	VREFB6CN0	CLK10n	CLK10n				U1	No			
6C	VREFB6CN0	IO	CLK11p		DIFFIO_RX_R23p	DIFFOUT_R45p	T2	No			

Bank Number	VREF	Pin Name/ Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
6C	VREFB6CN0	IO	CLK11n		DIFFIO_RX_R23n	DIFFOUT_R45n	T1	No			
6C	VREFB6CN0	IO	PLL_R2_FB_CLKOUT0p		DIFFIO_TX_R23p	DIFFOUT_R46p	U11	No			
6C	VREFB6CN0	IO	PLL_R2_CLKOUT0n		DIFFIO_TX_R23n	DIFFOUT_R46n	U10	No			
6C	VREFB6CN0	IO			DIFFIO_RX_R24p	DIFFOUT_R47p	P2	Yes	DQ14R	DQ17R	
6C	VREFB6CN0	IO			DIFFIO_RX_R24n	DIFFOUT_R47n	R1	Yes	DQ14R	DQ17R	
6C	VREFB6CN0	IO			DIFFIO_TX_R24p	DIFFOUT_R48p	T7	Yes	DQ14R	DQ17R	
6C	VREFB6CN0	IO			DIFFIO_TX_R24n	DIFFOUT_R48n	U6	Yes	DQ14R	DQ17R	
6C	VREFB6CN0	IO			DIFFIO_RX_R25p	DIFFOUT_R49p	R4	Yes	DQS14R	DQS17R/CQ17R	
6C	VREFB6CN0	IO			DIFFIO_RX_R25n	DIFFOUT_R49n	R3	Yes	DQSn14R	DQSn17R/DQ17R	
6C	VREFB6CN0	IO			DIFFIO_TX_R25p	DIFFOUT_R50p	T9	Yes	DQ15R	DQ17R	
6C	VREFB6CN0	IO			DIFFIO_TX_R25n	DIFFOUT_R50n	T8	Yes	DQ15R	DQ17R	
6C	VREFB6CN0	IO			DIFFIO_RX_R26p	DIFFOUT_R51p	N2	Yes	DQS15R	DQ17R/CQn17R	
6C	VREFB6CN0	IO			DIFFIO_RX_R26n	DIFFOUT_R51n	P1	Yes	DQSn15R	DQ17R	
6C	VREFB6CN0	IO			DIFFIO_TX_R26p	DIFFOUT_R52p	T5	Yes	DQ15R	DQ17R	
6C	VREFB6CN0	IO			DIFFIO_TX_R26n	DIFFOUT_R52n	T4	Yes	DQ15R	DQ17R	
6C	VREFB6CN0	IO			DIFFIO_RX_R27p	DIFFOUT_R53p	P4	Yes	DQ16R	DQ18R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_RX_R27n	DIFFOUT_R53n	P3	Yes	DQ16R	DQ18R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R27p	DIFFOUT_R54p	R7	Yes	DQ16R	DQ18R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R27n	DIFFOUT_R54n	R6	Yes	DQ16R	DQ18R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_RX_R28p	DIFFOUT_R55p	M1	Yes	DQS16R	DQS18R/CQ18R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_RX_R28n	DIFFOUT_R55n	N1	Yes	DQSn16R	DQSn18R/DQ18R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R28p	DIFFOUT_R56p	P6	Yes	DQ17R	DQ18R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R28n	DIFFOUT_R56n	P5	Yes	DQ17R	DQ18R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_RX_R29p	DIFFOUT_R57p	N4	Yes	DQS17R	DQ18R/CQn18R	DQS19R/CQ19R
6C	VREFB6CN0	IO			DIFFIO_RX_R29n	DIFFOUT_R57n	N3	Yes	DQSn17R	DQ18R	DQSn19R/DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R29p	DIFFOUT_R58p	R12	Yes	DQ17R	DQ18R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R29n	DIFFOUT_R58n	T11	Yes	DQ17R	DQ18R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_RX_R30p	DIFFOUT_R59p	L2	Yes	DQ18R	DQ19R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_RX_R30n	DIFFOUT_R59n	L1	Yes	DQ18R	DQ19R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R30p	DIFFOUT_R60p	R10	Yes	DQ18R	DQ19R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R30n	DIFFOUT_R60n	R9	Yes	DQ18R	DQ19R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_RX_R31p	DIFFOUT_R61p	M4	Yes	DQS18R	DQS19R/CQ19R	DQ19R/CQn19R
6C	VREFB6CN0	IO			DIFFIO_RX_R31n	DIFFOUT_R61n	M3	Yes	DQSn18R	DQSn19R/DQ19R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R31p	DIFFOUT_R62p	P8	Yes	DQ19R	DQ19R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R31n	DIFFOUT_R62n	P7	Yes	DQ19R	DQ19R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_RX_R32p	DIFFOUT_R63p	K2	Yes	DQS19R	DQ19R/CQn19R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_RX_R32n	DIFFOUT_R63n	K1	Yes	DQSn19R	DQ19R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R32p	DIFFOUT_R64p	N6	Yes	DQ19R	DQ19R	DQ19R
6C	VREFB6CN0	IO			DIFFIO_TX_R32n	DIFFOUT_R64n	N5	Yes	DQ19R	DQ19R	DQ19R
6A	VREFB6AN0	IO			DIFFIO_RX_R33p	DIFFOUT_R65p	H2	Yes			
6A	VREFB6AN0	IO			DIFFIO_RX_R33n	DIFFOUT_R65n	J1	Yes			
6A	VREFB6AN0	IO			DIFFIO_TX_R33p	DIFFOUT_R66p	P11	Yes	DQ20R		
6A	VREFB6AN0	IO			DIFFIO_TX_R33n	DIFFOUT_R66n	P10	Yes	DQ20R		
6A	VREFB6AN0	IO			DIFFIO_RX_R34p	DIFFOUT_R67p	K4	Yes	DQS20R		
6A	VREFB6AN0	IO			DIFFIO_RX_R34n	DIFFOUT_R67n	K3	Yes	DQSn20R		
6A	VREFB6AN0	IO			DIFFIO_TX_R34p	DIFFOUT_R68p	M7	Yes	DQ20R		
6A	VREFB6AN0	IO			DIFFIO_TX_R34n	DIFFOUT_R68n	M6	Yes	DQ20R		
6A	VREFB6AN0	IO			DIFFIO_RX_R35p	DIFFOUT_R69p	G2	Yes	DQ21R	DQ24R	
6A	VREFB6AN0	IO			DIFFIO_RX_R35n	DIFFOUT_R69n	H1	Yes	DQ21R	DQ24R	
6A	VREFB6AN0	IO			DIFFIO_TX_R35p	DIFFOUT_R70p	L5	Yes	DQ21R	DQ24R	
6A	VREFB6AN0	IO			DIFFIO_TX_R35n	DIFFOUT_R70n	L4	Yes	DQ21R	DQ24R	
6A	VREFB6AN0	IO			DIFFIO_RX_R36p	DIFFOUT_R71p	J4	Yes	DQS21R	DQS24R/CQ24R	
6A	VREFB6AN0	IO			DIFFIO_RX_R36n	DIFFOUT_R71n	J3	Yes	DQSn21R	DQSn24R/DQ24R	
6A	VREFB6AN0	IO			DIFFIO_TX_R36p	DIFFOUT_R72p	L7	Yes	DQ22R	DQ24R	
6A	VREFB6AN0	IO			DIFFIO_TX_R36n	DIFFOUT_R72n	L6	Yes	DQ22R	DQ24R	
6A	VREFB6AN0	IO			DIFFIO_RX_R37p	DIFFOUT_R73p	F1	Yes	DQS22R	DQ24R/CQn24R	
6A	VREFB6AN0	IO			DIFFIO_RX_R37n	DIFFOUT_R73n	G1	Yes	DQSn22R	DQ24R	
6A	VREFB6AN0	IO			DIFFIO_TX_R37p	DIFFOUT_R74p	N9	Yes	DQ22R	DQ24R	
6A	VREFB6AN0	IO			DIFFIO_TX_R37n	DIFFOUT_R74n	N8	Yes	DQ22R	DQ24R	
6A	VREFB6AN0	IO			DIFFIO_RX_R38p	DIFFOUT_R75p	H4	Yes	DQ23R	DQ25R	DQ26R

Bank Number	VREF	Pin Name/ Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
6A	VREFB6AN0	IO			DIFFIO_RX_R38n	DIFFOUT_R75n	H3	Yes	DQ23R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R38p	DIFFOUT_R76p	K6	Yes	DQ23R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R38n	DIFFOUT_R76n	K5	Yes	DQ23R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R39p	DIFFOUT_R77p	E2	Yes	DQS23R	DQS25R/CQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R39n	DIFFOUT_R77n	E1	Yes	DQSn23R	DQSn25R/DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R39p	DIFFOUT_R78p	N11	Yes	DQ24R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R39n	DIFFOUT_R78n	N10	Yes	DQ24R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R40p	DIFFOUT_R79p	F4	Yes	DQS24R	DQ25R/CQn25R	DQS26R/CQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R40n	DIFFOUT_R79n	F3	Yes	DQSn24R	DQ25R	DQSn26R/DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R40p	DIFFOUT_R80p	J7	Yes	DQ24R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R40n	DIFFOUT_R80n	J6	Yes	DQ24R	DQ25R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R41p	DIFFOUT_R81p	G5	Yes	DQ25R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R41n	DIFFOUT_R81n	G4	Yes	DQ25R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R41p	DIFFOUT_R82p	K8	Yes	DQ25R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R41n	DIFFOUT_R82n	K7	Yes	DQ25R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R42p	DIFFOUT_R83p	C1	Yes	DQS25R	DQS26R/CQ26R	DQ26R/CQn26R
6A	VREFB6AN0	IO			DIFFIO_RX_R42n	DIFFOUT_R83n	D1	Yes	DQSn25R	DQSn26R/DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R42p	DIFFOUT_R84p	M10	Yes	DQ26R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R42n	DIFFOUT_R84n	M9	Yes	DQ26R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R43p	DIFFOUT_R85p	D3	Yes	DQS26R	DQ26R/CQn26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_RX_R43n	DIFFOUT_R85n	D2	Yes	DQSn26R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R43p	DIFFOUT_R86p	L9	Yes	DQ26R	DQ26R	DQ26R
6A	VREFB6AN0	IO			DIFFIO_TX_R43n	DIFFOUT_R86n	L8	Yes	DQ26R	DQ26R	DQ26R
6A	VREFB6AN0	IO	RUP6A		DIFFIO_RX_R44p	DIFFOUT_R87p	E4	Yes			
6A	VREFB6AN0	IO	RDN6A		DIFFIO_RX_R44n	DIFFOUT_R87n	E3	Yes			
6A	VREFB6AN0	IO	PLL_R1_FB_CLKOUT0p		DIFFIO_TX_R44p	DIFFOUT_R88p	H6	Yes			
6A	VREFB6AN0	IO	PLL_R1_CLKOUT0n		DIFFIO_TX_R44n	DIFFOUT_R88n	H5	Yes			
		MSEL2		MSEL2			K9	No			
		MSEL1		MSEL1			J9	No			
		MSEL0		MSEL0			K10	No			
7A	VREFB7AN0	IO				DIFFOUT_T1n	F8	Yes	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T1p	F6	Yes	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO	RDN7A		DIFFIO_RX_T1n	DIFFOUT_T2n	E7	Yes	DQSn1T	DQ1T	DQ1T
7A	VREFB7AN0	IO	RUP7A		DIFFIO_RX_T1p	DIFFOUT_T2p	F7	Yes	DQS1T	DQ1T/CQn1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T3n	F9	Yes	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T3p	G8	Yes	DQ1T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T2n	DIFFOUT_T4n	C3	Yes	DQSn2T	DQSn1T/DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T2p	DIFFOUT_T4p	C4	Yes	DQS2T	DQS1T/CQ1T	DQ1T/CQn1T
7A	VREFB7AN0	IO				DIFFOUT_T5n	C6	Yes	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T5p	D6	Yes	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T3n	DIFFOUT_T6n	B5	Yes	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T3p	DIFFOUT_T6p	C5	Yes	DQ2T	DQ1T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T7n	J11	Yes	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T7p	G9	Yes	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T4n	DIFFOUT_T8n	G11	Yes	DQSn3T	DQ2T	DQSn1T/DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T4p	DIFFOUT_T8p	H11	Yes	DQS3T	DQ2T/CQn2T	DQS1T/CQ1T
7A	VREFB7AN0	IO				DIFFOUT_T9n	J12	Yes	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T9p	G10	Yes	DQ3T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T5n	DIFFOUT_T10n	A2	Yes	DQSn4T	DQSn2T/DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T5p	DIFFOUT_T10p	B2	Yes	DQS4T	DQS2T/CQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T11n	A5	Yes	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T11p	A3	Yes	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T6n	DIFFOUT_T12n	A4	Yes	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO			DIFFIO_RX_T6p	DIFFOUT_T12p	B4	Yes	DQ4T	DQ2T	DQ1T
7A	VREFB7AN0	IO				DIFFOUT_T13n	D7	Yes	DQ5T	DQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T13p	E8	Yes	DQ5T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T7n	DIFFOUT_T14n	C9	Yes	DQSn5T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T7p	DIFFOUT_T14p	D9	Yes	DQS5T	DQ3T/CQn3T	
7A	VREFB7AN0	IO				DIFFOUT_T15n	E10	Yes	DQ5T	DQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T15p	D8	Yes	DQ5T	DQ3T	

Bank Number	VREF	Pin Name/ Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
7A	VREFB7AN0	IO			DIFFIO_RX_T8n	DIFFOUT_T16n	A7	Yes	DQSn6T	DQSn3T/DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T8p	DIFFOUT_T16p	B7	Yes	DQS6T	DQS3T/CQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T17n	A6	Yes	DQ6T	DQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T17p	C7	Yes	DQ6T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T9n	DIFFOUT_T18n	A8	Yes	DQ6T	DQ3T	
7A	VREFB7AN0	IO			DIFFIO_RX_T9p	DIFFOUT_T18p	B8	Yes	DQ6T	DQ3T	
7A	VREFB7AN0	IO				DIFFOUT_T19n	M13	Yes			
7A	VREFB7AN0	IO				DIFFOUT_T19p	L13	Yes			
7A	VREFB7AN0	IO			DIFFIO_RX_T10n	DIFFOUT_T20n	K11	Yes			
7A	VREFB7AN0	IO			DIFFIO_RX_T10p	DIFFOUT_T20p	K12	Yes			
7B	VREFB7BN0	IO				DIFFOUT_T25n	G12	Yes	DQ9T	DQ9T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T25p	F11	Yes	DQ9T	DQ9T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T13n	DIFFOUT_T26n	F12	Yes	DQSn9T	DQ9T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T13p	DIFFOUT_T26p	F13	Yes	DQS9T	DQ9T/CQn9T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T27n	G13	Yes	DQ9T	DQ9T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T27p	E11	Yes	DQ9T	DQ9T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T14n	DIFFOUT_T28n	C11	Yes	DQSn10T	DQSn9T/DQ9T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T14p	DIFFOUT_T28p	D11	Yes	DQS10T	DQS9T/CQ9T	DQ9T/CQn9T
7B	VREFB7BN0	IO				DIFFOUT_T29n	D13	Yes	DQ10T	DQ9T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T29p	D10	Yes	DQ10T	DQ9T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T15n	DIFFOUT_T30n	C12	Yes	DQ10T	DQ9T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T15p	DIFFOUT_T30p	D12	Yes	DQ10T	DQ9T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T31n	K14	Yes	DQ11T	DQ10T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T31p	K13	Yes	DQ11T	DQ10T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T16n	DIFFOUT_T32n	H14	Yes	DQSn11T	DQ10T	DQSn9T/DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T16p	DIFFOUT_T32p	J14	Yes	DQS11T	DQ10T/CQn10T	DQS9T/CQ9T
7B	VREFB7BN0	IO				DIFFOUT_T33n	K15	Yes	DQ11T	DQ10T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T33p	L14	Yes	DQ11T	DQ10T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T17n	DIFFOUT_T34n	A10	Yes	DQSn12T	DQSn10T/DQ10T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T17p	DIFFOUT_T34p	B10	Yes	DQS12T	DQS10T/CQ10T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T35n	A12	Yes	DQ12T	DQ10T	DQ9T
7B	VREFB7BN0	IO				DIFFOUT_T35p	A9	Yes	DQ12T	DQ10T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T18n	DIFFOUT_T36n	A11	Yes	DQ12T	DQ10T	DQ9T
7B	VREFB7BN0	IO			DIFFIO_RX_T18p	DIFFOUT_T36p	B11	Yes	DQ12T	DQ10T	DQ9T
7C	VREFB7CN0	IO				DIFFOUT_T49n	D14	Yes	DQ17T	DQ17T	
7C	VREFB7CN0	IO				DIFFOUT_T49p	E13	Yes	DQ17T	DQ17T	
7C	VREFB7CN0	IO			DIFFIO_RX_T25n	DIFFOUT_T50n	E14	Yes	DQSn17T	DQ17T	
7C	VREFB7CN0	IO			DIFFIO_RX_T25p	DIFFOUT_T50p	F14	Yes	DQS17T	DQ17T/CQn17T	
7C	VREFB7CN0	IO				DIFFOUT_T51n	F15	Yes	DQ17T	DQ17T	
7C	VREFB7CN0	IO				DIFFOUT_T51p	D15	Yes	DQ17T	DQ17T	
7C	VREFB7CN0	IO			DIFFIO_RX_T26n	DIFFOUT_T52n	A13	Yes	DQSn18T	DQSn17T/DQ17T	
7C	VREFB7CN0	IO			DIFFIO_RX_T26p	DIFFOUT_T52p	B13	Yes	DQS18T	DQS17T/CQ17T	
7C	VREFB7CN0	IO				DIFFOUT_T53n	A15	Yes	DQ18T	DQ17T	
7C	VREFB7CN0	IO				DIFFOUT_T53p	C14	Yes	DQ18T	DQ17T	
7C	VREFB7CN0	IO			DIFFIO_RX_T27n	DIFFOUT_T54n	A14	Yes	DQ18T	DQ17T	
7C	VREFB7CN0	IO			DIFFIO_RX_T27p	DIFFOUT_T54p	B14	Yes	DQ18T	DQ17T	
7C	VREFB7CN0	IO				DIFFOUT_T55n	C17	Yes	DQ19T		
7C	VREFB7CN0	IO				DIFFOUT_T55p	C15	Yes	DQ19T		
7C	VREFB7CN0	IO			DIFFIO_RX_T28n	DIFFOUT_T56n	C16	Yes	DQSn19T		
7C	VREFB7CN0	IO			DIFFIO_RX_T28p	DIFFOUT_T56p	D16	Yes	DQS19T		
7C	VREFB7CN0	IO				DIFFOUT_T57n	D17	Yes	DQ19T		
7C	VREFB7CN0	IO				DIFFOUT_T57p	E17	Yes	DQ19T		
7C	VREFB7CN0	IO			DIFFIO_RX_T29n	DIFFOUT_T58n	J16	Yes			
7C	VREFB7CN0	IO			DIFFIO_RX_T29p	DIFFOUT_T58p	J15	Yes			
7C	VREFB7CN0	IO	PLL_T2_CLKOUT4			DIFFOUT_T59n	L16	No			
7C	VREFB7CN0	IO	PLL_T2_CLKOUT3			DIFFOUT_T59p	K16	No			
7C	VREFB7CN0	IO			DIFFIO_RX_T30n	DIFFOUT_T60n	G16	No			
7C	VREFB7CN0	IO			DIFFIO_RX_T30p	DIFFOUT_T60p	H16	No			
7C	VREFB7CN0	IO	PLL_T2_CLKOUT0n			DIFFOUT_T61n	K17	No			
7C	VREFB7CN0	IO	PLL_T2_CLKOUT0p			DIFFOUT_T61p	L17	No			

Bank Number	VREF	Pin Name/ Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
7C	VREFB7CN0	IO	PLL_T2_FBn/CLKOUT2		DIFFIO_RX_T31n	DIFFOUT_T62n	E16	No			
7C	VREFB7CN0	IO	PLL_T2_FBp/CLKOUT1		DIFFIO_RX_T31p	DIFFOUT_T62p	F16	No			
7C	VREFB7CN0	IO	CLK13n			DIFFOUT_T63n	A16	No			
7C	VREFB7CN0	IO	CLK13p			DIFFOUT_T63p	B16	No			
7C	VREFB7CN0	IO	CLK12n		DIFFIO_RX_T32n	DIFFOUT_T64n	A17	No			
7C	VREFB7CN0	IO	CLK12p		DIFFIO_RX_T32p	DIFFOUT_T64p	B17	No			
8C	VREFB8CN0	IO	CLK14p		DIFFIO_RX_T33p	DIFFOUT_T65p	B19	No			
8C	VREFB8CN0	IO	CLK14n		DIFFIO_RX_T33n	DIFFOUT_T65n	A19	No			
8C	VREFB8CN0	IO	CLK15p			DIFFOUT_T66p	B20	No			
8C	VREFB8CN0	IO	CLK15n			DIFFOUT_T66n	A20	No			
8C	VREFB8CN0	IO	PLL_T1_FBp/CLKOUT1		DIFFIO_RX_T34p	DIFFOUT_T67p	D18	No			
8C	VREFB8CN0	IO	PLL_T1_FBn/CLKOUT2		DIFFIO_RX_T34n	DIFFOUT_T67n	C18	No			
8C	VREFB8CN0	IO	PLL_T1_CLKOUT0p			DIFFOUT_T68p	K19	No			
8C	VREFB8CN0	IO	PLL_T1_CLKOUT0n			DIFFOUT_T68n	J19	No			
8C	VREFB8CN0	IO			DIFFIO_RX_T35p	DIFFOUT_T69p	D19	No			
8C	VREFB8CN0	IO			DIFFIO_RX_T35n	DIFFOUT_T69n	C19	No			
8C	VREFB8CN0	IO	PLL_T1_CLKOUT3			DIFFOUT_T70p	L19	No			
8C	VREFB8CN0	IO	PLL_T1_CLKOUT4			DIFFOUT_T70n	L20	No			
8C	VREFB8CN0	IO			DIFFIO_RX_T36p	DIFFOUT_T71p	F19	Yes			
8C	VREFB8CN0	IO			DIFFIO_RX_T36n	DIFFOUT_T71n	E19	Yes			
8C	VREFB8CN0	IO				DIFFOUT_T72p	C20	Yes	DQ20T		
8C	VREFB8CN0	IO				DIFFOUT_T72n	D20	Yes	DQ20T		
8C	VREFB8CN0	IO			DIFFIO_RX_T37p	DIFFOUT_T73p	D21	Yes	DQS20T		
8C	VREFB8CN0	IO			DIFFIO_RX_T37n	DIFFOUT_T73n	C21	Yes	DQSn20T		
8C	VREFB8CN0	IO				DIFFOUT_T74p	D22	Yes	DQ20T		
8C	VREFB8CN0	IO				DIFFOUT_T74n	E22	Yes	DQ20T		
8C	VREFB8CN0	IO			DIFFIO_RX_T38p	DIFFOUT_T75p	G20	Yes	DQ21T	DQ22T	
8C	VREFB8CN0	IO			DIFFIO_RX_T38n	DIFFOUT_T75n	F20	Yes	DQ21T	DQ22T	
8C	VREFB8CN0	IO				DIFFOUT_T76p	E20	Yes	DQ21T	DQ22T	
8C	VREFB8CN0	IO				DIFFOUT_T76n	H20	Yes	DQ21T	DQ22T	
8C	VREFB8CN0	IO			DIFFIO_RX_T39p	DIFFOUT_T77p	G21	Yes	DQS21T	DQS22T/CQ22T	
8C	VREFB8CN0	IO			DIFFIO_RX_T39n	DIFFOUT_T77n	F21	Yes	DQSn21T	DQSn22T/DQ22T	
8C	VREFB8CN0	IO				DIFFOUT_T78p	A22	Yes	DQ22T	DQ22T	
8C	VREFB8CN0	IO				DIFFOUT_T78n	A21	Yes	DQ22T	DQ22T	
8C	VREFB8CN0	IO			DIFFIO_RX_T40p	DIFFOUT_T79p	B23	Yes	DQS22T	DQ22T/CQn22T	
8C	VREFB8CN0	IO			DIFFIO_RX_T40n	DIFFOUT_T79n	A23	Yes	DQSn22T	DQ22T	
8C	VREFB8CN0	IO				DIFFOUT_T80p	B22	Yes	DQ22T	DQ22T	
8C	VREFB8CN0	IO				DIFFOUT_T80n	C23	Yes	DQ22T	DQ22T	
8B	VREFB8BN0	IO			DIFFIO_RX_T47p	DIFFOUT_T93p	B25	Yes	DQ27T	DQ29T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T47n	DIFFOUT_T93n	A25	Yes	DQ27T	DQ29T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T94p	A24	Yes	DQ27T	DQ29T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T94n	A26	Yes	DQ27T	DQ29T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T48p	DIFFOUT_T95p	C26	Yes	DQS27T	DQS29T/CQ29T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T48n	DIFFOUT_T95n	B26	Yes	DQSn27T	DQSn29T/DQ29T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T96p	K20	Yes	DQ28T	DQ29T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T96n	J20	Yes	DQ28T	DQ29T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T49p	DIFFOUT_T97p	J22	Yes	DQS28T	DQ29T/CQn29T	DQS30T/CQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T49n	DIFFOUT_T97n	J21	Yes	DQSn28T	DQ29T	DQSn30T/DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T98p	K21	Yes	DQ28T	DQ29T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T98n	K22	Yes	DQ28T	DQ29T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T50p	DIFFOUT_T99p	D25	Yes	DQ29T	DQ30T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T50n	DIFFOUT_T99n	D24	Yes	DQ29T	DQ30T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T100p	C24	Yes	DQ29T	DQ30T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T100n	E25	Yes	DQ29T	DQ30T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T51p	DIFFOUT_T101p	E23	Yes	DQS29T	DQS30T/CQ30T	DQ30T/CQn30T
8B	VREFB8BN0	IO			DIFFIO_RX_T51n	DIFFOUT_T101n	D23	Yes	DQSn29T	DQSn30T/DQ30T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T102p	A27	Yes	DQ30T	DQ30T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T102n	C27	Yes	DQ30T	DQ30T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T52p	DIFFOUT_T103p	B28	Yes	DQS30T	DQ30T/CQn30T	DQ30T
8B	VREFB8BN0	IO			DIFFIO_RX_T52n	DIFFOUT_T103n	A28	Yes	DQSn30T	DQ30T	DQ30T

Bank Number	VREF	Pin Name/ Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
8B	VREFB8BN0	IO				DIFFOUT_T104p	C28	Yes	DQ30T	DQ30T	DQ30T
8B	VREFB8BN0	IO				DIFFOUT_T104n	A29	Yes	DQ30T	DQ30T	DQ30T
8A	VREFB8AN0	IO			DIFFIO_RX_T55p	DIFFOUT_T109p	M23	Yes			
8A	VREFB8AN0	IO			DIFFIO_RX_T55n	DIFFOUT_T109n	L23	Yes			
8A	VREFB8AN0	IO				DIFFOUT_T110p	L22	Yes			
8A	VREFB8AN0	IO				DIFFOUT_T110n	K23	Yes			
8A	VREFB8AN0	IO			DIFFIO_RX_T56p	DIFFOUT_T111p	G23	Yes	DQ33T	DQ36T	
8A	VREFB8AN0	IO			DIFFIO_RX_T56n	DIFFOUT_T111n	F23	Yes	DQ33T	DQ36T	
8A	VREFB8AN0	IO				DIFFOUT_T112p	F22	Yes	DQ33T	DQ36T	
8A	VREFB8AN0	IO				DIFFOUT_T112n	H23	Yes	DQ33T	DQ36T	
8A	VREFB8AN0	IO			DIFFIO_RX_T57p	DIFFOUT_T113p	G24	Yes	DQS33T	DQS36T/CQ36T	
8A	VREFB8AN0	IO			DIFFIO_RX_T57n	DIFFOUT_T113n	F24	Yes	DQSn33T	DQSn36T/DQ36T	
8A	VREFB8AN0	IO				DIFFOUT_T114p	F25	Yes	DQ34T	DQ36T	
8A	VREFB8AN0	IO				DIFFOUT_T114n	D27	Yes	DQ34T	DQ36T	
8A	VREFB8AN0	IO			DIFFIO_RX_T58p	DIFFOUT_T115p	E26	Yes	DQS34T	DQ36T/CQn36T	
8A	VREFB8AN0	IO			DIFFIO_RX_T58n	DIFFOUT_T115n	D26	Yes	DQSn34T	DQ36T	
8A	VREFB8AN0	IO				DIFFOUT_T116p	F26	Yes	DQ34T	DQ36T	
8A	VREFB8AN0	IO				DIFFOUT_T116n	D28	Yes	DQ34T	DQ36T	
8A	VREFB8AN0	IO			DIFFIO_RX_T59p	DIFFOUT_T117p	B31	Yes	DQ35T	DQ37T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T59n	DIFFOUT_T117n	A31	Yes	DQ35T	DQ37T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T118p	A30	Yes	DQ35T	DQ37T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T118n	A33	Yes	DQ35T	DQ37T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T60p	DIFFOUT_T119p	B32	Yes	DQS35T	DQS37T/CQ37T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T60n	DIFFOUT_T119n	A32	Yes	DQSn35T	DQSn37T/DQ37T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T120p	C29	Yes	DQ36T	DQ37T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T120n	B29	Yes	DQ36T	DQ37T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T61p	DIFFOUT_T121p	D30	Yes	DQS36T	DQ37T/CQn37T	DQS38T/CQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T61n	DIFFOUT_T121n	C30	Yes	DQSn36T	DQ37T	DQSn38T/DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T122p	C31	Yes	DQ36T	DQ37T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T122n	D31	Yes	DQ36T	DQ37T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T62p	DIFFOUT_T123p	F28	Yes	DQ37T	DQ38T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T62n	DIFFOUT_T123n	E28	Yes	DQ37T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T124p	F27	Yes	DQ37T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T124n	G27	Yes	DQ37T	DQ38T	DQ38T
8A	VREFB8AN0	IO			DIFFIO_RX_T63p	DIFFOUT_T125p	F29	Yes	DQS37T	DQS38T/CQ38T	DQ38T/CQn38T
8A	VREFB8AN0	IO			DIFFIO_RX_T63n	DIFFOUT_T125n	E29	Yes	DQSn37T	DQSn38T/DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T126p	J24	Yes	DQ38T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T126n	K24	Yes	DQ38T	DQ38T	DQ38T
8A	VREFB8AN0	IO	RUP8A		DIFFIO_RX_T64p	DIFFOUT_T127p	H26	Yes	DQS38T	DQ38T/CQn38T	DQ38T
8A	VREFB8AN0	IO	RDN8A		DIFFIO_RX_T64n	DIFFOUT_T127n	G26	Yes	DQSn38T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T128p	J25	Yes	DQ38T	DQ38T	DQ38T
8A	VREFB8AN0	IO				DIFFOUT_T128n	K25	Yes	DQ38T	DQ38T	DQ38T
		GND					AF9	No			
		GND					V17	No			
		GND					B33	No			
		GND					AN2	No			
		GND					AN5	No			
		GND					AN8	No			
		GND					AN11	No			
		GND					AN14	No			
		GND					AN17	No			
		GND					AN20	No			
		GND					AN23	No			
		GND					AN26	No			
		GND					AN29	No			
		GND					AN32	No			
		GND					AM33	No			
		GND					AK2	No			
		GND					AK5	No			
		GND					AK8	No			

Bank Number	VREF	Pin Name/ Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
		GND					AK11	No			
		GND					AK14	No			
		GND					AK17	No			
		GND					AK20	No			
		GND					AK23	No			
		GND					AK26	No			
		GND					AK29	No			
		GND					AJ30	No			
		GND					AJ33	No			
		GND					AG2	No			
		GND					AG5	No			
		GND					AG8	No			
		GND					AG11	No			
		GND					AG14	No			
		GND					AG17	No			
		GND					AG20	No			
		GND					AG23	No			
		GND					AG26	No			
		GND					AF27	No			
		GND					AF30	No			
		GND					AF33	No			
		GND					AD2	No			
		GND					AD5	No			
		GND					AD8	No			
		GND					AD11	No			
		GND					AD14	No			
		GND					AD17	No			
		GND					AD20	No			
		GND					AD23	No			
		GND					AC14	No			
		GND					AC16	No			
		GND					AC18	No			
		GND					AC20	No			
		GND					AC24	No			
		GND					AC27	No			
		GND					AC30	No			
		GND					AC33	No			
		GND					AB13	No			
		GND					AB15	No			
		GND					AB17	No			
		GND					AB19	No			
		GND					AB21	No			
		GND					AB23	No			
		GND					AA2	No			
		GND					AA5	No			
		GND					AA8	No			
		GND					AA11	No			
		GND					AA14	No			
		GND					AA16	No			
		GND					AA18	No			
		GND					AA20	No			
		GND					AA22	No			
		GND					Y13	No			
		GND					Y15	No			
		GND					Y17	No			
		GND					Y19	No			
		GND					Y21	No			
		GND					Y24	No			
		GND					Y27	No			
		GND					Y30	No			

Bank Number	VREF	Pin Name/ Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
		GND					Y33	No			
		GND					W14	No			
		GND					W16	No			
		GND					W18	No			
		GND					W20	No			
		GND					W22	No			
		GND					V2	No			
		GND					V5	No			
		GND					V8	No			
		GND					V11	No			
		GND					V12	No			
		GND					V13	No			
		GND					V15	No			
		GND					V19	No			
		GND					V21	No			
		GND					V23	No			
		GND					U12	No			
		GND					U14	No			
		GND					U16	No			
		GND					U20	No			
		GND					U22	No			
		GND					U23	No			
		GND					U24	No			
		GND					U27	No			
		GND					U30	No			
		GND					U33	No			
		GND					T13	No			
		GND					T15	No			
		GND					T17	No			
		GND					T19	No			
		GND					T21	No			
		GND					R2	No			
		GND					R5	No			
		GND					R8	No			
		GND					R11	No			
		GND					R14	No			
		GND					R16	No			
		GND					R18	No			
		GND					R20	No			
		GND					R22	No			
		GND					P13	No			
		GND					P15	No			
		GND					P17	No			
		GND					P19	No			
		GND					P21	No			
		GND					P24	No			
		GND					P27	No			
		GND					P30	No			
		GND					P33	No			
		GND					N12	No			
		GND					N14	No			
		GND					N16	No			
		GND					N18	No			
		GND					N20	No			
		GND					N22	No			
		GND					M2	No			
		GND					M5	No			
		GND					M8	No			
		GND					M11	No			
		GND					M15	No			

Bank Number	VREF	Pin Name/ Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
		GND					M17	No			
		GND					M19	No			
		GND					M21	No			
		GND					L12	No			
		GND					L15	No			
		GND					L18	No			
		GND					L21	No			
		GND					L24	No			
		GND					L27	No			
		GND					L30	No			
		GND					L33	No			
		GND					J2	No			
		GND					J5	No			
		GND					J8	No			
		GND					H9	No			
		GND					H12	No			
		GND					H15	No			
		GND					H18	No			
		GND					H21	No			
		GND					H24	No			
		GND					H27	No			
		GND					H30	No			
		GND					H33	No			
		GND					F2	No			
		GND					F5	No			
		GND					E6	No			
		GND					E9	No			
		GND					E12	No			
		GND					E15	No			
		GND					E18	No			
		GND					E21	No			
		GND					E24	No			
		GND					E27	No			
		GND					E30	No			
		GND					E33	No			
		GND					C2	No			
		GND					B3	No			
		GND					B6	No			
		GND					B9	No			
		GND					B12	No			
		GND					B15	No			
		GND					B18	No			
		GND					B21	No			
		GND					B24	No			
		GND					B27	No			
		GND					B30	No			
		VCC					U17	No			
		VCC					AB14	No			
		VCC					AB22	No			
		VCC					AA13	No			
		VCC					AA15	No			
		VCC					AA17	No			
		VCC					AA19	No			
		VCC					AA21	No			
		VCC					Y14	No			
		VCC					Y16	No			
		VCC					Y18	No			
		VCC					Y20	No			
		VCC					W15	No			
		VCC					W17	No			

Bank Number	VREF	Pin Name/ Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
		VCC					W19	No			
		VCC					W21	No			
		VCC					V14	No			
		VCC					V16	No			
		VCC					V18	No			
		VCC					V20	No			
		VCC					U15	No			
		VCC					U19	No			
		VCC					U21	No			
		VCC					T14	No			
		VCC					T16	No			
		VCC					T18	No			
		VCC					T20	No			
		VCC					R15	No			
		VCC					R17	No			
		VCC					R19	No			
		VCC					R21	No			
		VCC					P14	No			
		VCC					P16	No			
		VCC					P18	No			
		VCC					P20	No			
		VCC					P22	No			
		VCC					N13	No			
		VCC					N21	No			
		VCC					N19	No			
		VCC					AB16	No			
		VCC					AB18	No			
		VCC					AB20	No			
		VCC					Y22	No			
		VCC					W13	No			
		VCC					V22	No			
		VCC					U13	No			
		VCC					T22	No			
		VCC					R13	No			
		VCC					N15	No			
		VCC					N17	No			
		VCCPT					U29	No			
		VCCPT					M25	No			
		VCCPT					AJ17	No			
		VCCPT					V6	No			
		VCCPT					AC10	No			
		VCCPT					F18	No			
		DNU					U18	No			
		VCCPGM					AD24	No			
		VCCPGM					AD10	No			
		TEMPDIODEn					D4	No			
		TEMPDIODEp					E5	No			
		VCC_CLKIN3C					AG18	No			
		VCC_CLKIN4C					AE17	No			
		VCC_CLKIN7C					H17	No			
		VCC_CLKIN8C					K18	No			
		VCCBAT					G6	No			
		VCCA_PLL_B1					AH18	No			
		VCCA_PLL_B2					AH17	No			
		VCCA_PLL_L2					U28	No			
		VCCA_PLL_L3					V28	No			
		VCCA_PLL_R2					U7	No			
		VCCA_PLL_R3					V7	No			
		VCCA_PLL_T1					G18	No			
		VCCA_PLL_T2					G17	No			

Bank Number	VREF	Pin Name/ Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
		VCCD_PLL_B1					AF18	No			
		VCCD_PLL_B2					AF17	No			
		VCCD_PLL_L2					U26	No			
		VCCD_PLL_L3					V26	No			
		VCCD_PLL_R2					U9	No			
		VCCD_PLL_R3					V9	No			
		VCCD_PLL_T1					J18	No			
		VCCD_PLL_T2					J17	No			
		VCCIO1A					B34	No			
		VCCIO1A					N28	No			
		VCCIO1A					L26	No			
		VCCIO1A					H29	No			
		VCCIO1A					G32	No			
		VCCIO1C					M32	No			
		VCCIO1C					V30	No			
		VCCIO1C					U34	No			
		VCCIO1C					T31	No			
		VCCIO2A					AB28	No			
		VCCIO2A					AN34	No			
		VCCIO2A					AH32	No			
		VCCIO2A					AG28	No			
		VCCIO2A					AD25	No			
		VCCIO2C					W25	No			
		VCCIO2C					AD32	No			
		VCCIO2C					W29	No			
		VCCIO2C					W32	No			
		VCCIO3A					AF25	No			
		VCCIO3A					AM27	No			
		VCCIO3A					AL30	No			
		VCCIO3A					AJ25	No			
		VCCIO3B					AF22	No			
		VCCIO3B					AM25	No			
		VCCIO3C					AH21	No			
		VCCIO3C					AM20	No			
		VCCIO3C					AJ18	No			
		VCCIO4A					AF12	No			
		VCCIO4A					AM3	No			
		VCCIO4A					AL6	No			
		VCCIO4A					AH10	No			
		VCCIO4B					AH13	No			
		VCCIO4B					AM10	No			
		VCCIO4C					AG16	No			
		VCCIO4C					AP17	No			
		VCCIO4C					AM13	No			
		VCCIO5A					AD9	No			
		VCCIO5A					AN1	No			
		VCCIO5A					AH3	No			
		VCCIO5A					AG6	No			
		VCCIO5A					AB7	No			
		VCCIO5C					W4	No			
		VCCIO5C					AC3	No			
		VCCIO5C					V1	No			
		VCCIO5C					U5	No			
		VCCIO6A					H7	No			
		VCCIO6A					N7	No			
		VCCIO6A					L10	No			
		VCCIO6A					G3	No			
		VCCIO6A					B1	No			
		VCCIO6C					T10	No			
		VCCIO6C					T3	No			

Bank Number	VREF	Pin Name/ Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
		VCCIO6C					T6	No			
		VCCIO6C					L3	No			
		VCCIO7A					F10	No			
		VCCIO7A					J10	No			
		VCCIO7A					D5	No			
		VCCIO7A					C8	No			
		VCCIO7B					C10	No			
		VCCIO7B					J13	No			
		VCCIO7C					C13	No			
		VCCIO7C					G14	No			
		VCCIO7C					F17	No			
		VCCIO8A					C32	No			
		VCCIO8A					J23	No			
		VCCIO8A					G25	No			
		VCCIO8A					D29	No			
		VCCIO8B					C25	No			
		VCCIO8B					G22	No			
		VCCIO8C					A18	No			
		VCCIO8C					H19	No			
		VCCIO8C					C22	No			
		VCCPD1A					N23	No			
		VCCPD1C					R23	No			
		VCCPD2A					AA23	No			
		VCCPD2C					W23	No			
		VCCPD3A					AC23	No			
		VCCPD3B					AC21	No			
		VCCPD3C					AC19	No			
		VCCPD4A					AC13	No			
		VCCPD4B					AC15	No			
		VCCPD4C					AC17	No			
		VCCPD5A					AB12	No			
		VCCPD5C					Y12	No			
		VCCPD6A					P12	No			
		VCCPD6C					T12	No			
		VCCPD7A					M12	No			
		VCCPD7B					M14	No			
		VCCPD7C					M16	No			
		VCCPD8A					M22	No			
		VCCPD8B					M20	No			
		VCCPD8C					M18	No			
1A	VREFB1AN0	VREFB1AN0	VREFB1AN0				J26	No			
1C	VREFB1CN0	VREFB1CN0	VREFB1CN0				P26	No			
2A	VREFB2AN0	VREFB2AN0	VREFB2AN0				AA26	No			
2C	VREFB2CN0	VREFB2CN0	VREFB2CN0				V27	No			
3A	VREFB3AN0	VREFB3AN0	VREFB3AN0				AG25	No			
3B	VREFB3BN0	VREFB3BN0	VREFB3BN0				AG22	No			
3C	VREFB3CN0	VREFB3CN0	VREFB3CN0				AH20	No			
4A	VREFB4AN0	VREFB4AN0	VREFB4AN0				AG10	No			
4B	VREFB4BN0	VREFB4BN0	VREFB4BN0				AG13	No			
4C	VREFB4CN0	VREFB4CN0	VREFB4CN0				AH16	No			
5A	VREFB5AN0	VREFB5AN0	VREFB5AN0				AF7	No			
5C	VREFB5CN0	VREFB5CN0	VREFB5CN0				AA9	No			
6A	VREFB6AN0	VREFB6AN0	VREFB6AN0				P9	No			
6C	VREFB6CN0	VREFB6CN0	VREFB6CN0				U8	No			
7A	VREFB7AN0	VREFB7AN0	VREFB7AN0				H10	No			
7B	VREFB7BN0	VREFB7BN0	VREFB7BN0				H13	No			
7C	VREFB7CN0	VREFB7CN0	VREFB7CN0				G15	No			
8A	VREFB8AN0	VREFB8AN0	VREFB8AN0				H25	No			
8B	VREFB8BN0	VREFB8BN0	VREFB8BN0				H22	No			
8C	VREFB8CN0	VREFB8CN0	VREFB8CN0				G19	No			

Bank Number	VREF	Pin Name/ Function	Optional Function(s)	Configuration Function	Dedicated Tx/Rx Channel	Emulated LVDS Output Channel	F1152	Dynamic OCT Support	DQS for X4 for F1152	DQS for X8/X9 for F1152	DQS for X16/X18 for F1152
		NC					D32	No			
		NC					AL31	No			
		NC					AH7	No			
		NC					G7	No			
		NC					AK30	No			
		NC					L11	No			
		NC					L25	No			
		NC					K26	No			
		VCCAUX					J27	No			
		VCCAUX					AG27	No			
		VCCAUX					AG7	No			
		VCCAUX					H8	No			

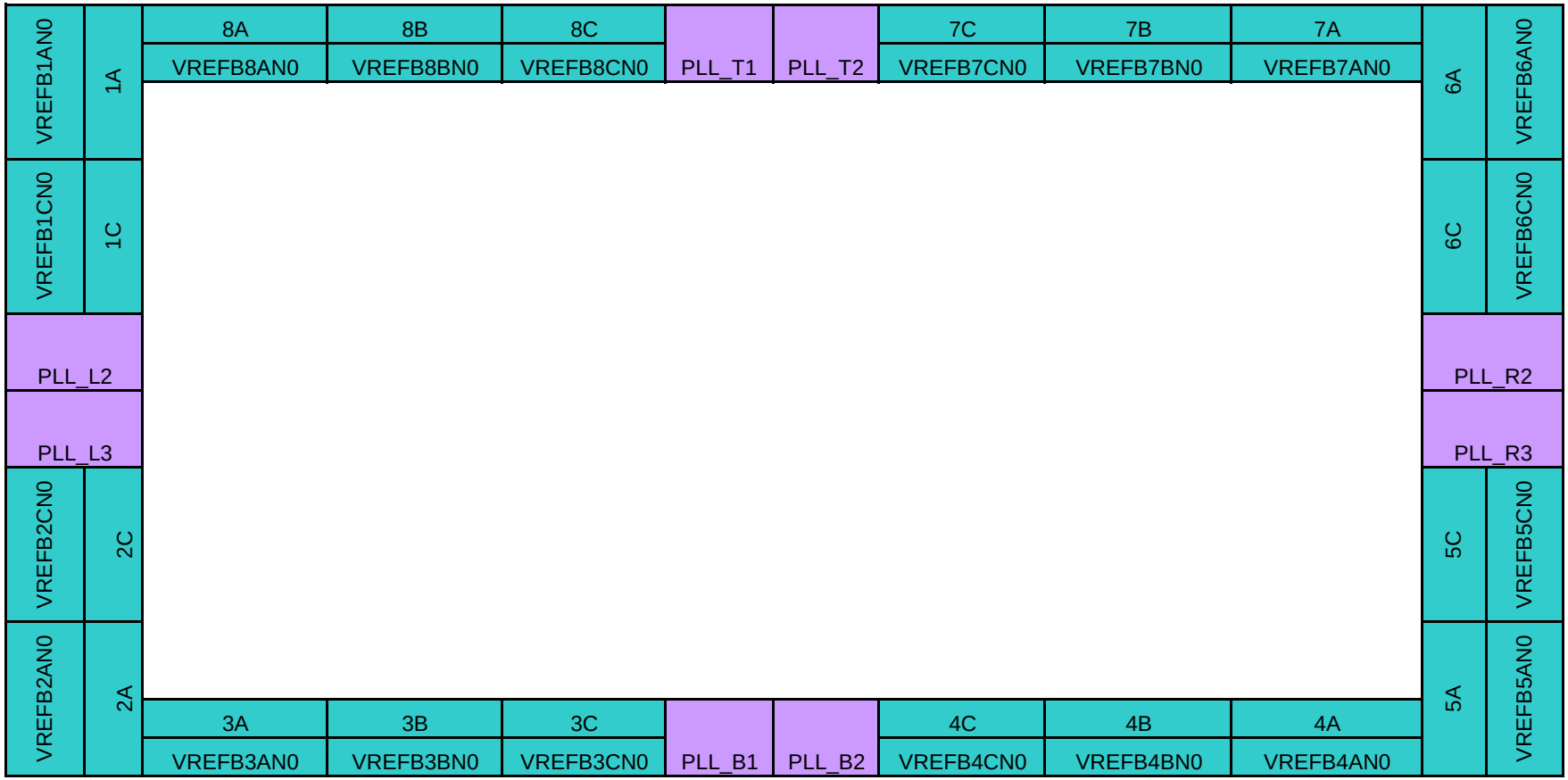
Pin Name	Pin Type (1st and 2nd Function)	Pin Description
		Clock and PLL Pins
CLK[1,3,8,10]p	Clock, Input	Dedicated high speed clock input pins 1, 3, 8, and 10 that can also be used for data inputs. OCT Rd is not supported on these pins.
CLK[1,3,8,10]n	Clock, Input	Dedicated negative clock input pins for differential clock input that can also be used for data inputs. OCT Rd is not supported on these pins.
CLK[0,2,9,11]p	I/O, Clock	These pins can be used as I/O pins or clock input pins. OCT Rd is supported on these pins.
CLK[0,2,9,11]n	I/O, Clock	These pins can be used as I/O pins or negative clock input pins for differential clock inputs. OCT Rd is supported on these pins.
CLK[4:7,12:15]p	I/O, Clock	These pins can be used as I/O pins or clock input pins. OCT Rd is not supported on these pins.
CLK[4:7,12:15]n	I/O, Clock	These pins can be used as I/O pins or negative clock input pins for differential clock inputs. OCT Rd is not supported on these pins.
PLL_[L1,L4,R1,R4]_CLKp	Clock, Input	Dedicated clock input pins to PLL L1, L4, R1, and R4 respectively.
PLL_[L1,L4,R1,R4]_CLKn	Clock, Input	Dedicated negative clock input pins for differential clock input to PLL L1, L4, R1, and R4 respectively.
PLL_[L1, L2, L3, L4]_CLKOUT0n PLL_[R1, R2, R3, R4]_CLKOUT0n	I/O, Clock	Each left and right PLL supports 2 clock I/O pins, configured either as 2 single ended I/O or one differential I/O pair. When using both pins as single ended I/Os, PLL_#_CLKOUT0n can be the clock output while the PLL_#_FB_CLKOUT0p is the external feedback input pin.
PLL_[L1, L2, L3, L4]_FB_CLKOUT0p PLL_[R1, R2, R3, R4]_FB_CLKOUT0p	I/O, Clock	
PLL_[T1,T2,B1,B2]_FBp/CLKOUT1	I/O, Clock	Dual purpose I/O pins that can be used as two single-ended outputs or one differential external feedback input pin.
PLL_[T1,T2,B1,B2]_FBn/CLKOUT2	I/O, Clock	
PLL_[T1,T2,B1,B2]_CLKOUT[3,4]	I/O, Clock	These pins can be used as I/O pins or two single-ended clock output pins.
PLL_[T1,T2,B1,B2]_CLKOUT0p	I/O, Clock	I/O pins that can be used as two single-ended clock output pins or one differential clock output pair.
PLL_[T1,T2,B1,B2]_CLKOUT0n	I/O, Clock	
		Dedicated Configuration/JTAG Pins
nIO_PULLUP	Input	Dedicated input that chooses whether the internal pull-ups on the user I/O pins and dual-purpose I/O pins (DATA[7..0], CLKUSR, INIT_DONE, DEV_OE, DEV_CLRn) are on or off before and during configuration. A logic high turns off the weak pull-up, while a logic low turns them on.
TEMPDIODEp	Input	Pin used in conjunction with the temperature sensing diode (bias-high input) inside the FPGA.
TEMPDIODEn	Input	Pin used in conjunction with the temperature sensing diode (bias-low input) inside the FPGA.
MSEL[0:2]	Input	Configuration input pins that set the FPGA device configuration scheme.
nCE	Input	Dedicated active-low chip enable. When nCE is low, the device is enabled. When nCE is high, the device is disabled.
nCONFIG	Input	Dedicated configuration control input. Pulling this pin low during user-mode will cause the FPGA to lose its configuration data, enter a reset state, and tri-state all I/O pins. Returning this pin to a logic high level will initiate reconfiguration.
CONF_DONE	Bidirectional (open-drain)	This is a dedicated configuration done pin. As a status output, the CONF_DONE pin drives low before and during configuration. Once all configuration data is received without error and the initialization cycle starts, CONF_DONE is released. As a status input, CONF_DONE goes high after all data is received. Then the device initializes and enters user mode. It is not available as a user I/O pin.
nCEO	Output	Output that drives low when device configuration is complete.
nSTATUS	Bidirectional (open-drain)	This is a dedicated configuration status pin. The FPGA drives nSTATUS low immediately after power-up and releases it after POR time. As a status output, the nSTATUS is pulled low if an error occurs during configuration. As a status input, the device enters an error state when nSTATUS is driven low by an external source during configuration or initialization. It is not available as a user I/O pin.
PORSEL	Input	Dedicated input which selects between a POR time of 12 ms or 100 ms. A logic high selects a POR time of 12 ms and a logic low selects POR time of 100 ms.
nCSO	Output	Dedicated output control signal from the FPGA to the serial configuration device in AS mode that enables the configuration device.
ASDO	Output	Control signal from the FPGA to the serial configuration device in AS mode used to read out configuration data.
DCLK	Input (PS, FPP) Output (AS)	Dedicated configuration clock pin. In PS and FPP configuration, DCLK is used to clock configuration data from an external source into the FPGA. In AS mode, DCLK is an output from the FPGA that provides timing for the configuration interface.
TCK	Input	Dedicated JTAG test clock input pin.
TMS	Input	Dedicated JTAG test mode select input pin.
TDI	Input	Dedicated JTAG test data input pin.
TDO	Output	Dedicated JTAG test data output pin.
TRST	Input	Dedicated active low JTAG test reset input pin. TRST is used to asynchronously reset the JTAG boundary-scan circuit.

Pin Name	Pin Type (1st and 2nd Function)	Pin Description
		Optional/Dual-Purpose Configuration Pins
CRC_ERROR	I/O, Output (open-drain)	Active high signal that indicates that the error detection circuit has detected errors in the configuration SRAM bits. This pin is optional and is used when the CRC error detection circuit is enabled.
DEV_CLRn	I/O, Input	Optional pin that allows designers to override all clears on all device registers. When this pin is driven low, all registers are cleared; when this pin is driven high (VCCPGM), all registers behave as programmed.
DEV_OE	I/O, Input	Optional pin that allows designers to override all tri-states on the device. When this pin is driven low, all I/O pins are tri-stated; when this pin is driven high (VCCPGM), all I/O pins behave as defined in the design.
DATA0	I/O, Input	Dual-purpose configuration data input pin. The DATA0 pin can be used for bit-wide configuration or as an I/O pin after configuration is complete.
DATA[1:7]	I/O, Input	Dual-purpose configuration input data pins. The DATA[0:7] pins can be used for byte-wide configuration or as regular I/O pins. These pins can also be used as user I/O pins after configuration.
INIT_DONE	I/O, Output (open-drain)	This is a dual-purpose pin and can be used as an I/O pin when not enabled as INIT_DONE. When enabled, a transition from low to high at the pin indicates when the device has entered user mode. If the INIT_DONE output is enabled, the INIT_DONE pin cannot be used as a user I/O pin after configuration.
CLKUSR	I/O, Input	Optional user-supplied clock input. Synchronizes the initialization of one or more devices. If this pin is not enabled for use as a user-supplied configuration clock, it can be used as a user I/O pin.
		Differential I/O Pins
DIFFIO_RX[##]p, DIFFIO_RX[##]n	I/O, RX channel	These are true LVDS receiver channels on side row and column I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFIO_TX[##]p, DIFFIO_TX[##]n	I/O, TX channel	These are true LVDS transmitter channels on side I/O banks. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
DIFFOUT_[##]p, DIFFOUT_[##]n	I/O, TX channel	These are emulated LVDS output channels. On column I/O banks, there are true LVDS input buffers but no true LVDS output buffers. However, all column user I/Os, including I/Os with true LVDS input buffers, can be configured as emulated LVDS output buffers. Pins with a "p" suffix carry the positive signal for the differential channel. Pins with an "n" suffix carry the negative signal for the differential channel. If not used for differential signaling, these pins are available as user I/O pins.
		External Memory Interface Pins
DQS[1:44][T,B], DQS[1:40][L,R]	I/O,DQS	Optional data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry. The shifted DQS signal can also drive to internal logic.
DQSn[1:44][T,B], DQSn[1:40][L,R]	I/O,DQSn	Optional complementary data strobe signal for use in external memory interfacing. These pins drive to dedicated DQS phase shift circuitry.
DQ[1:44][T,B], DQ[1:40][L,R]	I/O,DQ	Optional data signal for use in external memory interfacing. The order of the DQ bits within a designated DQ bus is not important; however, use caution when making pin assignments if you plan on migrating to a different memory interface that has a different DQ bus width. Analyze the available DQ pins across all pertinent DQS columns in the pin list.
CQ[1:44][T,B], CQ[1:40][L,R]	DQS	Optional data strobe signal for use in QDR II SRAM. These are the pins for echo clocks.
CQn[1:44][T,B], CQn[1:40][L,R]	DQS	Optional complementary data strobe signal for use in QDR II SRAM. These are the pins for echo clocks.
		Reference Pins
RUP[1:8]A, RUP[3,8]C	I/O, Input	Reference pins for I/O banks. The RUP pins share the same VCCIO with the I/O bank where they are located. The external precision resistor RUP must be connected to the designated RUP pin within the bank. If not required, this pin is a regular I/O pin.
RDN[1:8]A, RDN[3,8]C	I/O, Input	Reference pins for I/O banks. The RDN pins share the same GND with the I/O bank where they are located. The external precision resistor RDN must be connected to the designated RDN pin within the bank. If not required, this pin is a regular I/O pin.
DNU	Do Not Use	Do not connect to power or ground or any other signal; must be left floating.
NC	No Connect	Do not drive signals into these pins.
		Supply Pins
VCC	Power	VCC supplies power to the core and periphery.

Pin Name	Pin Type (1st and 2nd Function)	Pin Description
VCCD_PLL_[L,R][1:4], VCCD_PLL_[T,B][1:2]	Power	Digital power for PLL[L[1:4],R[1:4],T[1:2],B[1:2]]. The designer must connect these pins to the voltage level that recommended in data sheet, even if the PLL is not used.
VCCPT	Power	Power supply for the programmable power technology.
VCCA_PLL_[L,R][1:4], VCCA_PLL_[T,B][1:2]	Power	Analog power for PLL [L[1:4],R[1:4],T[1:2],B[1:2]]. The designer must connect these pins to the voltage level that recommended in data sheet, even if the PLL is not used. It is advised to keep this pin isolated from other VCC for better jitter performance.
VCCAUX	Power	Auxiliary supply for the programmable power technology.
VCCIO[1:8][A,B,C]	Power	These are I/O supply voltage pins for banks 1 through 8. Each bank can support a different voltage level. VCCIO supplies power to the output buffers for all LVDS, LVCMOS(1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V), HSTL(12, 15, 18), SSTL(15, 18, 2), 3.0 V PCI/PCI-X I/O as well as LVTTL 3.3 V I/O standards. VCCIO also supplies power to the input buffers used for LVCMOS(1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3 V), 3.0 V PCI/PCI-X and LVTTL 3.3 V I/O standards.
VCCPGM	Power	Configuration pins power supply.
VCCPD[1:8][A,B,C]	Power	Dedicated power pins. This supply is used to power the I/O pre-drivers.
VCC_CLKIN[3,4,7,8]C	Power	Differential clock input power supply for top and bottom I/O banks.
VCCBAT	Power	Battery back-up power supply for design security volatile key register.
GND	Ground	Device ground pins.
VREF[1:8][A,B,C]N0	Power	Input reference voltage for each I/O bank. If a bank uses a voltage-referenced I/O standard, then these pins are used as the voltage-reference pins for the bank.

Notes:

1. This pin definition is prepared based on the largest density, that is EP4SE820. Refer to pin list for the availability of the pins in each density.
2. Some of the pull-up /pull down resisitors mentioned in the table above may not be required, depending on the exact device configuration scheme.
The ability to NC or short them may be valuable during the debug phase, should you be required to use a different configuration scheme.
Refer to the Configuring Stratix IV E Devices chapter in the Stratix IV E Device Handbook for more information.
3. Refer to Pin Connections Guidelines and data sheet for the recommended operating voltage.



Note:

1. This is only a pictorial representation to provide an idea of placement on the device. Refer to the pin list and the Quartus® II software for exact locations.

Version Number	Date	Changes Made
1.0	7/10/2009	Initial Release.
1.1	12/3/2009	Added bank number for JTAG pins.
		Updated largest density in Note (1) of Pin Definitions.
		Updated DQS, DQSn, DQ, CQ, and CQn count in Pin Definitions.
		Grouped nCSO, ASDO, and DCLK into dedicated configuration/JTAG pins in Pin Definitions.
1.2	2/4/2015	Added the Dynamic OCT Support columns in Pin List F780 and Pin List F1152.