



# CRR Solver Accelerator for Financial Applications

## About the Solution

The CRR Solver performs COX-Ross-Rubinstein (CRR) binomial tree model for American option pricing. It models all the possible paths that might be followed by the underlying's price over the lifetime of an option. The solver has two versions, CRR without Greeks, which only computes the option prices, and CRR with Greeks, which computes the option prices as well as five finance Greeks: delta, gamma, theta, vega, and rho. The price of an option is the greater of:

1. The payoff from early exercise.
2. The payoff of the weighted average payoff from future exercises.

The formula to price an option in CRR is

$$f = \max(c1*f(d)+c2*f(u), x\text{-strike price})$$

where  $f$  is the payoff of an option,  $f(d)$  is the option payoff of a future down movement,  $f(u)$  is the option payoff of a future up movement,  $x$  is the current value of the underlying and strike is the strike price of the underlying. Coefficients  $c1$  is the probability of down movements,  $c2$  is the probability of up movement.

The algorithm is partitioned between CPU and FPGA with the bulk of computation intensive work being done on the FPGA. The CPU handles pre-processing and post-processing of data so that the FPGA can compute more efficiently and save precious board resources.

## Built to Scale with Intel FPGA Financial Libraries

Intel will be delivering over 250 library functions in 2019 enabling you to develop your own financial algorithms targeted for your implementation. This library includes a vast array of functions including statistics, linear algebra, and math primitives. To enable easy development of your algorithms with the financial library functions, we have built a platform with a full software stack to enable you to accelerate and orchestrate on FPGAs through OpenCL™. The CRR solver reference design leverages the orchestration capabilities of the software stack to deploy the CRR solver on four Intel® Programmable Acceleration Cards with Intel Arria® 10 GX FPGA on a single server.

### Authors

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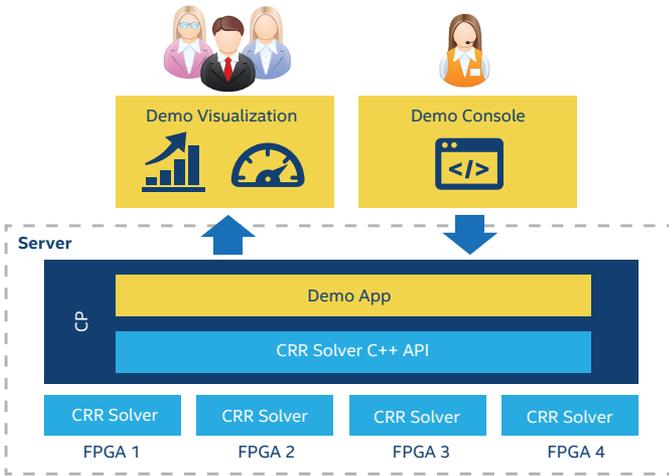


Figure 1. Data Center Orchestration Flow of Acceleration Platform



Figure 2. Actual Image of the Server Setup

### Delivering Performance

Figure 3 shows the type of performance you should expect to get with our mid-range Intel Arria 10 FPGAs. There is an estimated 4X performance improvement expected going to our high-end Intel Stratix® 10 FPGAs. Along with that, with the ability to orchestrate between multiple FPGAs the performance results show a linear improvement in performance as you scale. With this performance, the CPU utilization required the use of only one core, leaving the rest of the cores free to perform additional computations.

### Learn More

To learn more and get additional details on our libraries and reference designs, contact your local sales representative.

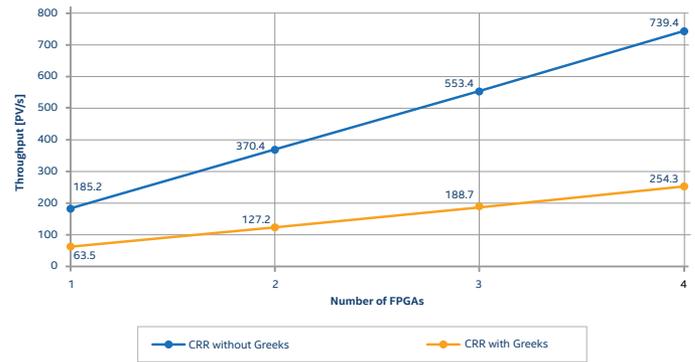
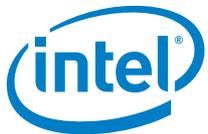


Figure 3. Linear Scalability for CRR Solver



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For more information go to [www.intel.com/benchmarks](http://www.intel.com/benchmarks).

Performance results are based on testing as of 7th October 2019 and may not reflect all publicly available security updates. See configuration disclosure for details. No product or component can be absolutely secure.

§ Configurations: The configuration is with 8191 time steps(input parameter), Intel Arria10 Programmable Acceleration Cards, tested on 7th October 2019 by Intel.

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