



Quadrature Solver Accelerator for Financial Applications

About the Solution

The quadrature solver performs numerical integration to compute the price of an option. Options are priced with the formula:

$$V_0 = E[\text{payoff}]$$

where V_0 is the expected return of the payoff function. This can be modeled as an integral that can be solved numerically via the quadrature method to price the option. The quadrature solver is a generalized integration of the lognormal using a modified version of Haselgrove's algorithm ("A Method for Numerical Integration", Haselgrove, 1960). Among the family of quadrature methods, Simpson's rule was chosen as the candidate due to its robustness and fast convergence rate of order $(n-4)$, where n is the number of intervals. The Quadrature solver integrates a payoff function to be used for option pricing. These functions are used on both the host and kernel. There are currently five payoff functions built into the accelerator which are multiplexed together and can be chosen via `func_sel` parameter. A user can implement their own payoff function by replacing the call to `fSpread` with a new function. Note that you must replace the payoff function on both the kernel and the host side. This is because the CPU pre-processing stage requires the payoff function and the CPU reference model requires it as well.

Built to Scale with Intel® FPGA Financial Libraries

Intel will be delivering over 250 library functions in 2019 enabling you to develop your own financial algorithms targeted for your implementation. This library includes a vast array of functions including statistics, linear algebra, and math primitives. To enable easy development of your algorithms with the financial library functions we have built a platform with a full software stack to enable you to accelerate and orchestrate on FPGAs through OpenCL™. The Quadrature solver reference design leverages the orchestration capabilities of the software stack to deploy the PDE solver on four Intel® Arria® 10 device programmable acceleration cards on a single server.

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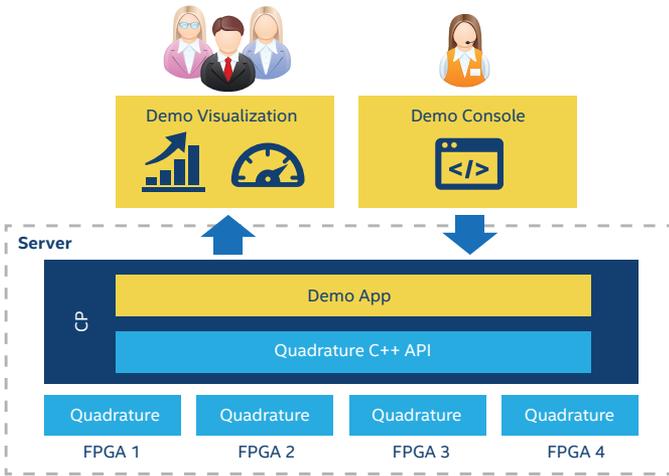


Figure 1. Data Center Orchestration Flow of Acceleration Platform

Figure 2. Actual Image of the Server Setup

Delivering Performance

Figure 3 shows the type of performance you should expect to get with our mid-range Intel Arria 10 FPGAs. There is an estimated 4X performance improvement expected going to our high-end Intel Stratix® 10 FPGAs†. Along with that, with the ability to orchestrate between multiple FPGAs the performance results show a linear improvement in performance as you scale. With this performance, the CPU utilization required the use of only one core, leaving the rest of the cores free to perform additional computations.

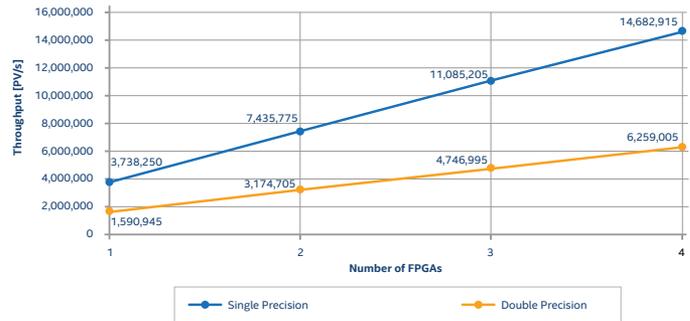


Figure 3. Linear Scalability of Quadrature Solver

Learn More

To learn more or get additional details on our libraries and reference designs, contact your local sales representative .



† Tests measure performance of components on a particular test, in specific systems. Differences in hardware, software, or configuration will affect actual performance. Consult other sources of information to evaluate performance as you consider your purchase. For more complete information about performance and benchmark results, visit www.intel.com/benchmarks.

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For more information go to www.intel.com/benchmarks.

Performance results are based on testing as of 7th October 2019 and may not reflect all publicly available security updates. See configuration disclosure for details. No product or component can be absolutely secure.

§ Configurations: The configuration is tested using a server with four Intel Arria10 Programmable Acceleration Cards, tested on 7th October 2019 by Intel.

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