

# 50G Interlaken MegaCore Function User Guide



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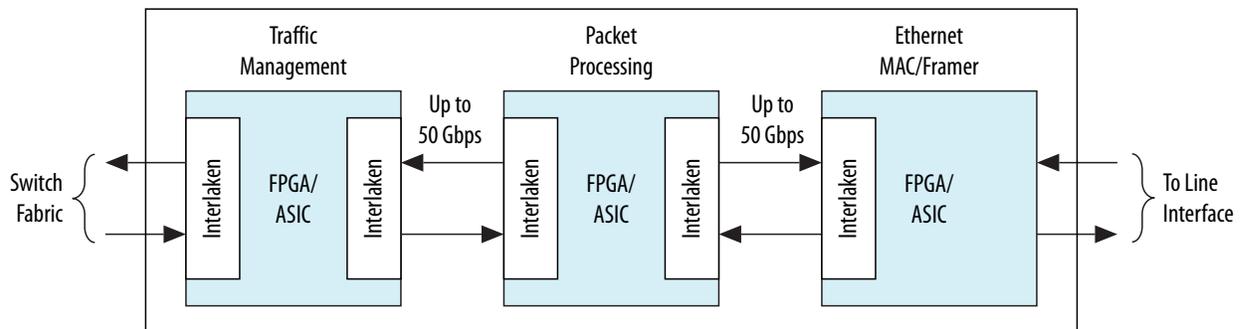


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Interlaken is a high-speed serial communication protocol for chip-to-chip packet transfers. The 50G Interlaken Intel® FPGA IP implements the *Interlaken Protocol Specification, Revision 1.2*. It supports eight lanes at a lane rate of 6.25 gigabits per second (Gbps), on Stratix® V, Arria® V GZ, and Intel Arria 10 devices, providing raw bandwidth of 50 Gbps.

Interlaken provides low I/O count compared to earlier protocols, supporting scalability in both number of lanes and lane speed. Other key features include flow control, low overhead framing, and extensive integrity checking. The 50G Interlaken IP core incorporates a physical coding sublayer (PCS), a physical media attachment (PMA), and a media access control (MAC) block.

**Figure 1-1: Typical Interlaken Application**



### Related Information

- [50G Interlaken IP core User Guide Archives](#) on page 11-1
- [Introduction to Altera IP Cores](#)  
Provides general information about all Intel FPGA IP cores, including parameterizing, generating, upgrading, and simulating IP cores.
- [Creating Version-Independent IP and Qsys Simulation Scripts](#)  
Create simulation scripts that do not require manual updates for software or IP version upgrades.
- [Project Management Best Practices](#)  
Guidelines for efficient management and portability of your project and IP files.
- [Interlaken Protocol Specification, Revision 1.2](#)

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- [50G Interlaken Example Design User Guide](#)  
A demonstration hardware example design is available for Intel Arria 10 IP core variations after you click **Generate Example Design**.

## Features

The 50G Interlaken IP core has the following features:

- Compliant with the *Interlaken Protocol Specification, Revision 1.2*.
- Supports eight serial lanes in configurations that provide up to 50 Gbps raw bandwidth.
- Supports per-lane data rate of 6.25 Gbps using Intel on-chip high-speed transceivers.
- Supports dynamically configurable BurstMax and BurstMin values.
- Supports Packet mode and Interleaved (Segmented) mode for user data transfer.
- Supports up to 256 logical channels in out-of-the-box configuration.
- Supports optional user-controlled in-band flow control with 1, 2, 4, 8, or 16 16-bit calendar pages.
- Supports optional out-of-band flow control blocks.

### Related Information

[Interlaken Protocol Specification, Revision 1.2](#)

## IP Core Supported Combinations of Number of Lanes and Data Rate

**Table 1-1: 50G Interlaken IP Core Supported Combinations of Number of Lanes and Data Rate**

The 50G Interlaken IP core supports only the following combination of number of lanes and data rate.

Number of Lanes	Lane Rate (Gbps)
8	6.25

## IP Core Raw Aggregate Bandwidth

The raw aggregate bandwidth of the 50G Interlaken IP core is  $8 \times 6.25 \text{ Gbps} = 50 \text{ Gbps}$ .

## Device Family Support

The following table lists the device support level definitions for Intel IP cores.

**Table 1-2: Intel FPGA IP Core Device Support Levels**

FPGA Device Families
<p><b>Preliminary support</b> — The core is verified with preliminary timing models for this device family. The IP core meets all functional requirements, but might still be undergoing timing analysis for the device family. It can be used in production designs with caution.</p>



## FPGA Device Families

**Final support** — The IP core is verified with final timing models for this device family. The IP core meets all functional and timing requirements for the device family and can be used in production designs.

The following table shows the level of support offered by the 50G Interlaken IP core for each Intel device family.

**Table 1-3: Intel FPGA IP Core Device Family Support**

Device Family	Support
Stratix V (GS, GT, and GX)	Final
Arria V (GZ)	Final
Intel Arria 10	Preliminary
Other device families	No support

## IP Core Verification

Before releasing a version of the 50G Interlaken IP core, Intel runs comprehensive regression tests in the current version of the Quartus® Prime software. These tests use standalone methods. These files are tested in simulation and hardware to confirm functionality. Intel tests and verifies the 50G Interlaken IP core in hardware for different platforms and environments.

Constrained random techniques generate appropriate stimulus for the functional verification of the IP core. Functional coverage metrics measure the quality of the random stimulus, and ensure that all important features are verified.

## Performance and Resource Utilization

**Table 1-4: 50G Interlaken MegaCore Function FPGA Resource Utilization**

The table shows results obtained using the Quartus II software v13.1 and v13.1 Arria 10 edition releases for the following devices:

- Arria 10 device 10AX115S2F45I2SGES
- Arria V GZ device 5AGZE1H2F35I3
- Stratix V GX device 5SGXMA7N2F45I3
- Stratix V GT device 5SGTMC7K3F40I2

The results in this table do not include the out-of-band flow control block.

The numbers of ALMs and logic registers are rounded up to the nearest 100. The numbers of ALMs, before rounding, are the **ALMs needed** numbers from the Quartus II Fitter Report.

Device	Resource Utilization			
	ALMs	Logic Registers		M20K Blocks
		Primary	Secondary	
Arria 10	9900	200020600	1500	17
Arria V GZ	9800	20800	1600	17
Stratix V GX	9800	20700	1700	17
Stratix V GT	9800	20700	1600	17

## Device Speed Grade Support

**Table 1-5: Minimum Recommended FPGA Fabric Speed Grades**

For each device family the 50G Interlaken IP core supports, Altera recommends that you configure the 50G Interlaken IP core only in the FPGA fabric speed grades listed in the table, and any faster (lower numbered) FPGA fabric speed grades that are available. Altera does not support configuration of this IP core in slower speed grades.

Device Family	Minimum Supported Speed Grade
Arria 10	I2, E2
Arria V GZ	I3, C3
Stratix V GX	I3, C3
Stratix V GT	I3, C3
Stratix V GS	I3, C3

### Related Information

- [Intel Arria 10 Device Datasheet](#)  
Provides information about Intel Arria 10 transceiver speed grades for specific operating conditions.
- [Stratix V Device Datasheet](#)  
Provides information about Stratix V transceiver speed grades for specific operating conditions.
- [Arria V Device Datasheet](#)  
Provides information about Arria V GZ transceiver speed grades for specific operating conditions.

## Release Information

Intel FPGA IP versions match the Intel Quartus Prime Design Suite software versions until v19.1. Starting in Intel Quartus Prime Design Suite software version 19.2, Intel FPGA IP has a new versioning scheme.

The Intel FPGA IP version (X.Y.Z) number can change with each Intel Quartus Prime software version. A change in:

- X indicates a major revision of the IP. If you update the Intel Quartus Prime software, you must regenerate the IP.
- Y indicates the IP includes new features. Regenerate your IP to include these new features.
- Z indicates the IP includes minor changes. Regenerate your IP to include these changes.

**Table 1-6: 50G Interlaken IP Core Current Release Information**

Item	Value
IP Version	19.2.0
Intel Quartus Prime Version	19.2
Release Date	2019.07.12
Ordering Code	IP-ILKN/50G
Vendor ID	6AF7
Product ID	010D

# Getting Started With the 50G Interlaken IP Core

# 2

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The following sections explain how to install, parameterize, simulate, and initialize the 50G Interlaken IP core.

[Installing and Licensing Intel FPGA IP Cores](#) on page 2-2

The Intel Quartus Prime software installation includes the Intel FPGA IP library. This library provides many useful IP cores for your production use without the need for an additional license. Some Intel FPGA IP cores require purchase of a separate license for production use. The Intel FPGA IP Evaluation Mode allows you to evaluate these licensed Intel FPGA IP cores in simulation and hardware, before deciding to purchase a full production IP core license. You only need to purchase a full production license for licensed Intel IP cores after you complete hardware testing and are ready to use the IP in production.

[Specifying the 50G Interlaken IP Core Parameters and Options](#) on page 2-5

The 50G Interlaken parameter editor allows you to quickly configure your custom IP variation. You specify IP core options and parameters in the Quartus Prime software.

[Files Generated for Arria V GZ and Stratix V Variations](#) on page 2-6

[Files Generated for Intel Arria 10 Variations](#) on page 2-7

[Simulating the 50G Interlaken IP Core](#) on page 2-8

[Integrating Your IP Core in Your Design](#) on page 2-8

[Compiling the Full Design and Programming the FPGA](#) on page 2-17

[Creating a Signal Tap Debug File to Match Your Design Hierarchy](#) on page 2-17

For Intel Arria 10 and Intel Cyclone® 10 GX devices, the Intel Quartus Prime software generates two files, `build_stp.tcl` and `<ip_core_name>.xml`. You can use these files to generate a Signal Tap file with probe points matching your design hierarchy.

## Related Information

- [Introduction to Altera IP Cores](#)  
Provides general information about all Intel FPGA IP cores, including parameterizing, generating, upgrading, and simulating IP cores.
- [Creating Version-Independent IP and Qsys Simulation Scripts](#)  
Create simulation scripts that do not require manual updates for software or IP version upgrades.
- [Project Management Best Practices](#)  
Guidelines for efficient management and portability of your project and IP files.

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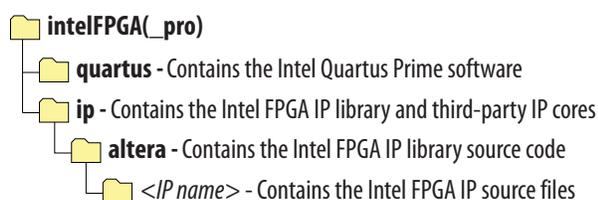
- **50G Interlaken Example Design User Guide**  
A demonstration hardware example design is available for Intel Arria 10 IP core variations after you click **Generate Example Design**.

## Installing and Licensing Intel FPGA IP Cores

The Intel Quartus Prime software installation includes the Intel FPGA IP library. This library provides many useful IP cores for your production use without the need for an additional license. Some Intel FPGA IP cores require purchase of a separate license for production use. The Intel FPGA IP Evaluation Mode allows you to evaluate these licensed Intel FPGA IP cores in simulation and hardware, before deciding to purchase a full production IP core license. You only need to purchase a full production license for licensed Intel IP cores after you complete hardware testing and are ready to use the IP in production.

The Intel Quartus Prime software installs IP cores in the following locations by default:

**Figure 2-1: IP Core Installation Path**



**Table 2-1: IP Core Installation Locations**

Location	Software	Platform
<drive>:\intelFPGA_pro\quartus\ip\altera	Intel Quartus Prime Pro Edition	Windows*
<drive>:\intelFPGA\quartus\ip\altera	Intel Quartus Prime Standard Edition	Windows
<home directory>:\intelFPGA_pro\quartus\ip\altera	Intel Quartus Prime Pro Edition	Linux*
<home directory>:\intelFPGA\quartus\ip\altera	Intel Quartus Prime Standard Edition	Linux

**Note:** The Intel Quartus Prime software does not support spaces in the installation path.

### Intel FPGA IP Evaluation Mode

The free Intel FPGA IP Evaluation Mode allows you to evaluate licensed Intel FPGA IP cores in simulation and hardware before purchase. Intel FPGA IP Evaluation Mode supports the following evaluations without additional license:

- Simulate the behavior of a licensed Intel FPGA IP core in your system.
- Verify the functionality, size, and speed of the IP core quickly and easily.
- Generate time-limited device programming files for designs that include IP cores.
- Program a device with your IP core and verify your design in hardware.

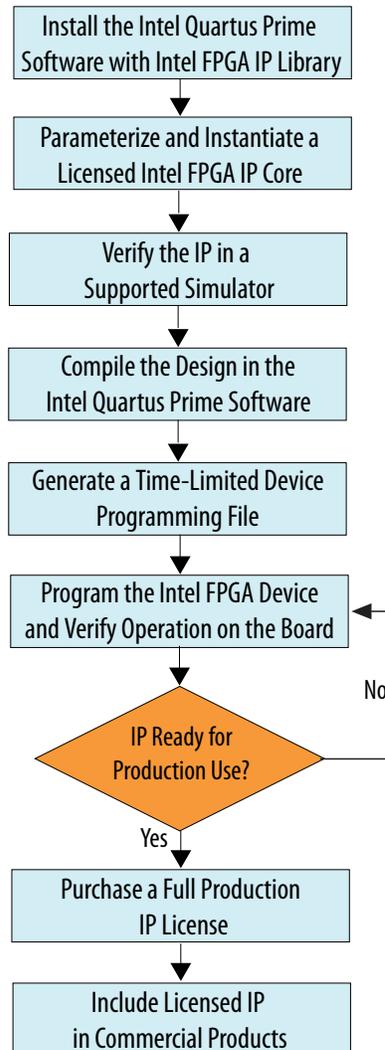
Intel FPGA IP Evaluation Mode supports the following operation modes:

- **Tethered**—Allows running the design containing the licensed Intel FPGA IP indefinitely with a connection between your board and the host computer. Tethered mode requires a serial joint test action group (JTAG) cable connected between the JTAG port on your board and the host computer, which is running the Intel Quartus Prime Programmer for the duration of the hardware evaluation period. The Programmer only requires a minimum installation of the Intel Quartus Prime software, and requires no Intel Quartus Prime license. The host computer controls the evaluation time by sending a periodic signal to the device via the JTAG port. If all licensed IP cores in the design support tethered mode, the evaluation time runs until any IP core evaluation expires. If all of the IP cores support unlimited evaluation time, the device does not time-out.
- **Untethered**—Allows running the design containing the licensed IP for a limited time. The IP core reverts to untethered mode if the device disconnects from the host computer running the Intel Quartus Prime software. The IP core also reverts to untethered mode if any other licensed IP core in the design does not support tethered mode.

When the evaluation time expires for any licensed Intel FPGA IP in the design, the design stops functioning. All IP cores that use the Intel FPGA IP Evaluation Mode time out simultaneously when any IP core in the design times out. When the evaluation time expires, you must reprogram the FPGA device before continuing hardware verification. To extend use of the IP core for production, purchase a full production license for the IP core.

You must purchase the license and generate a full production license key before you can generate an unrestricted device programming file. During Intel FPGA IP Evaluation Mode, the Compiler only generates a time-limited device programming file (*<project name>\_time\_limited.sof*) that expires at the time limit.

Figure 2-2: Intel FPGA IP Evaluation Mode Flow



**Note:** Refer to each IP core's user guide for parameterization steps and implementation details.

Intel licenses IP cores on a per-seat, perpetual basis. The license fee includes first-year maintenance and support. You must renew the maintenance contract to receive updates, bug fixes, and technical support beyond the first year. You must purchase a full production license for Intel FPGA IP cores that require a production license, before generating programming files that you may use for an unlimited time. During Intel FPGA IP Evaluation Mode, the Compiler only generates a time-limited device programming file (`<project name>_time_limited.sof`) that expires at the time limit. To obtain your production license keys, visit the [Self-Service Licensing Center](#).

The [Intel FPGA Software License Agreements](#) govern the installation and use of licensed IP cores, the Intel Quartus Prime design software, and all unlicensed IP cores.

#### Related Information

- [Intel FPGA Licensing Support Center](#)
- [Introduction to Intel FPGA Software Installation and Licensing](#)

## Specifying the 50G Interlaken IP Core Parameters and Options

The 50G Interlaken parameter editor allows you to quickly configure your custom IP variation. You specify IP core options and parameters in the Quartus Prime software.

The 50G Interlaken IP core is not supported in Platform Designer (Standard). You must use the IP Catalog accessible from the Quartus Prime **Tools** menu.

The 50G Interlaken IP core does not support VHDL simulation models. Intel recommends that you specify the Verilog HDL for both synthesis and simulation models.

1. In the IP Catalog (**Tools > IP Catalog**), locate and double-click the name of the IP core to customize. The parameter editor appears.
2. Specify a top-level name for your custom IP variation. The parameter editor saves the IP variation settings in a file named `<your_ip>.qsys`. Click **OK**.

**Note:** For Arria V GZ and Stratix V variations, you are prompted to specify an IP variation file type. To generate the demonstration testbench and example design, you must select the **Verilog** HDL and specify the Verilog file extension (`.v`).

3. Specify the parameters and options for your IP variation in the parameter editor, including one or more of the following. Refer to [50G Interlaken IP Core Parameter Settings](#) for information about specific IP core parameters.
  - Specify parameters defining the IP core functionality, port configurations, and device-specific features.
  - Specify options for processing the IP core files in other EDA tools.
4. For Intel Arria 10 variations, follow these steps:
  - a. Click **Generate HDL**. The **Generation** dialog box appears.
  - b. Specify output file generation options, and then click **Generate**. The IP variation files generate according to your specifications.

**Note:** To generate the demonstration testbench and example design, you must specify Verilog HDL for both synthesis and simulation models.
  - c. Optionally, click the **Generate Example Design** button in the parameter editor to generate a testbench and a hardware example design that targets the Intel Arria 10 Transceiver Signal Integrity Development Kit.
  - d. Click **Finish**. The parameter editor adds the top-level `.qsys` file to the current project automatically. If you are prompted to manually add the `.qsys` file to the project, click **Project > Add/Remove Files in Project** to add the file.
5. For Arria V GZ and Stratix V variations, follow these steps:
  - a. Click **Finish**. The **Generation** dialog box appears.
  - b. If you want to generate a demonstration testbench and example design for your IP core variation, turn on **Generate example design**.
  - c. Click **Generate**.
  - d. Click **Exit**. The parameter editor adds the top-level `.qsys` file to the current project automatically. If you are prompted to manually add the `.qsys` file to the project, click **Project > Add/Remove Files in Project** to add the file.
6. After generating and instantiating your IP variation, make appropriate pin assignments to connect ports.

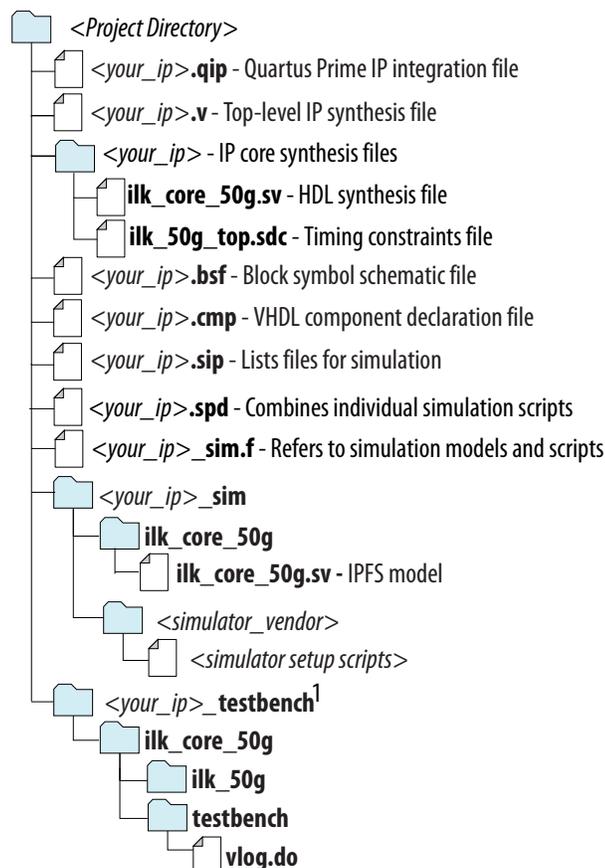
**Related Information**

- [50G Interlaken IP Core Parameter Settings](#) on page 3-1  
Details about the parameters available in the 50G Interlaken parameter editor.
- [Intel Arria 10 GX Transceiver Signal Integrity Development Kit product page](#)

## Files Generated for Arria V GZ and Stratix V Variations

The Quartus Prime software generates multiple files during generation of your 50G Interlaken IP core Arria V GZ or Stratix V variation.

**Figure 2-3: IP Core Generated Files**

**Notes:**

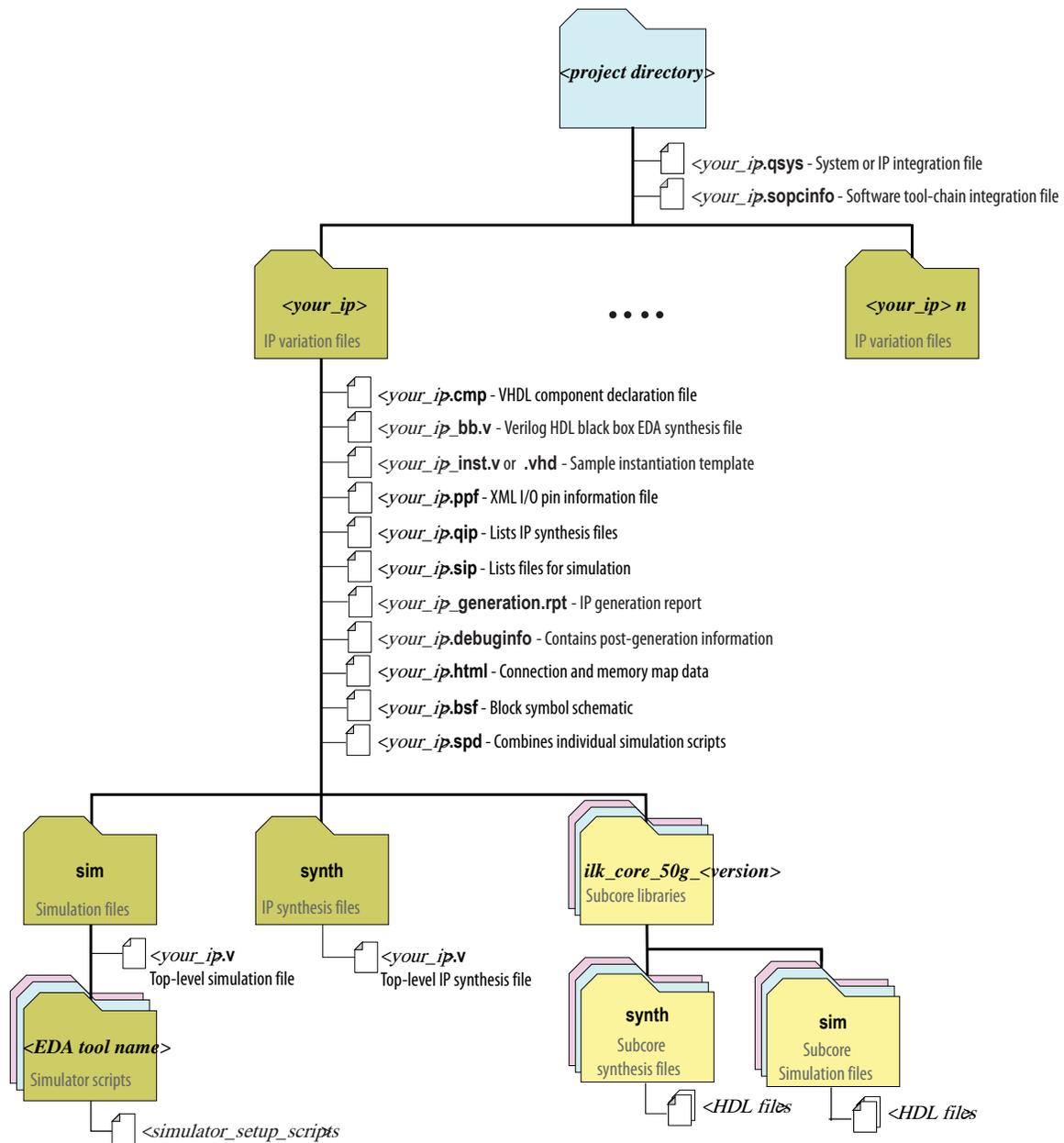
1. If example design is generated

For 50G Interlaken IP cores that target a non-Intel Arria 10 device, if you select the Verilog HDL for synthesis and simulation models and turn on **Generate example design**, the demonstration testbench and example design files are located in <your\_ip>\_testbench/ilk\_core\_50g/testbench.

## Files Generated for Intel Arria 10 Variations

The Quartus Prime software generates multiple files during generation of your 50G Interlaken IP core Intel Arria 10 variation.

Figure 2-4: IP Core Generated Files



In the Quartus Prime software v15.1 release, generating a 50G Interlaken IP core that targets an Intel Arria 10 device does not generate a demonstration testbench. To generate the Verilog HDL testbench and example design files in this release, you must click the **Generate Example Design** button in the

50G Interlaken parameter editor. When you do so, you are prompted to specify the location of the Verilog HDL demonstration testbench and example design files.

## Simulating the 50G Interlaken IP Core

You can simulate your 50G Interlaken IP core variation using any of the vendor-specific IEEE encrypted functional simulation models which are generated in the new `<instance name>_sim` or `<instance name>/sim` subdirectory of your project directory.

The 50G Interlaken IP core supports the Synopsys VCS, Cadence NC Sim, and Mentor Graphics Modelsim-SE simulators.

The 50G Interlaken IP core generates only a Verilog HDL simulation model and testbench. The IP core parameter editor appears to offer you the option of generating a VHDL simulation model, but this IP core does not support a VHDL simulation model or testbench.

For more information about functional simulation models for Intel IP cores, refer to the *Simulating Intel Designs* chapter in volume 3 of the *Quartus Prime Handbook*.

For non-Intel Arria 10 variations with Verilog HDL models, if you turn on **Generate example design** when you generate the IP core, the Quartus Prime software generates a testbench. This testbench demonstrates the resetting, clocking, and toggling of the 50G Interlaken IP core user interfaces in simulation. For Intel Arria 10 variations, you can generate both this testbench and a hardware example design by clicking **Generate Example Design** in the 50G Interlaken parameter editor.

### Related Information

- [50G Interlaken Example Design User Guide](#)  
A demonstration hardware example design is available for Intel Arria 10 IP core variations after you click **Generate Example Design**.
- [Simulating Intel Designs](#)

## Integrating Your IP Core in Your Design

After you generate your 50G Interlaken IP core variation, you can instantiate it in the RTL for your design. When you integrate your IP core instance in your design, you must pay attention to the following items.

### Pin Assignments

When you integrate your 50G Interlaken IP core instance in your design, you must make appropriate pin assignments. You do not need to specify pin assignments for simulation. However, you should make the pin assignments before you compile, to provide direction to the Quartus Prime Fitter and to specify the signals that should be assigned to device pins.

You can create a virtual pin to avoid making specific pin assignments for top-level signals while you are simulating and not ready to map the design to hardware. Do not create virtual pins for clock or Interlaken link data signals.

For the Intel Arria 10 device family, you must configure a PLL external to the 50G Interlaken IP core. The required number of PLLs depends on the distribution of your Interlaken lane data pins in the different A10 transceiver blocks.

**Related Information**

- [Adding the External PLL](#) on page 2-15
- [Quartus Prime Help](#)  
For information about the Quartus Prime software, including virtual pins.

## Transceiver Logical Channel Numbering

In Arria V and Stratix V devices, logical channel numbering starts from zero. The logical channel numbering starts at the bottom of the die with logical channel 0 and continues in physical pin order through the four ordered transceiver blocks on the same side of the device. Each data channel and TX PLL has its own dedicated reconfiguration interface with an assigned logical channel.

In Intel Arria 10 devices, you control the mapping of Interlaken lanes directly in the Intel Arria 10 Native PHY IP core that is included in the 50G Interlaken IP core.

In Arria V and Stratix V devices, you can control the logical channel assignments in the IP core. You typically assign lanes to match the logical channel numbering. However, the default Interlaken lane assignment does not assign a lane to Channel 1 or Channel 4 in a transceiver block, leaving either available for the CMU PLL. You can use the information in the following table to map the lanes to their default logical channel numbering. The logical channel numbering always starts at the bottom of a transceiver block.

**Table 2-2: Transceiver Logical Channel Numbering**

The default expected mapping of logical channels to Interlaken lanes in Arria V and Stratix V devices.

Transceiver Block Number	Logical Channel Number in Device	Direction	Interlaken Lane Number in IP Core
	27	TX PLL 3	

Transceiver Block Number	Logical Channel Number in Device	Direction	Interlaken Lane Number in IP Core	
3	26	TX		
		RX		
	25	TX		
		RX		
	24	TX		
		RX		
	23	TX		
		RX		
	22	TX		
		RX		
	21	TX		
		RX		
		20	TX PLL 2	

Transceiver Block Number	Logical Channel Number in Device	Direction	Interlaken Lane Number in IP Core	
2	19	TX		
		RX		
	18	TX		
		RX		
	17	TX		
		RX		
	16	TX		
		RX		
	15	TX		
		RX		
	14	TX		
		RX		
		13	TX PLL 1	

Transceiver Block Number	Logical Channel Number in Device	Direction	Interlaken Lane Number in IP Core	
1	12	TX	7	
		RX		
	11	TX	(Left available for CMU PLL)	
		RX		
	10	TX	6	
		RX		
	9	TX	5	
		RX		
	8	TX	(Left available for CMU PLL)	
		RX		
	7	TX	4	
		RX		
		6	TX PLL 0	

Transceiver Block Number	Logical Channel Number in Device	Direction	Interlaken Lane Number in IP Core
0	5	TX	3
		RX	
	4	TX	(Left available for CMU PLL)
		RX	
	3	TX	2
		RX	
	2	TX	1
		RX	
	1	TX	(Left available for CMU PLL)
		RX	
	0	TX	0
		RX	

For example, in an Arria V or Stratix V device, to change the VOD setting for lane 7, you write logical channel 12 to the Reconfiguration Controller.

**Related Information**

- [Lane Profile](#) on page 8-4  
Describes how to modify the logical channel mapping. Use this option with caution.
- [Intel Transceiver PHY IP User Guide](#)  
Background information to better understand logical channel numbering.

**Adding the Reconfiguration Controller**

50G Interlaken IP core variations that target an Arria V or a Stratix V device require an external reconfiguration controller to function correctly in hardware. 50G Interlaken IP core variations that target an Arria 10 device include a reconfiguration controller block and do not require an external reconfiguration controller.

Keeping the Reconfiguration Controller external to the IP core in Arria V and Stratix V devices provides the flexibility to share the Reconfiguration Controller among multiple IP cores and to accommodate FPGA transceiver layouts based on the usage model of your application. In Intel Arria 10 devices, you can

configure individual transceiver channels flexibly through an Avalon-MM Intel Arria 10 transceiver reconfiguration interface.

The following simple instructions show you how to instantiate an Intel Transceiver Reconfiguration Controller and how to connect the design blocks:

## Generating the Reconfiguration Controller

You can use the IP Catalog to generate an Intel Transceiver Reconfiguration Controller.

In the Transceiver Reconfiguration Controller parameter editor, you select the features of the transceiver that can be dynamically reconfigured. However, you must ensure that the following two features are turned on:

1. **Enable PLL calibration**
2. **Enable Analog controls**

You must also set the value of the **Number of reconfiguration interfaces** parameter. Each TX PLL requires its own reconfiguration interface, whether or not you intend to reconfigure it. The following formula determines the correct number of reconfiguration interfaces:

$$\text{NUMBER\_OF\_RECONFIGURATION\_INTERFACES} = \text{NUMBER\_OF\_LANES} + \text{NUMBER\_OF\_TX\_PLLs}$$

where

- `NUMBER_OF_LANES` is the total number of physical lanes used in your implemented design.
- `NUMBER_OF_TX_PLLs` is the total number of transceiver blocks (number of TX PLLs) used in your design.

For example, for a design that includes an Interlaken variation that is configured in two transceiver blocks, you must set **Number of reconfiguration interfaces** to the value of 10.

## Connecting the Reconfiguration Controller to the IP Core

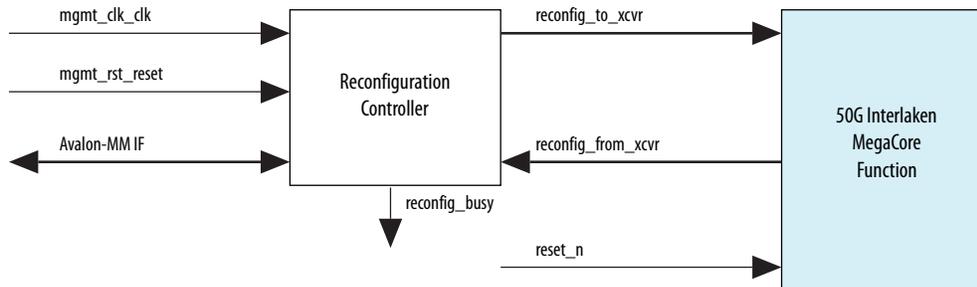
The Reconfiguration Controller communicates with the 50G Interlaken IP core on two busses:

- `reconfig_to_xcvr` (output)
- `reconfig_from_xcvr` (input)

Each of these busses connects to the bus of the same name in the 50G Interlaken IP core.

You must also connect the following signals:

- `mgmt_clk_clk`: Reconfiguration Controller clock (input)
- `mgmt_rst_reset`: Reconfiguration Controller reset (input)
- `reconfig_busy`: Reconfiguration Controller busy indication (output)

**Figure 2-5: Typical Connection of Reconfiguration Controller to 50G Interlaken IP Core**

Intel recommends that you set the Reconfiguration Controller input clock frequency in the range of 100 MHz to 125 MHz. Refer to the *Intel Transceiver PHY IP Core User Guide* for frequency range requirements specific to the device family.

The Reconfiguration Controller reset input should be asserted high during power up and remain asserted until its clock input becomes stable with the `mgmt_clk_locked` signal indicating a locked condition of the clock. Upon power up, the Reconfiguration Controller asserts `reconfig_busy` output high. The `reconfig_busy` signal remains asserted until the Reconfiguration Controller completes the configuration of all transceivers.

#### Related Information

[Intel Transceiver PHY IP Core User Guide](#)

## Adding the External PLL

50G Interlaken IP core variations that target an Arria 10 device require an external transceiver PLL to function correctly in hardware. 50G Interlaken IP core variations that target an Arria V or Stratix V device include the transceiver PLLs and do not require that you configure any additional PLLs.

You can use the IP Catalog to generate an external PLL IP core that configures a TX PLL on the device.

- Select **Intel Arria 10 Transceiver ATX PLL**, **Intel Arria 10 Transceiver CMU PLL**, or **Intel Arria 10 FPLL**.
- In the parameter editor, set the following parameter values:
  - **PLL output frequency** to one half the per-lane data rate of the IP core variation. The transceiver performs dual edge clocking, using both the rising and falling edges of the input clock from the PLL. Therefore, this PLL output frequency setting drives the transceiver with the correct clock for the Interlaken lanes.
  - **PLL reference clock frequency** to a frequency at which you can drive the TX PLL input reference clock. You must drive the external PLL reference clock input signal at the frequency you specify for this parameter.

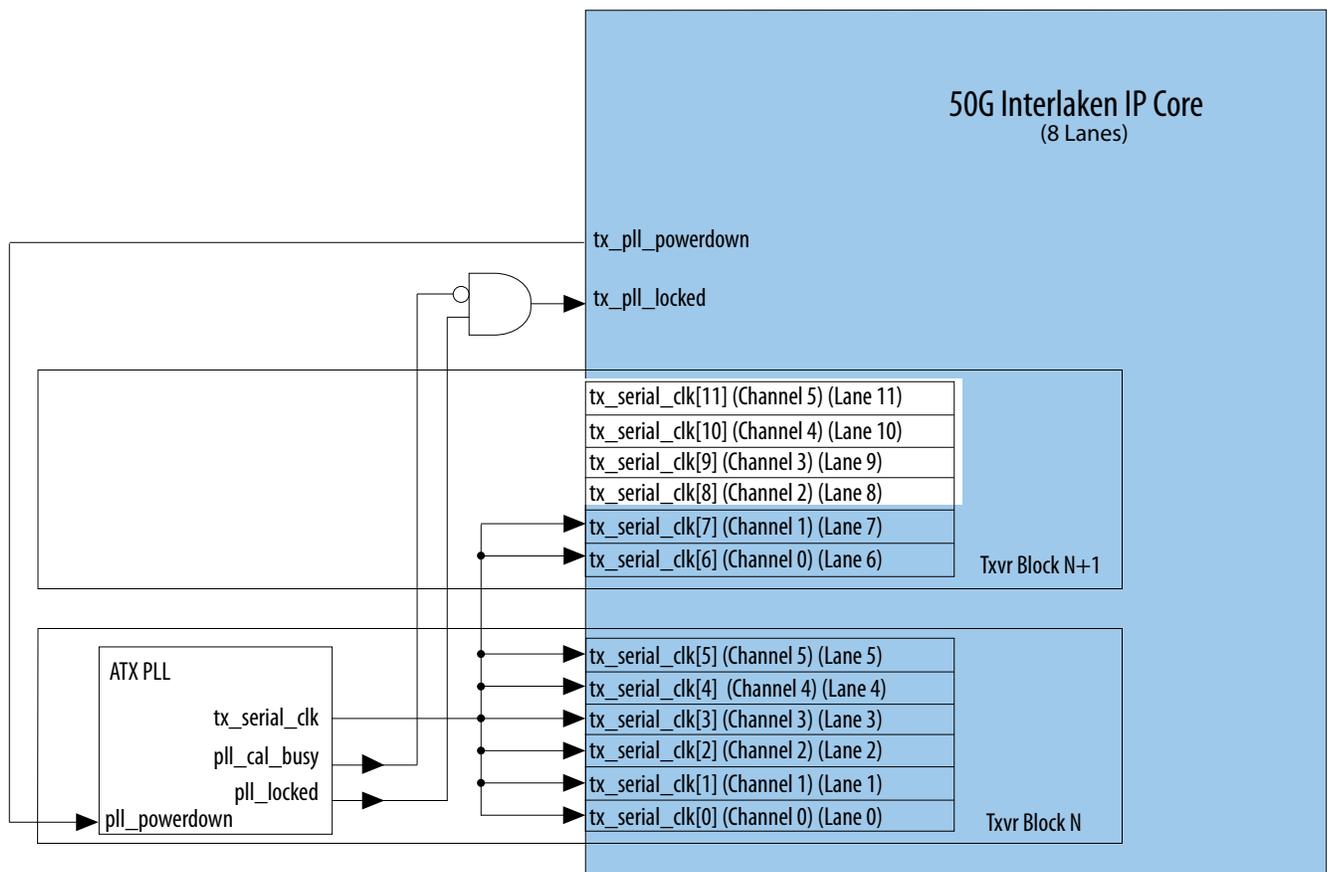
The number of external PLLs you must define depends on the distribution of your Interlaken TX serial lines across physical transceiver channels. You specify the clock network to which each PLL output connects by setting the clock network in the PLL parameter editor.

You must connect the external PLL signals and the Intel Arria 10 50G Interlaken IP core transceiver Tx PLL interface signals according to the following rules:

- Connect the `tx_serial_clk` input pin for each Interlaken lane to the output port of the same name in the corresponding external PLL.
- Connect the `tx_pll_locked` input pin of the 50G Interlaken IP core to the logical AND of the `pll_locked` output signals of the external PLLs for all of the Interlaken lanes and the inverse of each of the `pll_cal_busy` signals from the external PLLs.
- Connect the `tx_pll_powerdown` output pin of the 50G Interlaken IP core to the `pll_powerdown` reset pin of the external PLLs for all of the Interlaken lanes.

User logic must provide the AND function and connections. The following figure provides an example of one correct method, among many, to implement connection logic. You can also refer to the example design for example working user logic including one correct method to instantiate and connect an external PLL.

**Figure 2-6: Example Connection of ATX PLL with 50G Interlaken IP Core Using Intel Arria 10 xN Clock Network**



#### Related Information

- [Intel Arria 10 External PLL Interface](#) on page 4-3
- [Pin Assignments](#) on page 2-8

- [Intel Arria 10 External PLL Interface Signals](#) on page 5-15
- [Intel Arria 10 Transceiver PHY User Guide](#)  
Information about the correspondence between PLLs and transceiver channels, and information about how to configure an external PLL for your own design. You specify the clock network to which the PLL output connects by setting the clock network in the PLL parameter editor.

## Compiling the Full Design and Programming the FPGA

You can use the **Start Compilation** command on the Processing menu in the Quartus Prime software to compile your design. After successfully compiling your design, program the targeted Intel device with the Programmer and verify the design in hardware.

### Related Information

- [Incremental Compilation for Hierarchical and Team-Based Design](#)
- [Programming Intel Devices](#)

## Creating a Signal Tap Debug File to Match Your Design Hierarchy

For Intel Arria 10 and Intel Cyclone® 10 GX devices, the Intel Quartus Prime software generates two files, `build_stp.tcl` and `<ip_core_name>.xml`. You can use these files to generate a Signal Tap file with probe points matching your design hierarchy.

The Intel Quartus Prime software stores these files in the `<IP core directory>/synth/debug/stp/` directory.

### Before you begin

Synthesize your design using the Intel Quartus Prime software.

1. To open the Tcl console, click **View > Utility Windows > Tcl Console**.
2. Type the following command in the Tcl console:  

```
source <IP core directory>/synth/debug/stp/build_stp.tcl
```
3. To generate the STP file, type the following command:  

```
main -stp_file <output stp file name>.stp -xml_file <input xml_file name>.xml -mode build
```
4. To add this Signal Tap file (`.stp`) to your project, select **Project > Add/Remove Files in Project**. Then, compile your design.
5. To program the FPGA, click **Tools > Programmer**.
6. To start the Signal Tap Logic Analyzer, click **Quartus Prime > Tools > Signal Tap Logic Analyzer**.  
The software generation script may not assign the Signal Tap acquisition clock in `<output stp file name>.stp`. Consequently, the Intel Quartus Prime software automatically creates a clock pin called `auto_stp_external_clock`. You may need to manually substitute the appropriate clock signal as the Signal Tap sampling clock for each STP instance.
7. Recompile your design.
8. To observe the state of your IP core, click **Run Analysis**.

You may see signals or Signal Tap instances that are red, indicating they are not available in your design. In most cases, you can safely ignore these signals and instances. They are present because software generates wider buses and some instances that your design does not include.

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You customize the 50G Interlaken IP core by specifying parameters in the 50G Interlaken parameter editor, which you access from the Quartus Prime IP Catalog.

This chapter describes the parameters and how they affect the behavior of the IP core. To customize your 50G Interlaken IP core, you can modify parameters to specify the following properties:

[Meta Frame Length in Words](#) on page 3-1

[Enable Native PHY Debug Master Endpoint \(NPDME\)](#) on page 3-1

[Transceiver Reference Clock Frequency](#) on page 3-2

[Number of Calendar Pages](#) on page 3-2

[TX Scrambler Seed](#) on page 3-3

[Transfer Mode Selection](#) on page 3-3

## Meta Frame Length in Words

The **Meta frame length in words** parameter specifies the length of the meta frame, in 64-bit (8-byte) words. In the Interlaken specification, this parameter is called the **MetaFrameLength** parameter.

Smaller values for this parameter shorten the time to achieve lock. Larger values reduce overhead while transferring data, after lock is achieved.

For simulation, you can set the **Meta frame length in words** parameter to the value of 128 for fast lane locking. For hardware testing, Intel recommends that you set the **Meta frame length in words** parameter to the value of 2048.

The default value of the **Meta frame length in words** parameter is 2048.

## Enable Native PHY Debug Master Endpoint (NPDME)

The **Enable Native PHY Debug Master Endpoint (NPDME)** parameter specifies whether your Intel Arria 10 50G Interlaken IP core variation supports the ADME feature.

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This parameter exposes debugging features of the Intel Arria 10 Native PHY IP core that specifies the transceiver settings in the 50G Interlaken IP core. You can turn this parameter on to enable the following Intel Arria 10 Native PHY IP core features:

- **Enable Native PHY Debug Master Endpoint (NPDME)**
- **Enable capability registers**
- **Enable prbs soft accumulators**
- **Enable odi acceleration logic**

A checkmark in the check box to the left of the parameter turns this parameter on. When the parameter is turned on, the IP core include these transceiver reconfiguration capabilities. A check box with no checkmark indicates that the option is turned off, and the IP core does not support these features.

By default, the **Enable Native PHY Debug Master Endpoint (NPDME)** parameter is turned off.

This parameter is available only for 50G Interlaken IP core variations that target an Intel Arria 10 device.

#### Related Information

##### [Intel Intel Arria 10 Transceiver PHY User Guide](#)

The Implementing Protocols in Intel Intel Arria 10 Transceivers chapter explains these Intel Intel Arria 10 Native PHY IP core parameters.

## Transceiver Reference Clock Frequency

The **Transceiver reference clock frequency** parameter specifies the expected frequency of the `p11_ref_clk` input clock.

If the actual frequency of the `p11_ref_clk` input clock does not match the value you specify for this parameter, the design fails in both simulation and hardware.

The 50G Interlaken IP core supports the following `p11_ref_clk` frequencies: 156.25 MHz, 195.3125 MHz, 250 MHz, 312.5 MHz, 390.625 MHz, 500 MHz, and 625 MHz.

The default value of the **Transceiver reference clock frequency** parameter is 312.5 MHz.

#### Related Information

- [50G Interlaken IP Core Clock Signals](#) on page 4-5
- [50G Interlaken IP Core Clock Interface Signals](#) on page 5-1

## Number of Calendar Pages

The **Number of calendar pages** parameter specifies the number of 16-bit pages of in-band flow control data that your 50G Interlaken IP core supports. The supported values are **1, 2, 4, 8, and 16**.

Each 16-bit calendar page includes 16 in-band flow control bits. The application determines the interpretation of the in-band flow control bits. The IP core supports a maximum of 256 channels with in-band flow control.

If your design requires a different number of pages, select the lowest supported number of pages which is larger than the number required, and ignore any unused pages. For example, if your configuration requires three in-band flow control calendar pages, you can set **Number of Calendar pages** to 4 and use pages 3, 2, and 1 while ignoring page 0.

The default value of the **Number of calendar pages** parameter is 1.

## TX Scrambler Seed

The **TX scrambler seed** parameter specifies the initial scrambler state.

If a single 50G Interlaken IP Core is configured on your device, you can use the default value of this parameter.

If multiple 50G Interlaken IP Cores are configured on your device, you must use a different initial scrambler state for each IP core to reduce crosstalk. Try to select random values for each 50G Interlaken IP core, such that they have an approximately even mix of ones and zeros and differ from the other scramblers in multiple spread out bit positions.

The default value of this parameter is 58'hdeadbeef123.

## Transfer Mode Selection

The **Transfer mode selection** parameter specifies whether the 50G Interlaken transmitter expects incoming traffic to the TX user data transfer interface to be interleaved or packet based. The supported values are **Interleaved** and **Packet**. Interleaved mode is also called Segmented mode. The value of this parameter cannot be modified dynamically; it is determined when you generate the IP core.

If the value of this parameter is **Packet**, the 50G Interlaken transmitter expects incoming traffic to the TX user data transfer interface to be packet based. This setting enables the internal enhanced scheduler and causes the IP core to send data on the Interlaken link based on the programmed `BurstMax` and `BurstMin` parameter settings.

If the value of this parameter is **Interleaved**, the 50G Interlaken transmitter expects you to provide Start of Burst (SOB) and End of Burst (EOB) indications with the data on the TX user data transfer interface. In Interleaved mode, you can send either packet-based traffic or interleaved traffic, but you must provide the correct SOB and EOB signals even when sending non-interleaved packets. In this mode, the IP core does not implement the enhanced scheduler. The IP core ignores the `BurstMax` and `BurstMin` values. `BurstShort` is still in effect. To avoid overflowing the transmit FIFO, you should not send a burst that is longer than 1024 bytes.

If packets are always sent contiguously in your application, Intel recommends that you set this parameter to the value of **Packet**. This setting enables simpler transfers on the user data transfer interface, and enables the 50G Interlaken IP core to perform enhanced scheduling based on the `BurstMax` and `BurstMin` settings. If the data bursts that arrive on the TX application interface might be interleaved between channels, then you must set **Transfer mode selection** to the value of **Interleaved**.

The default value of the **Transfer mode selection** parameter is **Interleaved**.

### Related Information

[Interleaved and Packet Modes](#) on page 4-7

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The 50G Interlaken IP core provides the functionality described in the *Interlaken Protocol Specification, Revision 1.2*.

#### Related Information

[Interlaken Protocol Specification, Revision 1.2](#)

## Interfaces Overview

The Intel 50G Interlaken IP core supports the following interfaces:

[Application Interface](#) on page 4-1

[Interlaken Interface](#) on page 4-1

[Out-of-Band Flow Control Interface](#) on page 4-2

[Management Interface](#) on page 4-2

[Transceiver Control Interfaces](#) on page 4-2

## Application Interface

The application interface, also called the user data transfer interface, provides up to 256 channels of communication to and from the Interlaken link.

#### Related Information

- [High Level Block Diagram](#) on page 4-4  
The figure lists the major application interface signals.
- [50G Interlaken IP Core User Data Transfer Interface Signals](#) on page 5-4  
Comprehensive list of application interface signals and information about required signal behavior.

## Interlaken Interface

The Interlaken interface complies with the *Interlaken Protocol Specification, Revision 1.2*. It provides a high-speed transceiver interface to an Interlaken link.

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The 50G Interlaken IP core value for the Interlaken BurstMax parameter is determined by the value you specify on the `burst_max_in` input signal. The 50G Interlaken IP core supports two values for BurstMax, 128 bytes and 256 bytes.

**Note:** You should only modify the value of the `burst_max_in` signal when no traffic is present.

You can configure your 50G Interlaken IP core to use 1, 2, 4, 8, or 16 pages of 16 calendar bits. The application determines the use of the in-band flow control bits that the IP core receives on the incoming Interlaken link, and the application is responsible for specifying the values of the in-band flow control bits the IP core transmits on the outgoing Interlaken link.

#### Related Information

- [50G Interlaken IP Core Interlaken Link and Miscellaneous Interface Signals](#) on page 5-8  
Information about setting the BurstMax and BurstShort values, including the encoding of your desired value on the `burst_max_in` or `burst_short_in` input signal.
- [50G Interlaken IP Core User Data Transfer Interface Signals](#) on page 5-4  
Information about the in-band flow control signals.
- [Interlaken Protocol Specification, Revision 1.2](#)  
Available from the Interlaken Alliance web site at [www.interlakenalliance.com](http://www.interlakenalliance.com).

## Out-of-Band Flow Control Interface

The optional out-of-band flow control interface conforms to the out-of-band requirements in Section 5.3.4.2, Out-of-Band Flow Control, of the *Interlaken Protocol Specification, Revision 1.2*.

#### Related Information

- [Out-of-Band Flow Control in the 50G Interlaken IP core](#) on page 9-1
- [Interlaken Protocol Specification, Revision 1.2](#)  
Available from the Interlaken Alliance web site at [www.interlakenalliance.com](http://www.interlakenalliance.com).

## Management Interface

The management interface provides access to the 50G Interlaken IP core internal status and control registers. This interface does not provide access to the hard PCS registers on the device.

The management interface complies with the Avalon Memory-Mapped (Avalon-MM) specification defined in the *Avalon Interface Specifications*.

#### Related Information

[Avalon Interface Specifications](#)

## Transceiver Control Interfaces

The 50G Interlaken IP core provides several interfaces to control the transceiver. The transceiver control interfaces in your 50G Interlaken IP core variation depend on the device family the variation targets.

The 50G Interlaken IP core supports the following transceiver control interfaces:

[Transceiver Reconfiguration Controller Interface](#) on page 4-3

[Intel Arria 10 External PLL Interface](#) on page 4-3

[Intel Arria 10 Transceiver Reconfiguration Interface](#) on page 4-3

## Transceiver Reconfiguration Controller Interface

50G Interlaken IP core variations that target an Arria V or a Stratix V device require an external reconfiguration controller to function correctly in hardware. 50G Interlaken IP core variations that target an Arria 10 device include a reconfiguration controller block and do not require an external reconfiguration controller.

### Related Information

#### [Intel Transceiver PHY IP Core User Guide](#)

Describes the Intel Transceiver Reconfiguration Controller and the signals that connect to the 50G Interlaken IP core transceiver reconfiguration controller interface.

## Intel Arria 10 External PLL Interface

50G Interlaken IP core variations that target an Arria 10 device require an external transceiver PLL to function correctly in hardware. 50G Interlaken IP core variations that target an Arria V or Stratix V device include the transceiver PLLs and do not require that you configure any additional PLLs.

### Related Information

- [Adding the External PLL](#) on page 2-15  
Describes how to generate an external TX PLL, including parameter requirements.
- [Intel Arria 10 External PLL Interface Signals](#) on page 5-15
- [Intel Arria 10 Transceiver PHY User Guide](#)  
Information about the Intel Arria 10 transceiver PLLs and clock network.

## Intel Arria 10 Transceiver Reconfiguration Interface

The Intel Arria 10 transceiver reconfiguration interface provides access to the registers in the embedded Intel Arria 10 Native PHY IP core. This interface provides direct access to the hard PCS registers on the device.

This interface is available only in variations that target an Intel Arria 10 device. In variations that target an Arria V device or a Stratix V device, user logic reconfigures the transceivers through the transceiver reconfiguration controller, an external block that you must instantiate in your design outside the 50G Interlaken IP core.

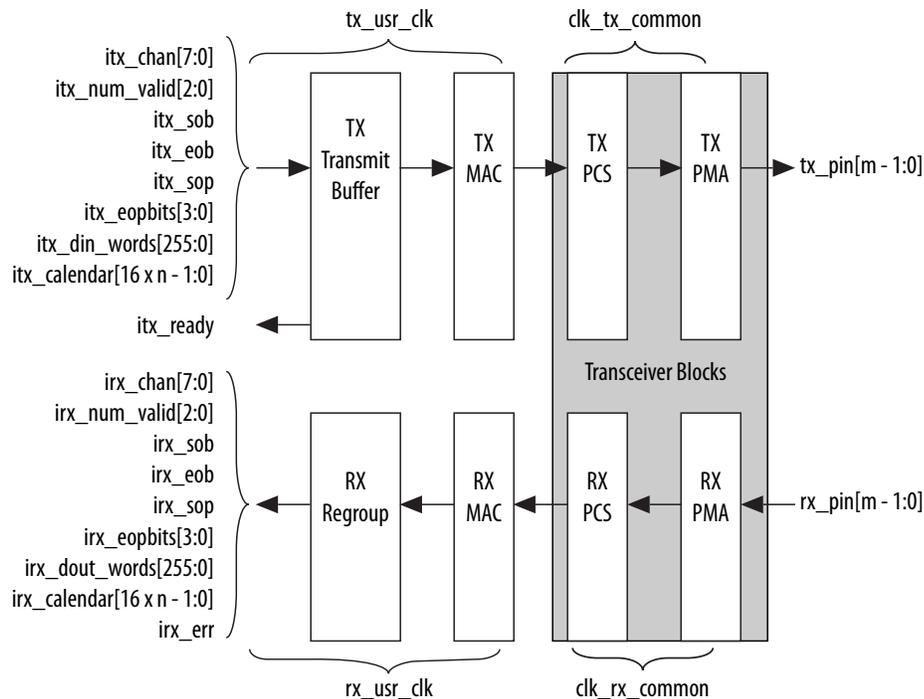
The Intel Arria 10 transceiver reconfiguration interface complies with the Avalon Memory-Mapped (Avalon-MM) specification defined in the *Avalon Interface Specifications*.

### Related Information

- [Avalon Interface Specifications](#)  
Defines the Avalon Memory-Mapped (Avalon-MM) specification.
- [Intel Arria 10 Transceiver PHY User Guide](#)  
Information about the Intel Arria 10 transceiver reconfiguration interface.
- [Intel Arria 10 Transceiver Registers](#)  
Information about the Intel Arria 10 transceiver registers.

## High Level Block Diagram

Figure 4-1: 50G Interlaken Block Diagram



The 50G Interlaken IP core consists of two paths: an Interlaken TX path and an Interlaken RX path. Each path includes MAC, PCS, and PMA blocks. The PCS blocks are implemented in hard IP.

### Related Information

- [50G Interlaken IP Core Transmit Path Blocks](#) on page 4-13  
For more information about the Interlaken TX path.
- [50G Interlaken IP Core Receive Path Blocks](#) on page 4-19  
For more information about the Interlaken RX path.

## Clocking and Reset Structure for IP Core

The following topics describe the clocking and reset structure of the 50G Interlaken IP core:

[50G Interlaken IP Core Clock Signals](#) on page 4-5

[IP Core Reset](#) on page 4-5

[IP Core Reset Sequence with the Reconfiguration Controller](#) on page 4-7

## 50G Interlaken IP Core Clock Signals

Table 4-1: 50G Interlaken IP Core Clocks

Clock Name	Description
<code>pll_ref_clk</code>	Reference clock for the RX CDR PLL in IP core variations that target an Intel Arria 10 device. Reference clock for the RX CDR PLL and the TX transceiver PLL in all other variations.
<code>tx_serial_clk[NUM_LANES-1:0]</code>	Clocks for the individual transceiver channels in 50G Interlaken IP core variations that target an Intel Arria 10 device.
<code>rx_usr_clk</code>	Clock for the receive application interface.
<code>tx_usr_clk</code>	Clock for the transmit application interface.
<code>mm_clk</code>	Management clock for 50G Interlaken IP core register access.
<code>reconfig_clk</code>	Management clock for Intel Arria 10 hard PCS register access, including access for Intel Arria 10 transceiver reconfiguration and testing features.

If you choose to instantiate the optional out-of-band flow control blocks, your 50G Interlaken IP core has additional clock domains.

### Related Information

[Out-of-Band Flow Control Block Clocks](#) on page 9-2

Comprehensive list of out-of-band flow control block clocks and information about their expected frequencies.

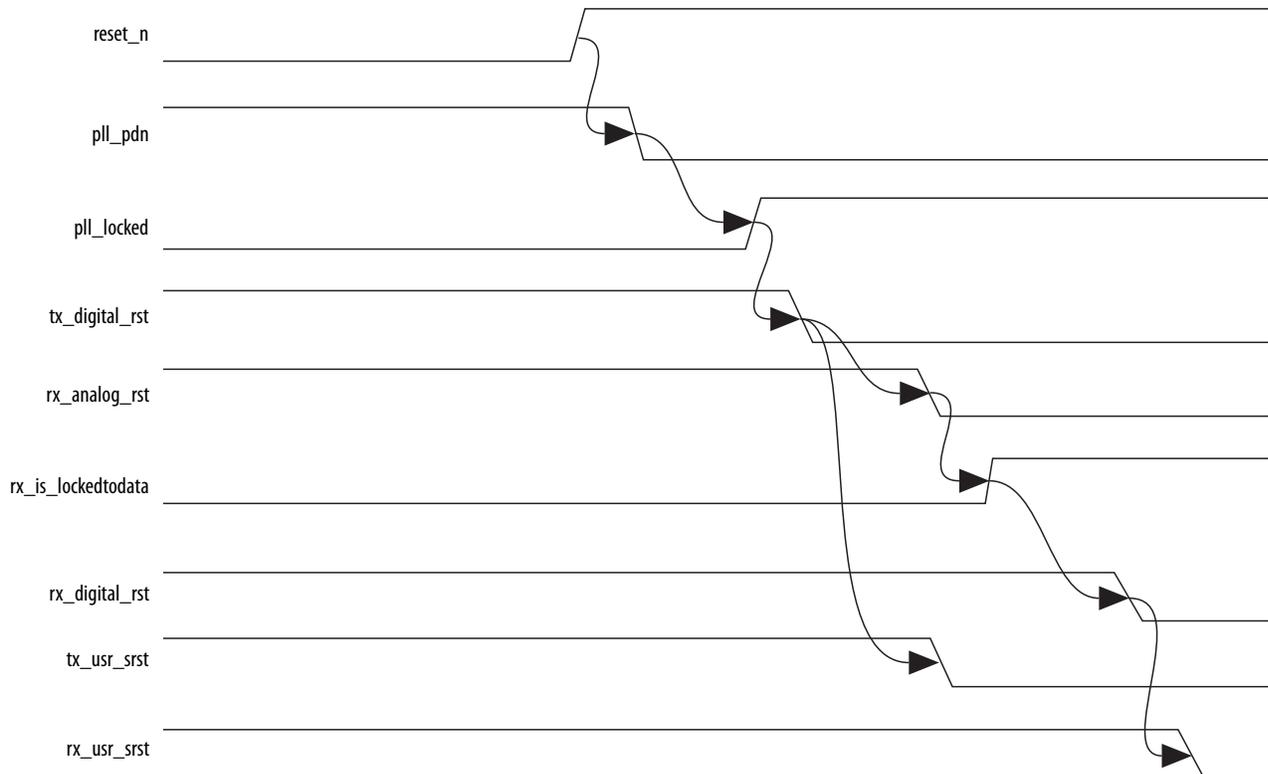
## IP Core Reset

The 50G Interlaken IP core variations have a single asynchronous reset, the `reset_n` signal. The 50G Interlaken IP core manages the initialization sequence internally. After you de-assert `reset_n` (raise it after asserting it low), the IP core automatically goes through the entire reset sequence.

**Note:** Intel recommends that you hold the `reset_n` signal low for at least the duration of two `mm_clk` cycles, to ensure the reset sequence proceeds correctly.

**Figure 4-2: 50G Interlaken IP Core Transceiver Initialization Sequence**

The internal initialization sequence implemented by the reset controller included in the 50G Interlaken IP core. In Intel Arria 10 devices, the `pll_locked` signal originates in the external PLL. In other devices, it originates in the 50G Interlaken IP core itself.



Following completion of the reset sequence internally, the 50G Interlaken IP core begins link initialization. If your 50G Interlaken IP core and its Interlaken link partner initialize the link successfully, you can observe the assertion of the lane and link status signals according to the Interlaken specification. For example, you can monitor the `tx_lanes_aligned`, `sync_locked`, `word_locked`, and `rx_lanes_aligned` output status signals.

By default, in Arria V GZ and Stratix V devices, after you de-assert the `reset_n` signal, you must wait  $2^{20}$  `mm_clk` cycles before you attempt to access the 50G Interlaken IP core registers using the IP core management interface. You can modify the size of the reset counter with an RTL parameter. Intel recommends that you set the value of the RTL parameter `CNTR_BITS` to six for simulation. If you set `CNTR_BITS` to the value of six, you must wait  $2^6$  `mm_clk` cycles before you attempt to access the 50G Interlaken IP core registers using the IP core management interface.

In Intel Arria 10 devices, the required wait time from de-asserting the `reset_n` signal to safely accessing the IP core registers is a function of the internal reset controller. The IP core instantiates an Intel Transceiver PHY Reset Controller in Intel Arria 10 variations.

**Related Information**

- [IP Core Reset Sequence with the Reconfiguration Controller](#) on page 4-7  
You must wait until the required Altera Transceiver Reconfiguration Controller completes configuration of the transceivers before you assert the `reset_n` signal.
- [Intel Arria 10 Transceiver PHY User Guide](#)  
For more information about the Intel Transceiver PHY Reset Controller that is included in Intel Arria 10 variations of the 50G Interlaken IP core, refer to the Transceiver Reset Control in Intel Arria 10 Devices chapter.

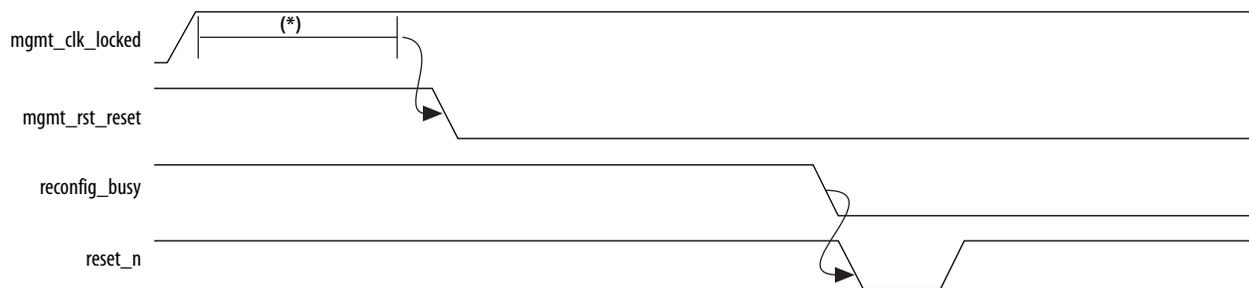
**IP Core Reset Sequence with the Reconfiguration Controller**

If your 50G Interlaken IP core targets an Arria V device or a Stratix V device, you must connect the 50G Interlaken IP core to an Intel Reconfiguration Controller. At power up, the Reconfiguration Controller configures the transceivers. After power up, upon completion of the transceiver configuration process, the Reconfiguration Controller returns control of the reset to your application. You must wait until the Reconfiguration Controller completes configuration of the transceivers before you assert the `reset_n` signal.

The Reconfiguration Controller indicates the end of the configuration cycle by deasserting the `reconfig_busy` signal. After `reconfig_busy` is deasserted, you can assert `reset_n`. Intel recommends that you hold the `reset_n` signal low for at least the duration of two `mm_clk` cycles, to ensure the reset sequence proceeds correctly.

**Figure 4-3: Reset Sequence With the Reconfiguration Controller**

Indicates when you can safely assert the `reset_n` signal of the 50G Interlaken IP core.



You must wait at least  $2^{(CNTR\_BITS + 3)}$  `mm_clk` cycles after the `mgmt_clk` locks before you deassert the `mgmt_rst_reset` input signal to the reconfiguration controller.

**Related Information****V-Series Transceiver PHY IP Core User Guide**

For more information about the Intel Reconfiguration Controller.

**Interleaved and Packet Modes**

You can configure the 50G Interlaken IP core to accept interleaved data transfers from the application on the TX user data transfer interface, or to not accept interleaved data transfers on this interface. If the IP core can accept interleaved data transfers, it is in Interleaved mode, sometimes also called Segmented

mode. If the IP core does not accept interleaved data transfers, it is in Packet mode. The value you specify for the **Transfer mode selection** parameter in the 50G Interlaken parameter editor determines the IP core transmit mode.

In Packet mode, the 50G Interlaken IP Core performs Optional Scheduling Enhancement based on Section 5.3.2.1.1 of the *Interlaken Protocol Specification, Revision 1.2*. The IP core ignores the `itx_sob` and `itx_eob` signals. Instead, the IP core performs optional enhanced scheduling based on the settings of `BurstMax`, `BurstMin`, and `BurstShort`.

In Interleaved mode, the 50G Interlaken IP Core inserts burst control words on the Interlaken link based on the `itx_sob` and `itx_eob` inputs. The internal optional enhanced scheduling is disabled and the `BurstMax` and `BurstMin` values are ignored. `BurstShort` is still in effect. To avoid overflowing the transmit FIFO, you should not send a burst that is longer than 1024 bytes.

In Interleaved mode or in Packet mode, the 50G Interlaken IP core is capable of accepting non-interleaved data on the TX user data transfer interface (`itx_din_words`). However, if the IP core is in Interleaved mode, the application must drive the `itx_sob` and `itx_eob` inputs correctly.

In Interleaved mode or in Packet mode, the 50G Interlaken IP core can generate interleaved data transfers on the RX user data transfer interface (`irx_dout_words`). The application must be able to accept interleaved data transfers if the Interlaken link partner transmits them on the Interlaken link. In this case, the Interlaken link partner must send traffic in Interleaved mode that conforms with the 50G Interlaken IP core `BurstShort` value.

**Note:** The transmitter (link partner) must only send packets with a minimum packet size of 64 bytes.

#### Related Information

- [Transfer Mode Selection](#) on page 3-3
- [50G Interlaken IP Core User Data Transfer Interface Signals](#) on page 5-4
- [Interlaken Protocol Specification, Revision 1.2](#)

## 50G Interlaken IP Core Transmit Path

The 50G Interlaken IP core accepts application data from up to 256 channels and combines it into a single data stream in which data is labeled with its source channel. The 50G Interlaken TX MAC and PCS blocks format the data into protocol-compliant bursts and insert Idle words where required.

### 50G Interlaken IP Core Transmit User Data Interface Examples

The following examples illustrate how to use the Intel 50G Interlaken IP core TX user data interface:

[50G Interlaken IP Core Interleaved Mode \(Segmented Mode\) Example](#) on page 4-8

[50G Interlaken IP Core Packet Mode Operation Example](#) on page 4-10

[50G Interlaken IP Core Back-Pressured Packet Transfer Example](#) on page 4-11

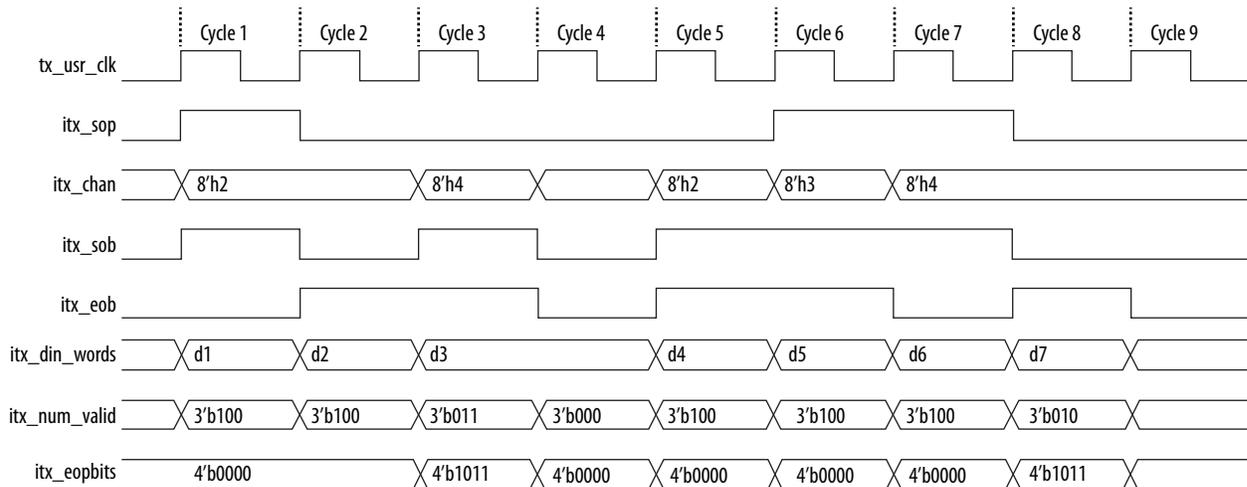
### 50G Interlaken IP Core Interleaved Mode (Segmented Mode) Example

In Interleaved Mode, you are responsible for scheduling the burst. You need to drive an extra pair of signals, Start of Burst (SOB) and End of Burst (EOB), to indicate the burst boundary. You can send the

traffic in packet order or interleaved order, as long as you set the SOB and EOB flags correctly to establish the data boundaries.

**Figure 4-4: Packet Transfer on Transmit Interface in Interleaved Mode**

This example illustrates the expected behavior of the 50G Interlaken IP core application interface transmit signals during data transfers from the application to the IP core on the TX user data transfer interface in interleaved mode.



The figure shows the timing diagram for an interleaved data transfer in Interleaved mode. In cycle 1, the application asserts `itx_sop` and `itx_sob`, indicating that this cycle is both the start of the burst and the start of the packet. The value the application drives on `itx_chan` indicates the data originates from channel 2.

In cycle 2, the application asserts `itx_eob`, indicating the data the application transfers to the IP core in this clock cycle is the end of the burst. (`itx_chan` only needs to be valid when `itx_sob` or `itx_sop` is asserted). `itx_num_valid[2:0]` indicates all four words are valid. However, the data in this cycle is not end of packet data. The application is expected to transfer at least one additional data burst in this packet, possibly interleaved with one or more bursts in packets from different data channels.

Cycle 3 is a short burst with both `itx_sob` and `itx_eob` asserted. The application drives the value of three on `itx_num_valid[2:0]` to indicate that three words of the four-word `itx_din_words` data bus are valid. The data is packed in the most significant words of `itx_din_words`. The application drives the value of `4'b1011` on `itx_eopbits` to indicate that the data the application transfers to the IP core in this cycle are the final words of the packet, and that in the final word of the packet, only three bytes are valid data. The value the application drives on `itx_chan` indicates this burst originates from channel 4.

In cycle 4, the `itx_num_valid[2:0]` signal has the value of zero, which means this cycle is an idle cycle.

In cycle 5, the application sends another single-cycle data burst from channel 2, by asserting `itx_sob` and `itx_eob` to indicate this data is both the start and end of the burst. The application does not assert `itx_sop`, because this burst is not start of packet data. `itx_eopbits` has the value of `4'b0000`, indicating this burst is also not end of packet data. This data follows the data burst transferred in cycles 1 and 2, within the same packet from channel 2.

In cycle 6, the application sends a start of packet, single-cycle data burst from channel 3.

In cycles 7 and 8, the application sends a two-cycle data packet in one two-cycle burst. In cycle 8, the second data cycle, the application drives the value of two on `itx_num_valid[2:0]` and the value of `4'b1011` on `itx_eopbits`, to tell the IP core that in this clock cycle, the two most significant words of the data symbol contain valid data and the remaining words do not contain valid data, and that in the second of these two words, only the three most significant bytes contain valid data.

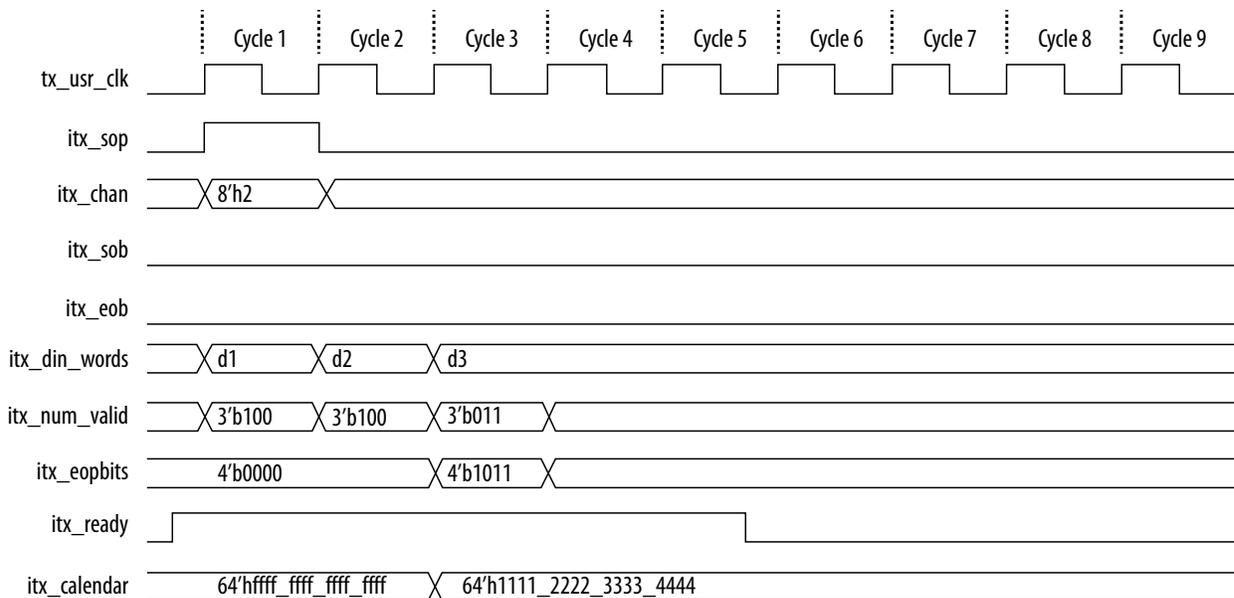
In Interleaved Mode, you can transfer a packet without interleaving as long as the channel number does not toggle during the same packet transfer. However, you must still assert the `itx_sob` and `itx_eob` signals correctly to maintain the proper burst boundaries.

If you do not drive the `itx_sob` and `itx_eob` signals, the 50G Interlaken IP Core does not operate properly and the transmit FIFO may overflow, since in this mode the internal logic is looking for `itx_sob` and `itx_eob` assertion for insertion of proper burst control words.

## 50G Interlaken IP Core Packet Mode Operation Example

**Figure 4-5: Packet Transfer on Transmit Interface in Packet Mode**

This example illustrates the expected behavior of the 50G Interlaken IP core application interface transmit signals during a packet transfer in packet mode.



The figure illustrates a packet mode data transfer of 83 bytes on the transmit interface into the IP core. In this mode, the 50G Interlaken IP core ignores the `itx_sob` and `itx_eob` input signals.

To start a transfer, you assert `itx_sop` when you have data ready on `itx_din_words`. At the following rising edge of the clock, the IP core detects that `itx_sop` is asserted, indicating that the value on `itx_din_words` in the current cycle is the start of an incoming data packet. When you assert `itx_sop`, you must also assert the correct value on `itx_chan` to tell the IP core the data channel source of the data. In this example, the value 2 on `itx_chan` tells the IP core that the data originates from channel number 2.

During the SOP cycle (labeled with data value d1) and the cycle that follows the SOP cycle (labeled with data value d2), you must hold the value of `itx_num_valid[2:0]` at 3'b100. In the following clock cycle, labeled with data value d3, you must hold the following values on critical input signals to the IP core:

- `itx_num_valid[2:0]` at the value of 3'b011 to indicate the current data symbol contains three 64-bit words of valid data.
- `itx_eopbits[3]` high to indicate the current cycle is an EOP cycle.
- `itx_eopbits[2:0]` at the value of 3'b011 to indicate that only three bytes of the final valid data word are valid data bytes.

This signal behavior correctly transfers a data packet with the total packet length of 83 bytes to the IP core, as follows:

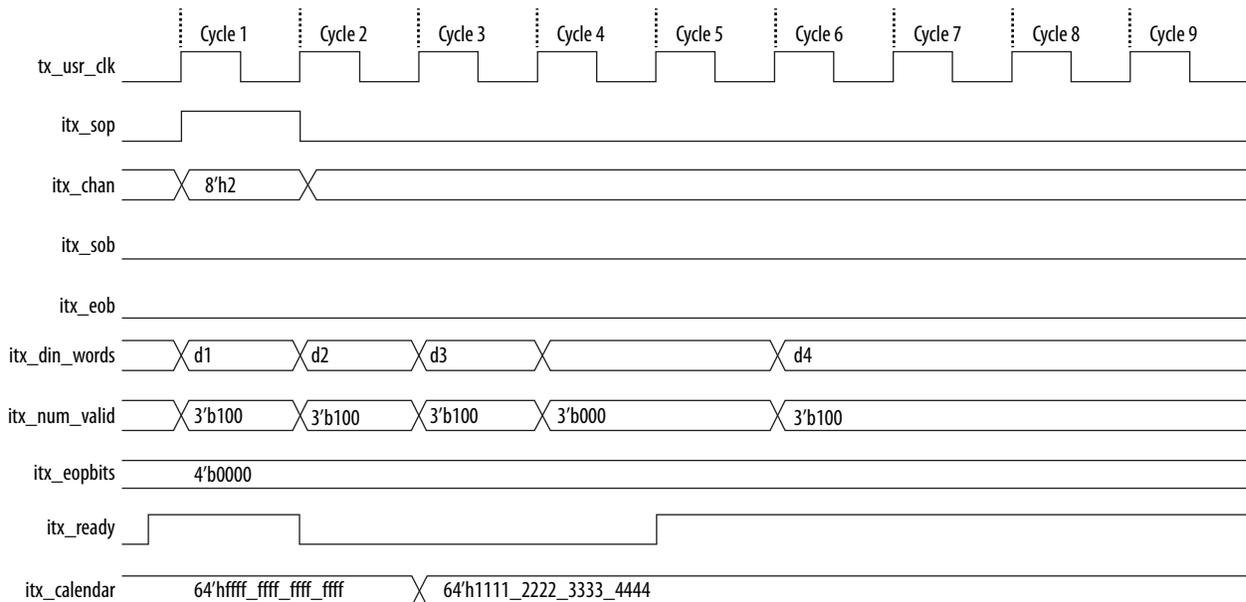
- In the SOP cycle, the IP core receives 32 bytes of valid data (d1).
- In the following clock cycle, the IP core receives another 32 bytes of valid data (d2).
- In the third clock cycle, the EOP cycle, the IP core receives two full words (2 x 8 = 16 bytes) and three bytes of valid data, for a total of 19 valid bytes.

The total packet length is 32 + 32 + 19 = 83 bytes.

## 50G Interlaken IP Core Back-Pressured Packet Transfer Example

Figure 4-6: Packet Transfer on Transmit Interface with Back Pressure

This example illustrates the expected behavior of the 50G Interlaken application interface transmit signals during a packet transfer with back pressure.



In this example, the 50G Interlaken IP Core accepts the first four data symbols (128 bytes) of a data packet. The clock cycles in which the application transfers the data values d2 and d3 to the 50G Interlaken IP Core are grace-period cycles following the 50G Interlaken IP Core's de-assertion of `itx_ready`.

The 50G Interlaken IP Core supports up to 4 cycles of grace period, enabling you to register the input data and control signals, as well as the `itx_ready` signal, without changing functionality. The grace period

supports your design in achieving timing closure more easily. In any case you must ensure that you hold `itx_num_valid` at the value of 0 when you are not driving data.

You can think of this interface as a FIFO write interface. When `itx_num_valid[2:0]` is nonzero, both data and control information (including `itx_num_valid[2:0]` itself) are written to the transmit side data interface. The `itx_ready` signal is the inverse of a hypothetical FIFO-almost-full flag. When `itx_ready` is high, the 50G Interlaken IP Core is ready to accept data. When `itx_ready` is low, you can continue to send data for another 6 to 8 clock cycles of `tx_usr_clk`.

#### Related Information

[50G Interlaken IP Core In-Band Calendar Bits on Transmit Side](#) on page 4-12  
Description of in-band calendar bits on the TX user data transfer interface.

## 50G Interlaken IP Core In-Band Calendar Bits on Transmit Side

The `itx_calendar` input signal supports in-band flow control. It is synchronous with `tx_usr_clk`, but does not align with the packets on the user data interface. The 50G Interlaken IP Core reads the `itx_calendar` bits and encodes them in control words (Burst control words and Idle control words) opportunistically.

If you hold all the calendar bits at one, you indicate an XON setting for each channel. You should set the calendar bits to 1 to indicate that the Interlaken link partner does not need to throttle the data it transfers to this 50G Interlaken IP Core. Set this value by default if you choose not to use the in-band flow control feature of the 50G Interlaken IP Core. If you decide to turn off any channel, you must drive the corresponding bits of `itx_calendar` with zero (the XOFF setting) for that channel.

The 50G Interlaken IP Core transmits each page of the `itx_calendar` bits on the Interlaken link in a separate control word, starting with the most significant page and working through the pages, in order, to the least significant page.

Consider an example where the number of calendar pages is four and `itx_calendar` bits are set to the value `64'h1111_2222_3333_4444`. In this example, the Number of calendar pages parameter is set to four, and therefore the width of the `itx_calendar` signal is  $4 \times 16 = 64$  bits. Each of these bits is a calendar bit. The transmission begins with the page with the value of `16'h1111` and works through the pages in order until the least significant page with the value of `16'h4444`.

In this example, four control words are required to send the full set of 64 calendar bits from the `itx_calendar` signal. The 50G Interlaken IP Core automatically sets the Reset Calendar bit[56] of the next available control word to the value of one, to indicate the start of transmission of a new set of calendar pages, and copies the most significant page (`16'h1111` in this example) to the In-Band Flow Control bits[55:40] of the control word. It maps the most significant bit of the page to the control word bit[55] and the least significant bit of the page to the control word bit[40].

The table shows the value of the Reset Calendar bit and the In-Band Flow Control bits in the four Interlaken link control words that transmit the `64'h1111_2222_3333_4444` value of `itx_calendar`:

**Table 4-2: Value of Reset Calendar Bit and In-band Flow Control Bits in the Example**

Control Word	Reset Calendar Bit (bit [56])	In-Band Flow Control Bits (bits [55:40])
First	1	16'b0001000100010001 (16'h1111)

Control Word	Reset Calendar Bit (bit [56])	In-Band Flow Control Bits (bits [55:40])
Second	0	16'b0010001000100010 (16'h2222)
Third	0	16'b0011001100110011 (16'h3333)
Fourth	0	16'b0100010001000100 (16'h4444)

For details of the control word format, refer to the *Interlaken Protocol Specification*, Revision 1.2.

The 50G Interlaken IP Core supports `itx_calendar` widths of **1, 2, 4, 8, and 16** 16-bit calendar pages. You configure the width in the 50G Interlaken IP Core parameter editor.

By convention, in a standard case, each calendar bit corresponds to a single data channel. However, the 50G Interlaken IP Core assumes no default usage. You must map the calendar bits to channels or link status according to your specific application needs. For example, if your design has 64 physical channels, but only 16 priority groups, you can use a single calendar page and map each calendar bit to four physical channels. As another example, for a different application, you can use additional calendar bits to pass quality-of-service related information to the Interlaken link partner.

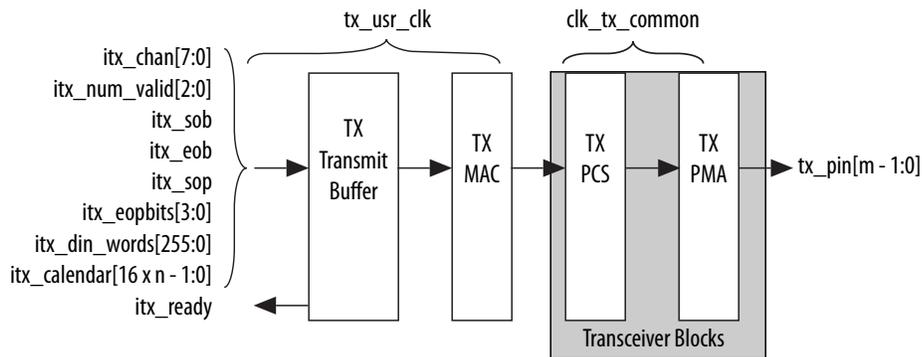
If your application flow-controls a channel, you are responsible for dropping the relevant packet. Intel supports the transfer of the `itx_calendar` values you provide without examining the data that is affected by in-band flow control of the Interlaken link.

**Related Information**

- [50G Interlaken IP Core Back-Pressured Packet Transfer Example](#) on page 4-11  
Example of in-band calendar bits usage on the TX user data transfer interface.
- [Interlaken Protocol Specification, Revision 1.2](#)

## 50G Interlaken IP Core Transmit Path Blocks

Figure 4-7: 50G Interlaken IP Core Transmit Path



The 50G Interlaken IP core transmit data path has the following four main functional blocks:

[50G Interlaken IP Core TX Transmit Buffer](#) on page 4-14

[50G Interlaken IP Core TX MAC](#) on page 4-14

[50G Interlaken IP Core TX PCS](#) on page 4-14

[50G Interlaken IP Core TX PMA](#) on page 4-14

## 50G Interlaken IP Core TX Transmit Buffer

The 50G Interlaken IP core TX transmit buffer performs the following function:

- Aligns the incoming user application data, `itx_data`, in the IP core internal format.

## 50G Interlaken IP Core TX MAC

The 50G Interlaken IP core TX MAC performs the following functions:

- Inserts burst and idle control words in the incoming data stream. Burst delineation allows packet segmentation in the Interlaken protocol.
- Performs flow adaptation of the data stream, repacking the data to ensure the maximum number of words is available on each valid clock cycle.
- Calculates and inserts CRC24 bits in all burst and idle words.
- Inserts calendar data in all burst and idle words.
- Stripes the data across the PCS lanes. Configurable order, default is MSB of the data goes to lane 0.
- Buffers data between the application and the TX PCS block in the TX FIFO buffer. The TX PCS block uses the FIFO buffer to recover bandwidth when the number of words delivered to the transmitter is less than the full width.

## 50G Interlaken IP Core TX PCS

TX PCS logic is an embedded hard macro and does not consume FPGA soft logic elements.

The 50G Interlaken IP core TX PCS block performs the following functions for each lane:

- Inserts the meta frame words in the incoming data stream.
- Calculates and inserts the CRC32 bits in the meta frame diagnostic words.
- Scrambles the data according to the scrambler seed and the protocol-specified polynomial.
- Performs 64B/67B encoding.

## 50G Interlaken IP Core TX PMA

The 50G Interlaken IP core TX PMA serializes the data and sends it out on the Interlaken link.

## 50G Interlaken IP Core Receive Path

The 50G Interlaken IP core receives data on the Interlaken link, monitors and removes Interlaken overhead, and provides user data to the application.

## 50G Interlaken IP Core Receive User Data Interface Examples

The following examples illustrate how to use the Intel 50G Interlaken IP core RX user data interface:

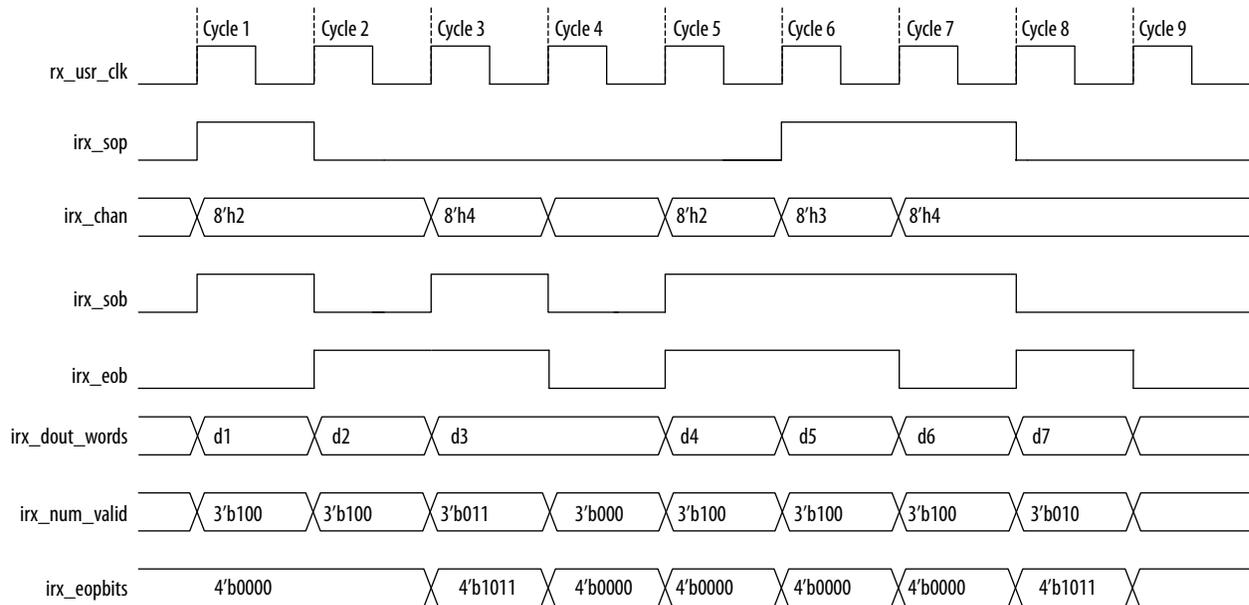
[50G Interlaken IP Core Receiver Side Example](#) on page 4-15

## 50G Interlaken IP Core Receiver Side Example

The 50G Interlaken IP Core can generate interleaved data transfers on the RX user data transfer interface. The IP core always toggles the `irx_sop` and `irx_eob` signals to indicate the beginning of the burst and end of the burst.

**Figure 4-8: 50G Interlaken IP Core Receiver Side Example**

This example illustrates the expected behavior of the 50G Interlaken IP core application interface receive signals during data transfers from the IP core to the application on the RX user data transfer interface in interleaved mode.



The figure shows the timing diagram for an interleaved data transfer in Interleaved mode. In cycle 1, the IP core asserts `irx_sop` and `irx_sob`, indicating that this cycle is both the start of the burst and the start of the packet. The first word is MSB aligned at the top. The value the IP core drives on `irx_chan` indicates the data targets channel 2. You must sample `irx_chan` during cycles in which `irx_sob` is asserted. The `irx_chan` output signal is not guaranteed to remain valid for the duration of the burst.

In cycle 2, the IP core asserts `irx_eob`, indicating the data the IP core transfers to the application in this clock cycle is the end of the burst. `irx_num_valid[2:0]` indicates all four words are valid. However, the data in this cycle is not end of packet data. The IP core transfers at least one additional data burst in this packet, possibly interleaved with one or more bursts in packets that target different data channels.

Cycle 3 is a short burst with both `irx_sob` and `irx_eob` asserted. The IP core drives the value of three on `irx_num_valid[2:0]` to indicate that three words of the four-word `irx_dout_words` data bus are valid. The data is packed in the most significant words of `irx_dout_words`. The IP core drives the value of `4'b1011` on `irx_eopbits` to indicate that the data the IP core transfers to the application in this cycle are the final words of the packet, and that in the final word of the packet, only three bytes are valid data. The value the IP core drives on `irx_chan` indicates this burst targets channel 4.

In cycle 4, the `irx_num_valid[2:0]` signal has the value of zero, which means this cycle is an idle cycle.

In cycle 5, the IP core sends another single-cycle data burst to channel 2, by asserting `irx_sob` and `irx_eob` to indicate this data is both the start and end of the burst. The IP core does not assert `irx_sop`,

because this burst is not start of packet data. `irx_eopbits` has the value of `4'b0000`, indicating this burst is also not end of packet data. This data follows the data burst transferred in cycles 1 and 2, within the same packet the IP core is sending to channel 2.

In cycle 6, the IP core sends a start of packet, single-cycle data burst to channel 3.

In cycles 7 and 8, the IP core sends a two-cycle data packet in one two-cycle burst. In cycle 8, the second data cycle, the IP core drives the value of two on `irx_num_valid[2:0]` and the value of `4'b1011` on `irx_eopbits`, to tell the application that in this clock cycle, the two most significant words of the data symbol contain valid data and the remaining words do not contain valid data, and that in the second of these two words, only the three most significant bytes contain valid data.

## 50G Interlaken IP Core RX Errored Packet Handling

The 50G Interlaken IP Core provides information about errored packets on the RX user data transfer interface through the following output signals:

- `irx_eopbits[3:0]`—If this signal has the value of `4'b0001`, an error indication arrived with the packet on the incoming Interlaken link: the `EOP_Format` field of the control word following the final burst of the packet on the Interlaken link has this value, which indicates an error and EOP.
- `irx_err`—The 50G Interlaken IP Core checks the integrity of incoming packets on the Interlaken link, and reports the packet corruption errors it detects on the RX user data transfer interface in the `irx_err` output signal.

In both cases, the application is responsible for discarding the relevant packet.

The `irx_err` signal reflects the following errors:

- CRC24 errors
- Loss of lane alignment
- Illegal control word
- Illegal framing pattern
- Missing SOP or EOP indicator

The `irx_err` output signal is aligned with `irx_eopbits`, and is always asserted when `irx_eopbits` has the value of `4'b0001`. However, `irx_eopbits` can have the value of `4'b0001` when `irx_err` is not asserted, if the error indication arrived on the Interlaken link but the 50G Interlaken IP Core does not detect any of the listed integrity issues in the incoming packet communication.

The `irx_err` signal indicates approximately where an error occurs: the corruption could have occurred at the SOP of the current packet, in some later cycle in the payload of the current packet, in a packet that is interleaved with the current packet, or in the current EOP cycle. When the IP core identifies an error in the data it receives on the Interlaken link, it marks every packet currently open on the link as errored, rather than attempt to associate the error with a specific channel. Therefore, the application need not drop any packets that are not marked explicitly as errored using one of the two mechanisms.

The `irx_err` signal asserts one time only, whether a single error or multiple errors occurred in the packet. If the current EOP cycle data is corrupted so badly that the EOP indication is missing, the `irx_err` error indication is aligned to the next EOP. If an error occurs during an IDLE cycle, the `irx_err` is aligned to the next EOP.

The application is responsible for discarding packets it receives from the IP core with `irx_err` asserted during the EOP cycle, just as it is responsible for discarding packets it receives from the IP core with `irx_eopbits` set to `4'b0001`. The application is not responsible for tracking the open packets interleaved

with the errored packet — the 50G Interlaken IP Core asserts `irx_err` in the EOP cycle of every potentially errored packet, and the application can rely on the fact that if `irx_err` is not asserted and `irx_eopbits` has a value other than `4'b0001`, the packet is not errored.

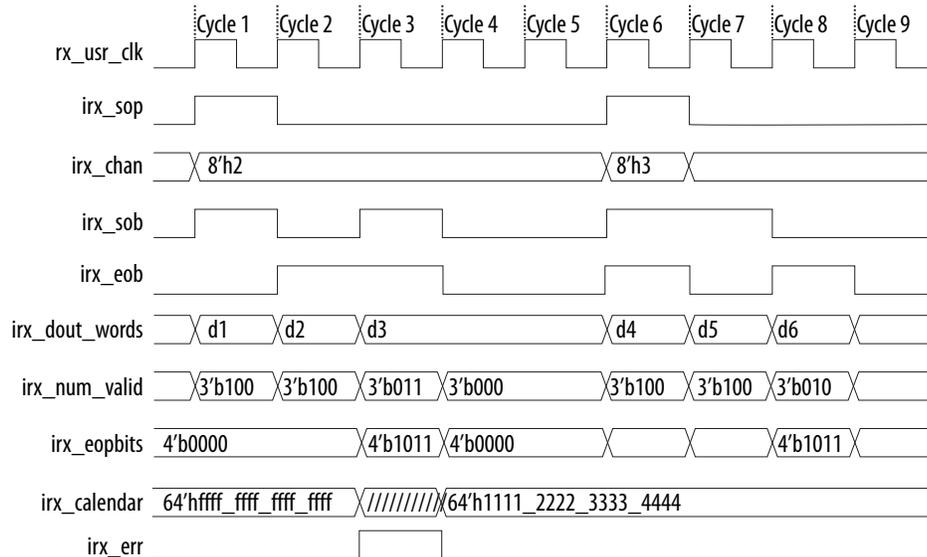
For CRC24 errors, you should use the `crc24_err` status signal, rather than relying on the `irx_err` signal, in the following situations:

- If you monitor the link when only Idle control words are being received (no data is flowing), you should monitor the real time status signal `crc24_err`.
- If you maintain a count of CRC24 errors, you should monitor the number of times that the real time status signal `crc24_err` is asserted.

## 50G Interlaken IP Core Receiver Side Example With Errors and In-Band Calendar Bits

Figure 4-9: 50G Interlaken IP Core Receiver Side Example With `irx_err` Errors

This example illustrates the expected behavior of the 50G Interlaken IP core application interface receive signals during a packet transfer with CRC or other errors. In the example, the errored packet transfer is followed by two idle cycles and a non-errored packet transfer.



This figure illustrates the attempted transfer of a 83-byte packet on the RX user data transfer interface to channel 2, after the 50G Interlaken IP Core receives the packet on the Interlaken link and detects corruption. Following the errored packet, the IP core transfers an uncorrupted packet to channel 3.

In cycle 1, the 50G Interlaken IP Core asserts `irx_sop` when data is ready on `irx_dout_words`. When the 50G Interlaken IP Core asserts `irx_sop`, it also asserts the correct value on `irx_chan` to tell the application the data channel destination of the data. In this example, the value 2 on `irx_chan` tells the application that the data should be sent to channel number 2.

During the SOP cycle (labeled with data value `d1`) and the cycle that follows the SOP cycle (labeled with data value `d2`), the 50G Interlaken IP Core holds the value of `irx_num_valid[2:0]` at `3'b100`. In the

following clock cycle, labeled with data value d3, the 50G Interlaken IP Core holds the following values on critical output signals:

- `irx_num_valid[2:0]` at the value of 3'b011 to indicate the current data symbol contains three 64-bit words of valid data.
- `irx_eopbits[3]` high to indicate the current cycle is an EOP cycle.
- `irx_eopbits[2:0]` at the value of 3'b011 to indicate that only three bytes of the final valid data word are valid data bytes.

This signal behavior, in the absence of the `irx_err` flag, would correctly transfer a data packet with the total packet length of 83 bytes from the 50G Interlaken IP Core.

However, the 50G Interlaken IP Core marks the packet as errored by asserting the `irx_err` signal, even though the `irx_eopbits` signal would appear to indicate the packet is valid.

The application is responsible for discarding the errored packet when it detects that the IP core has asserted the `irx_err` signal.

Following the corrupted packet, the IP core waits two idle cycles and then transfers a valid 75-byte packet.

#### Related Information

- [50G Interlaken IP Core Packet Mode Operation Example](#) on page 4-10  
The first data transfer in the current example is the receiver interface equivalent of the transmitter interface transfer example described at this link.
- [In-Band Calendar Bits on the 50G Interlaken IP Core Receiver User Data Interface](#) on page 4-18  
Description of in-band calendar bits on the RX user data transfer interface.

## In-Band Calendar Bits on the 50G Interlaken IP Core Receiver User Data Interface

The 50G Interlaken IP core receiver logic decodes incoming control words (both Burst control words and Idle control words) on the incoming Interlaken link, extracts the calendar pages from the In-Band Flow Control bits, and assembles them into the `irx_calendar` output signal.

The 50G Interlaken IP core receives the most significant calendar page in a control word with the Reset Calendar bit set, indicating the beginning of the calendar page sequence. The mapping of bits from the control words to the `irx_calendar` output signal is consistent with the mapping of bits from the `itx_calendar` input signal to the control words.

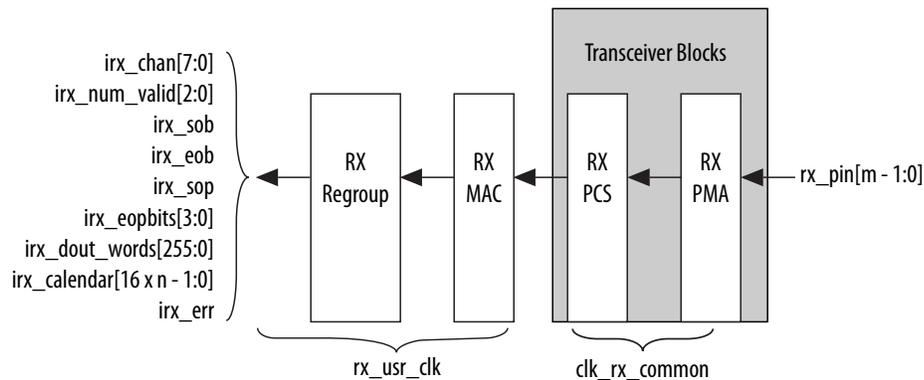
On the RX side, your application is responsible for mapping the calendar pages to the corresponding channels, according to any interpretation agreed upon with the Interlaken link partner application in sideband communication. On the TX side, your application is responsible for throttling the data it transfers to the TX user data transfer interface, in response to the agreed upon interpretation of the `irx_calendar` bits.

#### Related Information

- [50G Interlaken IP Core In-Band Calendar Bits on Transmit Side](#) on page 4-12
- [50G Interlaken IP Core Receiver Side Example With Errors and In-Band Calendar Bits](#) on page 4-17  
Example of in-band calendar bits usage on the RX user data transfer interface.

## 50G Interlaken IP Core Receive Path Blocks

Figure 4-10: 50G Interlaken IP Core Receive Path



The 50G Interlaken IP core receive data path has the following four main functional blocks:

[50G Interlaken IP Core RX PMA](#) on page 4-19

[50G Interlaken IP Core RX PCS](#) on page 4-19

[50G Interlaken IP Core RX MAC](#) on page 4-19

[50G Interlaken IP Core RX Regroup Block](#) on page 4-20

### 50G Interlaken IP Core RX PMA

The 50G Interlaken IP core RX PMA deserializes data that the IP core receives on the serial lines of the Interlaken link.

### 50G Interlaken IP Core RX PCS

RX PCS logic is an embedded hard macro and does not consume FPGA soft logic elements.

The 50G Interlaken IP core RX PCS block performs the following functions to retrieve the data:

- Detects word lock and word synchronization.
- Checks running disparity.
- Reverses gearboxing and 64/67B encoding.
- Descrambles the data.
- Delineates meta frame boundaries.
- Performs CRC32 checking.
- Sends lane status information to the calendar and status blocks.

### 50G Interlaken IP Core RX MAC

To recover a packet or burst, the RX MAC takes data from each of the PCS lanes and reassembles the packet or burst.

The 50G Interlaken IP core RX MAC performs the following functions:

- Data de-striping, including lane alignment and burst assembly from the PCS lanes.
- CRC24 validation
- Calendar recovery

### 50G Interlaken IP Core RX Regroup Block

The 50G Interlaken IP core RX regroup block performs the following function:

- Translates the IP core internal data format to the outgoing user application data `irx_data` format.

**Note:** Regroup block requires the upstream logic to send packets with the minimum `BURSTMIN` and `BURSTSHORT` parameter setting as 64 bytes.

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The 50G Interlaken IP core communicates with the surrounding design through multiple external signals.

## 50G Interlaken IP Core Clock Interface Signals

Table 5-1: 50G Interlaken IP Core Clock Interface

Signal Name	Direction	Width (Bits)	Description
<b>Clock Ports</b>			
pll_ref_clk	Input	1	<p>Transceiver reference clock for the RX CDR PLL in IP core variations that target an Intel Arria 10 device. Transceiver reference clock for the RX CDR PLL and the TX transceiver PLL in all other variations.</p> <p>The 50G Interlaken IP core supports the following pll_ref_clk frequencies: 156.25 MHz, 195.3125 MHz, 250 MHz, 312.5 MHz, 390.625 MHz, 500 MHz, and 625 MHz.</p> <p>The pll_ref_clk input clock frequency must match the value you specify for the <b>Transceiver reference clock frequency</b> parameter.</p>
tx_serial_clk	Input	NUM_LANES-	Clocks for the individual transceiver channels in 50G Interlaken IP core variations that target an Intel Arria 10 device.
clk_tx_common	Output	1	PCS common lane clock driven by the SERDES transmit PLL. The clock rate is the lane rate divided by 40 bits. The clk_tx_common frequency is 156.25 MHz for 6.25 Gbps per lane.
clk_rx_common	Output	1	Master recovered lane clock. The Interlaken specification requires all incoming lanes to run at the same frequency.

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Signal Name	Direction	Width (Bits)	Description
tx_usr_clk	Input	1	<p>Transmit side user data interface clock. To achieve 40 Gbps Ethernet traffic throughput, you must run this clock at a minimum frequency of 200 MHz.</p> <p>By default, you must drive this clock at 250 MHz. To change the input clock frequency, you must first modify the value of the TX_USR_CLK_MHZ advanced parameter to the new frequency. The allowed range of frequencies you can specify is 200 MHz to 300 MHz.</p>
rx_usr_clk	Input	1	<p>Receive side user data interface clock. To achieve 40 Gbps Ethernet traffic throughput, you must run this clock at a minimum frequency of 200 MHz.</p> <p>By default, you must drive this clock at 250 MHz. To change the input clock frequency, you must first modify the value of the TX_USR_CLK_MHZ advanced parameter to the new frequency. The allowed range of frequencies you can specify is 200 MHz to 300 MHz.</p>
mm_clk	Input	1	<p>Management clock. Clocks the register accesses. It is also used for clock rate monitoring and some analog calibration procedures. You must run this clock at a frequency in the range of 100 MHz–125 MHz.</p>
reconfig_clk	Input	1	<p>Clocks the Intel Arria 10 transceiver reconfiguration interface. This clock is available only in IP core variations that target an Intel Arria 10 device. You should run this clock at a frequency of 100 MHz.</p>

**Note:** If you change the port name or period of a clock, then you must modify `.sdc` file to match the corresponding changes.

#### Related Information

[Performance and Fmax Requirements for 40G Ethernet Traffic](#) on page 10-1

Explains the tx\_usr\_clk and rx\_usr\_clk frequency requirements.

## 50G Interlaken IP Core Reset Interface Signals

Table 5-2: 50G Interlaken IP Core Reset Interface

Signal Name	Direction	Width (Bits)	Description
<b>50G Interlaken IP Core Reset Signals</b>			

Signal Name	Direction	Width (Bits)	Description
<code>reset_n</code>	Input	1	Active-low reset signal for the 50G Interlaken IP core. Intel recommends that you hold this signal low for at least the duration of two <code>mm_clk</code> cycles, to ensure the reset sequence proceeds correctly.
<code>reconfig_reset</code>	Input	1	Reset signal for the Intel Arria 10 transceiver reconfiguration interface. This signal is available only in IP core variations that target an Intel Arria 10 device.
<code>srst_tx_common</code>	Output	1	Synchronous reset signal that the IP core asserts high while the transmitter is initializing. This signal is synchronous with <code>clk_tx_common</code> .  This signal goes low to indicate that the transceiver PLL has locked to the reference clock. The TX PCS and the TX MAC are held in reset while the <code>srst_tx_common</code> reset signal is asserted. You can use this signal for diagnostic purposes.
<code>srst_rx_common</code>	Output	1	Synchronous reset that is active at startup. This signal is synchronous with <code>clk_rx_common</code> . This signal goes low to indicate that the transceiver PLL has achieved lock and the recovered clock has locked to data in normal operation, this signal is deasserted after the transceiver completes its reset sequence. The RX PCS and the RX MAC are held in reset while the <code>srst_rx_common</code> reset signal is asserted. This signal is also active in the event of a serious clock data recovery failure on any of the RX lanes.
<code>tx_usr_srst</code>	Output	1	Transmit side reset output signal. Indicates the transmit side user data interface is resetting. This signal is synchronous with <code>tx_usr_clk</code> . Your application can use this signal to reset any status counters you may maintain in the <code>tx_usr_clk</code> domain.
<code>rx_usr_srst</code>	Output	1	Receive side reset output signal. Indicates the receive side user data interface is resetting. This signal is synchronous with <code>rx_usr_clk</code> . Your application can use this signal to reset any status counters you may maintain in the <code>rx_usr_clk</code> domain.

## 50G Interlaken IP Core User Data Transfer Interface Signals

Table 5-3: 50G Interlaken IP Core User Data Transfer Interface

Signal Name	Direction	Width (Bits)	Description
<b>50G Interlaken IP Core Transmit User Interface</b>			
itx_chan	Input	8	Transmit logic channel number. The IP core supports up to 256 channels. The 50G Interlaken IP core samples this value only when <code>itx_sop</code> or <code>itx_sob</code> is high and <code>itx_num_valid</code> has a non-zero value.
itx_num_valid	Input	3	<p><code>itx_num_valid[2:0]</code> specifies the number of valid 64-bit words in the current packet in the current data symbol. The maximum value of <code>itx_num_valid[2:0]</code> is four, because a data symbol on the 256 bit wide data path has four words (4 x 64 bits = 256 bits).</p> <p>In non-valid cycles, you must set the value of <code>itx_num_valid[2:0]</code> to zero.</p> <p>In valid cycles, you must set the value of <code>itx_num_valid[2:0]</code> as follows:</p> <ul style="list-style-type: none"> <li>3'b100: if all four words contain valid data from the current packet.</li> <li>3'b0xx: where xx indicates the number of valid words that are part of the current packet, if the number is less than four. Data is always MSB aligned (left aligned). For example, the value of 3'b011 indicates that word 0 (bit [63:0]) is not valid.</li> </ul> <p>You must set the value of <code>itx_num_valid</code> to zero in all non-valid cycles, even when <code>itx_ready</code> is not asserted.</p>
itx_sop	Input	1	<p>Indicates the current data symbol on <code>itx_din_words</code> contains the start of a packet (SOP). This signal has the following valid values:</p> <ul style="list-style-type: none"> <li>1'b0—The current data symbol does not contain the start of a packet.</li> <li>1'b1—The current data symbol contains the start of a packet.</li> </ul>

Signal Name	Direction	Width (Bits)	Description
<code>itx_eopbits</code>	Input	4	<p>Indicates whether the current data symbol contains the end of a packet (EOP) with or without an error, and specifies the number of valid bytes in the current end-of-packet, non-error 8-byte data word, if relevant.</p> <p>You must set the value of <code>itx_eopbits</code> as follows:</p> <ul style="list-style-type: none"> <li>4b'0000: no end of packet, no error.</li> <li>4b'0001: Error and end of packet.</li> <li>4b'1xxx: End of packet. xxx indicates the number of valid bytes in the final valid 8-byte word of the packet, as follows: <ul style="list-style-type: none"> <li>3b'000: all 8 bytes are valid.</li> <li>3b'001: 1 byte is valid.</li> <li>...</li> <li>3b'111: 7 bytes are valid.</li> </ul> </li> </ul> <p>All other values (4'b01xx, 4'b001x) are undefined.</p> <p>The valid bytes always start in bit positions [63:56] of the final valid data word of the packet.</p>
<code>itx_sob</code>	Input	1	<p>Indicates the current data symbol contains the start of a burst (SOB). If the 50G Interlaken IP core is in Interleaved mode, you are responsible for providing this start of the burst signal. If the 50G Interlaken IP core is in Packet mode, the IP core ignores this signal. The 50G Interlaken IP core samples the <code>itx_chan</code> signal during this cycle.</p> <p>This signal has the following valid values:</p> <ul style="list-style-type: none"> <li>1'b0—The current data symbol does not contain the start of a burst.</li> <li>1'b1—The current data symbol contains the start of a burst.</li> </ul> <p>Typically, you use this mode for sending interleaved packets. However, you can still send non-interleaved packets as long as you provide the <code>itx_sob</code> and <code>itx_eob</code> signal values. You are responsible to comply with the <code>BurstMax</code> and <code>BurstMin</code> parameters. If the burst you send is too large, it can overflow the 50G Interlaken transmit buffer.</p>
<code>itx_eob</code>	Input	1	<p>End of the burst. If the 50G Interlaken IP core is in Interleaved mode, you are responsible for providing this end of the burst signal. If the 50G Interlaken IP core is in Packet mode, the IP core ignores this signal. You are responsible to comply with the <code>BurstMax</code> and <code>BurstMin</code> parameters.</p>
<code>itx_din_words</code>	Input	256	<p>The four 64-bit words of input data (one data symbol). When <code>itx_num_valid</code> has the value of zero, the IP core ignores <code>itx_din_words</code>.</p>

Signal Name	Direction	Width (Bits)	Description
itx_calendar	Input	16 N	Multiple pages (16 bits per page) of calendar input bits. The 50G Interlaken IP Core copies these bits to the in-band flow control bits in N control words that it sends on the Interlaken link. N is the value of the <b>Number of calendar pages</b> parameter, which can be any of 1, 2, 4, 8, or 16. This signal is synchronous with <code>tx_usr_clk</code> , although it is not part of the user data transfer protocol.
itx_ready	Output	1	Flow control signal to back pressure transmit traffic. When this signal is high, you can send traffic to the IP core. When this signal is low, you should stop sending traffic to the IP core within one to four cycles.  You can consider the inverse of <code>itx_ready</code> to be a FIFO-almost-full indicator. In full duplex mode, <code>itx_ready</code> is low when <code>rx_lanes_aligned</code> is low.
itx_ifc_err	Output	1	Indicates the transmit side user data transfer interface received traffic that the 50G Interlaken IP Core does not support. The IP core asserts the <code>itx_ifc_err</code> signal in the following cases: <ul style="list-style-type: none"> <li>In Interleaved mode, the IP core receives a burst that exceeds the size of MaxBurst.</li> <li>Two instances of non-zero <code>itx_sop</code> (a start of packet), or two instances of non-zero <code>itx_sob</code> (a start of burst), are separated by fewer than 64 bytes.</li> </ul> The IP core asserts the <code>itx_ifc_err</code> signal for a single clock cycle. The signal pulses within the current burst, with a delay of one or two cycles after the error on the transmit side user data transfer interface.

## 50G Interlaken IP Core Receive User Interface

irx_chan	Output	8	Receive logic channel number. The IP core supports up to 256 channels. You should sample this value when <code>irx_sop</code> or <code>irx_sob</code> is high and <code>irx_num_valid</code> has a non-zero value.
irx_num_valid	Output	3	<code>irx_num_valid[2:0]</code> specifies the number of valid 64-bit words in the current packet in the current data symbol. The maximum value of <code>irx_num_valid[2:0]</code> is four, because a data symbol on the 256 bit wide data path has four words (4 x 64 bits = 256 bits).  In valid cycles, the IP core sets the value of <code>irx_num_valid[2:0]</code> as follows: <ul style="list-style-type: none"> <li>3'b100: if all four words contain valid data from the current packet.</li> <li>3'b0xx: where xx indicates the number of valid words that are part of the current packet, if the number is less than four. Data is always MSB aligned (left aligned). For example, the value of 3'b011 indicates that word 0 (bit [63:0]) is not valid.</li> </ul> The IP core sets the value of <code>irx_num_valid</code> to zero in all non-valid cycles.

Signal Name	Direction	Width (Bits)	Description
<code>irx_sop</code>	Output	1	<p>Indicates the current data symbol on <code>irx_dout_words</code> contains the start of a packet (SOP). This signal has the following valid values:</p> <ul style="list-style-type: none"> <li>1'b0—The current data symbol does not contain the start of a packet.</li> <li>1'b1—The current data symbol contains the start of a packet.</li> </ul>
<code>irx_eopbits</code>	Output	4	<p>Indicates whether the current data symbol contains the end of a packet (EOP) with or without an error, and specifies the number of valid bytes in the current end-of-packet, non-error 8-byte data word, if relevant.</p> <p>The IP core sets the value of <code>irx_eopbits</code> as follows:</p> <ul style="list-style-type: none"> <li>4b'0000: no end of packet, no error.</li> <li>4b'0001: Error and end of packet.</li> <li>4b'1xxx: End of packet. xxx indicates the number of valid bytes in the final valid 8-byte word of the packet, as follows: <ul style="list-style-type: none"> <li>3b'000: all 8 bytes are valid.</li> <li>3b'001: 1 byte is valid.</li> <li>...</li> <li>3b'111: 7 bytes are valid.</li> </ul> </li> </ul> <p>All other values (4'b01xx, 4'b001x) are undefined and are not generated by the IP core.</p> <p>The valid bytes always start in bit positions [63:56] of the final valid data word of the packet.</p>
<code>irx_sob</code>	Output	1	<p>Start of the burst. The 50G Interlaken IP core indicates the start of the burst. The signal <code>irx_channel</code> is only valid when <code>irx_sob</code> is high. This signal toggles in Packet Mode and in Interleaved Mode.</p> <p>This signal has the following valid values:</p> <ul style="list-style-type: none"> <li>1'b0—The current data symbol does not contain the start of a burst.</li> <li>1'b1—The current data symbol contains the start of a burst.</li> </ul>
<code>irx_eob</code>	Output	1	<p>End of the burst. The 50G Interlaken IP core indicates the end of the burst. This signal toggles in Packet Mode and in Interleaved Mode.</p>
<code>irx_dout_words</code>	Output	256	<p>The four 64-bit words of output data (one data symbol). When <code>irx_num_valid</code> has the value of zero, you should ignore <code>irx_dout_words</code>.</p>
<code>irx_calendar</code>	Output	16 × N	<p>Multiple pages (16 bits per page) of calendar output bits. The value is the in-band flow control bits from N control words on the incoming Interlaken link. N is the value of the <b>Number of calendar pages</b> parameter, which can be any of 1, 2, 4, 8, or 16. This signal is synchronous with <code>rx_usr_clk</code>, although it is not part of the user data transfer protocol.</p>

Signal Name	Direction	Width (Bits)	Description
irx_err	Output	1	<p>Indicates an errored packet. This signal is valid only when both <code>irx_num_valid[2:0]</code> and <code>irx_eopbits[3:0]</code> are non-zero.</p> <p>When a CRC24 or other error occurs, the 50G Interlaken IP core asserts this signal for all open channel packets to label them all as errored packets, because the IP core cannot assign the error to a specific channel.</p>

#### Related Information

- [50G Interlaken IP Core RX Errored Packet Handling](#) on page 4-16  
Describes the behavior of the `irx_err` signal.
- [Transfer Mode Selection](#) on page 3-3  
Describes the parameter to select Packet or Interleaved mode.
- [Interleaved and Packet Modes](#) on page 4-7  
Describes the Packet and Interleaved modes.

## 50G Interlaken IP Core Interlaken Link and Miscellaneous Interface Signals

Table 5-4: 50G Interlaken IP Core SERDES Signals, Burst Parameter Signals, and Real Time Status Signals

Signal Name	Direction	Width (Bits)	Description
<b>SERDES Pins</b>			
<code>rx_pin</code>	Input	Number of lanes	Each bit represents the differential pair on an RX Interlaken lane.
<code>tx_pin</code>	Output	Number of lanes	Each bit represents the differential pair on a TX Interlaken lane.

#### TX Burst Control Settings

Signal Name	Direction	Width (Bits)	Description
burst_max_in	Input	4	<p>Encodes the BurstMax parameter for the IP core. The actual value of the BurstMax parameter must be a multiple of 64 bytes. While traffic is present, this input signal should remain static. However, when no traffic is present, you can modify the value of the <code>burst_max_in</code> signal to modify the BurstMax value of the IP core.</p> <p>The 50G InterlakenIP core supports the following valid values for this signal:</p> <ul style="list-style-type: none"> <li>2: 128 bytes</li> <li>4: 256 bytes</li> </ul>
burst_short_in	Input	4	<p>Encodes the BurstShort parameter for the IP core.</p> <p>The 50G Interlaken IP core supports the following valid value for this parameter:</p> <ul style="list-style-type: none"> <li>1: 32 bytes</li> </ul> <p>In general, the presence of the BurstMin parameter makes the BurstShort parameter obsolete.</p>
burst_min_in	Input	4	<p>Encodes the BurstMin parameter for the IP core.</p> <p>The IP core supports the following valid values for this signal:</p> <ul style="list-style-type: none"> <li>0: Disable optional enhanced scheduling. Intel recommends you do not drive this value. If you disable enhanced scheduling, performance is non-optimal.</li> <li>1: 32 bytes</li> <li>2: 64 bytes</li> <li>4: 128 bytes</li> </ul> <p>The BurstMin parameter should have a value that is less than or equal to half of the value of the BurstMax parameter.</p> <p>Intel recommends that you modify the value of this input signal only when no traffic is present on the TX user data interface. You do not need to reset the IP core.</p>

**Real-Time Transmit Status Signals (Synchronous with tx\_usr\_clk)**

Signal Name	Direction	Width (Bits)	Description
tx_lanes_aligned	Output	1	All of the transmitter lanes are aligned and are ready to send traffic.
itx_hungry	Output	1	<p>A dynamic status flag indicating that a downstream buffer which supplies data to the PCS is running empty. The IP core handles this situation by inserting IDLE symbols (IDLE control words) in the packet stream. Therefore, this signal does not indicate an error.</p> <p>This signal is asserted for the duration of the condition it indicates.</p> <p>The PCS runs continuously with the provided data or inserted IDLE symbols. This signal is usually asserted immediately after the IP core comes out of reset. However, the signal can also be asserted during normal operation, and is not a cause for concern.</p>
itx_overflow	Output	1	An error flag indicating that the PCS buffer is currently overflowing. This signal is asserted for the duration of the overflow condition: it is asserted in the first clock cycle in which the overflow occurs, and remains asserted until the PCS buffer pointers indicate that no overflow condition exists.
itx_underflow	Output	1	An error flag indicating that the PCS buffer is currently underflowed. In normal operation, this signal may be asserted temporarily immediately after the 50G Interlaken IP core comes out of reset. It is asserted as a single cycle wide pulse.

#### Real-Time Receiver Status Signals (Synchronous with rx\_usr\_clk)

sync_locked	Output	Number of lanes	Receive lane has locked on the remote transmitter Meta Frame. These signals are level signals: all bits are expected to stay high unless a problem occurs on the serial line.
word_locked	Output	Number of lanes	Receive lane has identified the 67-bit word boundaries in the serial stream. These signals are level signals: all bits are expected to stay high unless a problem occurs on the serial line.
rx_lanes_aligned	Output	1	All of the receiver lanes are aligned and are ready to receive traffic. This signal is a level signal.

Signal Name	Direction	Width (Bits)	Description
crc24_err	Output	1	<p>A CRC24 error flag covering both control word and data word. This signal does not associate the CRC24 error with a particular packet. Instead, its value indicates the overall SERDES status. You can use this signal to count the number of CRC24 errors.</p> <p>This signal is asserted as a single cycle wide pulse. If the IP core detects back-to-back CRC24 errors, this signal toggles.</p>
crc32_err	Output	Number of lanes	An error flag indicating diagnostic CRC32 failures per lane. This signal is asserted as a single cycle wide pulse. If back-to-back CRC32 errors are detected, this signal toggles.
irx_overflow	Output	1	An error flag indicating the presence of excessive jitter at the receiver side. This signal is included in the current IP core opportunistically for diagnostic purposes.
rdc_overflow	Output	1	An error flag indicating that the RX domain-crossing FIFO is currently overflowed. The RX domain-crossing FIFO transfers data from the PCS clock domain to the MAC clock domain.
rg_overflow	Output	1	An error flag indicating that the Reassembly FIFO is currently overflowed. The Reassembly FIFO is the receiver FIFO that feeds directly to the user data interface.
rxfifo_fill_level	Output	RXFIFO_ADDR_WIDTH	The fill level of the Reassembly FIFO, in units of 64-bit words. The width of this signal is the value of the RXFIFO_ADDR_WIDTH parameter, which is 12 by default. You can use this signal to monitor when the RX Reassembly FIFO is empty.
sop_cntr_inc	Output	1	A pulse indicating that the 50G Interlaken IP core receiver user data interface received a start-of-packet. You can use this signal to increment a count of SOPs the application observes on the receive interface.
eop_cntr_inc	Output	1	A pulse indicating that the 50G Interlaken IP core receiver user data interface received an end-of-packet. You can use this signal to increment a count of EOPs the application observes on the receive interface.

**Related Information**

[RXFIFO Address Width](#) on page 8-2

Information about programming the depth of the Reassembly FIFO with the `RXFIFO_ADDR_WIDTH` parameter.

## 50G Interlaken IP Core Management Interface

The 50G Interlaken IP core management interface allows you to communicate with IP core internal status and control registers. This interface manages the PMA (resets and serial loopback controls) and PCS control and status registers. This interface does not provide access to the hard PCS registers on the device.

The management interface is a typical 32-bit memory-mapped register port. It complies with the Avalon Memory-Mapped (Avalon-MM) specification defined in the *Avalon Interface Specifications*.

**Table 5-5: 50G Interlaken IP Core Management Interface Signals**

Signal Name	Direction	Width (Bits)	Description
<b>50G Interlaken IP Core Management Interface Signals</b>			
<code>mm_clk</code>	Input	1	Management clock. Clocks the register accesses. It is also used for clock rate monitoring and some analog calibration procedures. You must run this clock at a frequency in the range of 100 MHz–125 MHz.
<code>mm_clk_locked</code>	Input	1	Assert this signal to indicate that <code>mm_clk</code> is stable.  The IP core responds to this signal in the same way it responds to the <code>reset_n</code> signal: loss of lock restarts the reset sequence.  Intel recommends that you tie this signal high and not rely on its functionality. It is expected to be deprecated in the near future.
<code>mm_read</code>	Input	1	Read access to the register ports.
<code>mm_write</code>	Input	1	Write access to the register ports.
<code>mm_addr</code>	Input	16	Address to access the register ports.
<code>mm_rdata</code>	Output	32	When <code>mm_rdata_valid</code> is high, <code>mm_rdata</code> holds valid read data.
<code>mm_rdata_valid</code>	Output	1	Valid signal for <code>mm_rdata</code> .

Signal Name	Direction	Width (Bits)	Description
mm_wdata	Input	32	When mm_write is high, mm_wdata holds valid write data.

If you do not use the management interface, drive the management inputs as follows:

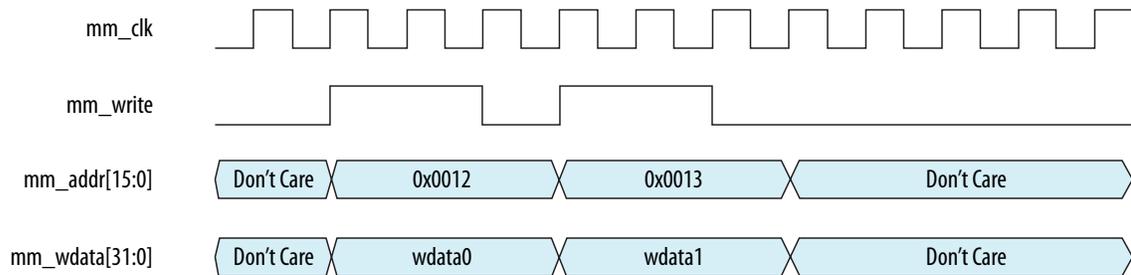
- mm\_clk must connect to a stable clock. However, the clock signal need not be of unusually high quality.
- mm\_clk\_locked must be tied to zero.
- mm\_read and mm\_write must be tied to zero.

If you use the management interface, drive the control lines as shown in the examples and observing the following constraints:

- During a write operation, you must maintain the mm\_write signal asserted for at least two clock cycles. Back-to-back writes must be separated by at least one clock cycle.
- During a read operation, you must maintain the mm\_read signal asserted for at least two clock cycles. Back-to-back reads must be separated by at least one clock cycle.

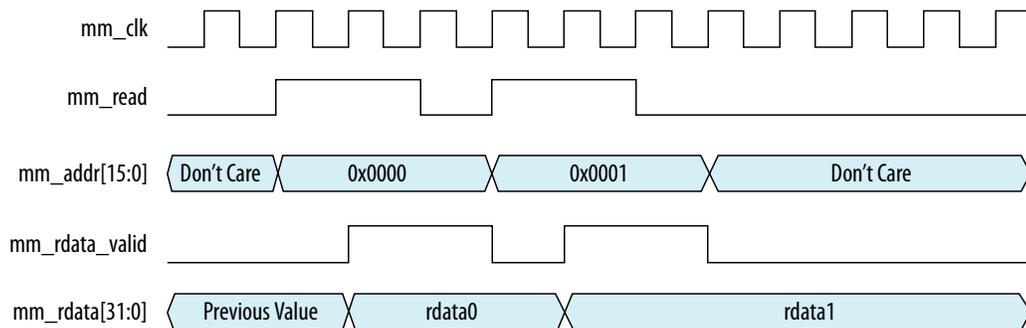
**Figure 5-1: 50G Interlaken IP Core Management Interface Write Operation**

Shows the timing requirements for a write operation on the 50G Interlaken IP core management interface.



**Figure 5-2: 50G Interlaken IP Core Management Interface Read Operation**

Shows the timing requirements for a read operation on the 50G Interlaken IP core management interface. The IP core asserts the mm\_rdata\_valid signal one cycle after the mm\_read signal is asserted.



**Related Information**[Avalon Interface Specifications](#)

## Device Dependent Signals

Some of the 50G Interlaken IP core signals depend on the device that your variation targets. Variations that target an Arria V device or a Stratix V device have an interface to connect to an Intel Transceiver Reconfiguration Controller that you must instantiate outside the 50G Interlaken IP core for successful functioning in hardware. Variations that target an Intel Arria 10 device have Intel Arria 10-specific requirements to support the Intel Arria 10 transceivers. The following 50G Interlaken IP core interfaces are device specific:

[Transceiver Reconfiguration Controller Interface Signals](#) on page 5-14

[Intel Arria 10 External PLL Interface Signals](#) on page 5-15

[Intel Arria 10 Transceiver Reconfiguration Interface Signals](#) on page 5-15

## Transceiver Reconfiguration Controller Interface Signals

50G Interlaken IP core variations that target an Arria V or a Stratix V device require an external reconfiguration controller to function correctly in hardware. 50G Interlaken IP core variations that target an Arria 10 device include a reconfiguration controller block and do not require an external reconfiguration controller.

**Table 5-6: 50G Interlaken IP Core Arria V and Stratix V Transceiver Reconfiguration Controller Interface Signals**

Signal Name	Direction	Width (Bits)	Description
reconfig_to_xcvr	Input	70 bits per reconfiguration interface.	Bus from the external transceiver reconfiguration controller to the 50G Interlaken IP core. The bus includes signals from multiple transceiver reconfiguration interfaces. The reconfiguration controller has one interface to control each transceiver channel (one per Interlaken lane) plus one interface to control each TX PLL configured in the IP core. The width of each reconfiguration controller output reconfiguration interface is 70 bits.

Signal Name	Direction	Width (Bits)	Description
reconfig_from_xcvr	Output	46 bits per reconfiguration interface	Bus to the external transceiver reconfiguration controller from the 50G Interlaken IP core. The bus includes signals for multiple reconfiguration interfaces of the transceiver reconfiguration controller. The reconfiguration controller has one interface for each transceiver channel (one per Interlaken lane) plus one interface for each TX PLL configured in the IP core. The width of each reconfiguration controller input reconfiguration interface is 46 bits.

## Intel Arria 10 External PLL Interface Signals

50G Interlaken IP core variations that target an Arria 10 device require an external transceiver PLL to function correctly in hardware. 50G Interlaken IP core variations that target an Arria V or Stratix V device include the transceiver PLLs and do not require that you configure any additional PLLs.

**Table 5-7: 50G Interlaken IP Core Intel Arria 10 External PLL Interface Signals**

Signal Name	Direction	Width (Bits)	Description
tx_serial_clk	Input	NUM_LANES	High-speed clock for Intel Arria 10 transceiver channel, provided from external TX PLL.
tx_pll_locked	Input	1	PLL-locked indication from external TX PLL.
tx_pll_powerdown	Output	1	Output signal from the IP core internal reset controller. The IP core asserts this signal to tell the external PLLs to power down.

### Related Information

[Adding the External PLL](#) on page 2-15

## Intel Arria 10 Transceiver Reconfiguration Interface Signals

The 50G Interlaken IP core Intel Arria 10 transceiver reconfiguration interface allows you to communicate with Intel Arria 10 hard PCS registers. This interface is available only in variations that target an Intel Arria 10 device. You use this interface to reconfigure the transceiver and to take advantage of built-in transceiver features that the 50G Interlaken IP Core supports for IP core testing. The interface allows you to address a single register in a single transceiver channel at one time.

The Intel Arria 10 transceiver reconfiguration interface is a typical 32-bit memory-mapped register port. It complies with the Avalon Memory-Mapped (Avalon-MM) specification defined in the *Avalon Interface Specifications*.

**Table 5-8: 50G Interlaken IP Core Intel Arria 10 Transceiver Reconfiguration Interface Signals**

Signal Name	Direction	Width (Bits)	Description
reconfig_clk	Input	1	Intel Arria 10 transceiver reconfiguration interface clock.
reconfig_reset	Input	1	Assert this signal to reset the Intel Arria 10 transceiver reconfiguration interface.
reconfig_read	Input	1	Read access to the Intel Arria 10 hard PCS registers.
reconfig_write	Input	1	Write access to the Intel Arria 10 hard PCS registers.
reconfig_address	Input	13	Address to access the hard PCS registers. This signal holds both the hard PCS register offset and the transceiver channel being addressed, in the following fields: <ul style="list-style-type: none"> <li>[9:0]: register offset in the hard PCS</li> <li>[12:10]: Interlaken lane number</li> </ul>
reconfig_readdata	Output	32	After user logic asserts the <code>reconfig_read</code> signal, when the IP core deasserts the <code>reconfig_waitrequest</code> signal, <code>reconfig_readdata</code> holds valid read data.
reconfig_waitrequest	Output	1	Busy signal for <code>reconfig_readdata</code> .
reconfig_writedata	Input	32	When <code>reconfig_write</code> is high, <code>reconfig_writedata</code> holds valid write data.

#### Related Information

##### [Avalon Interface Specifications](#)

Defines the Avalon-MM interface specification, including the behavior of the output signals and the expected behavior of the input signals.

# 50G Interlaken IP Core Register Map

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The 50G Interlaken IP core control registers are 32 bits wide and are accessible to you using the management interface, an Avalon-MM interface which conforms to the *Avalon Interface Specifications*. This table lists the registers available in the IP core. All unlisted locations are reserved.

**Table 6-1: 50G Interlaken IP Core Register Map**

Offset	Name	R/W	Description
9'h0	PCS_BASE	RO	[31:8] – Constant “HSi” ASCII [7:0] – version number Despite its name, this register does not encode the hard PCS base address.
9'h1	LANE_COUNT	RO	Number of lanes
9'h2	TEMP_SENSE	RO	Device temperature according to the internal temperature sensing diode. [7:0] – the temperature in degrees Fahrenheit [15:8] – the temperature in degrees Celsius For example, when the temperature is 54 degrees Celsius (130 degrees Fahrenheit), the value of the register is 0x3682. To interpret this register value, you read 0x36 (decimal 54) to be the temperature in degrees Celsius, and you read 0x82 (decimal 130) to be the temperature in degrees Fahrenheit. This register is invalid in the following IP core variations: <ul style="list-style-type: none"> <li>Variations that target an Intel Arria 10 device</li> <li>Variations in which you turn off the hidden parameter <b>Include Temp Sense</b></li> </ul>
9'h3	ELAPSED_SEC	RO	[23:0] - Elapsed seconds since power up. The IP core calculates this value from the management interface clock ( <code>mm_clk</code> ) for diagnostic purposes. During continuous operation, this value rolls over every 194 days.

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Offset	Name	R/W	Description
9'h4	TX_EMPTY	RO	[NUM_LANES-1:0] – Transmit FIFO status (empty)
9'h5	TX_FULL	RO	[NUM_LANES-1:0] – Transmit FIFO status (full)
9'h6	TX_PEMPTY	RO	[NUM_LANES-1:0] – Transmit FIFO status (partially empty)
9'h7	TX_PFULL	RO	[NUM_LANES-1:0] – Transmit FIFO status (partially full)
9'h8	RX_EMPTY	RO	[NUM_LANES-1:0] – Receive FIFO status (empty)
9'h9	RX_FULL	RO	[NUM_LANES-1:0] – Receive FIFO status (full)
9'hA	RX_PEMPTY	RO	[NUM_LANES-1:0] – Receive FIFO status (partially empty)
9'hB	RX_PFULL	RO	[NUM_LANES-1:0] – Receive FIFO status (partially full)
9'hC	REF_KHZ <sup>(1)</sup>	RO	PLL reference clock frequency (kHz)
9'hD	RX_KHZ <sup>(1)</sup>	RO	RX recovered clock frequency (kHz)
9'hE	TX_KHZ <sup>(1)</sup>	RO	TX serial clock frequency (kHz)
9'hF	LANE_PROFILE	RO	[NUM_LANES-1:0] – Mask delineating the transceivers this IP core uses on the device. For example, if the FPGA has 24 lanes on one side of the device and the IP core uses the bottom eight transceivers, the mask would be 24'b000000_000000_000011_111111..  This register is not available in IP core variations that target an Intel Arria 10 device.
9'h10	PLL_LOCKED	RO	In Intel Arria 10 devices: [0] – Transmit PLL lock indication.  In other device families: [Number of transceiver blocks-1:0] – Transceiver block transmit PLL n lock indication. One lock indicator per transceiver block. Bits that correspond to unused transceiver block PLLs are forced to 1.
9'h11	FREQ_LOCKED	RO	[NUM_LANES-1:0] – Clock data recovery is frequency locked on the inbound data stream

<sup>(1)</sup> Intel recommends that you use this register only during hardware operation. During simulation, you should not rely on the value in this register, because the amount of simulation time required for the IP core to provide consistent values in the REF\_KHZ, RX\_KHZ, and TX\_KHZ registers is too long.

Offset	Name	R/W	Description
9'h12	LOOPBACK	RW	[NUM_LANES-1:0] – For each lane, write a 1 to activate internal TX to RX serial loopback mode, or write a 0 to disable the loopback for normal operation.
9'h13	RESET	RW	<p>Bit 9 : 1 = Force lock to data mode</p> <p>Bit 8 : 1 = Force lock to reference mode</p> <p>Bit 7 : 1 = Synchronously clear the TX-side error counters and sticky flags</p> <p>Bit 6 : 1 = Synchronously clear the RX-side error counters and sticky flags</p> <p>Bit 5 : 1 = Program load mode: perform a sequence of DMA reads. Currently the IP core supports only the value of 1'b0, indicating a processor controls the read operations.</p> <p>Bit 4 : 1 = Ignore the RX analog reset</p> <p>Bit 3 : 1 = Reset the soft microcontroller</p> <p>Bit 2 : 1 = Reset the transmitter and the receiver</p> <p>Bit 1 : 1 = Reset the receiver</p> <p>Bit 0 : 1 = Ignore RX digital resets</p> <p>The normal operating state for this register is all zeroes, to allow automatic reset control. These bits are intended primarily for hardware debugging use. Bit 2 is a good general purpose soft reset. Bits 6 and 7 are convenient for monitoring long stretches of error-free operation.</p>
9'h20	ALIGN	RO	<p>Bit 12 : TX lanes are aligned</p> <p>Bit 0 : RX lanes are aligned.</p>
9'h21	WORD_LOCK	RO	[NUM_LANES-1:0] – Word (block) boundaries have been identified in the RX stream.
9'h22	SYNC_LOCK	RO	[NUM_LANES-1:0] – Metaframe synchronization has been achieved.
9'h23	CRC0	RO	<p>4 bit counters indicating CRC errors in lanes 7,6,5,4,3,2,1,0.</p> <p>These saturate at F, and you clear them by setting bit 6 in the RESET register.</p>
9'h24	CRC1	RO	<p>4 bit counters indicating CRC errors in lanes 15,14,13,12,11,10,9,8.</p> <p>These will saturate at F, and you clear them by setting bit 6 in the RESET register.</p>

Offset	Name	R/W	Description
9'h25	CRC2	RO	4 bit counters indicating CRC errors in lanes 23,22,21,20,19,18,17,16.  These will saturate at F, and you clear them by setting bit 6 in the RESET register.
9'h27	SH_ERR	RO	[NUM_LANES-1:0] – Sticky flag indicating a sync header (framing bit) error has occurred in the corresponding RX lane since this bit was last cleared through the RESET register.
9'h28	RX_LOA	RO	Bit [0] – Sticky flag indicating loss of RX side lane-to-lane alignment since this bit was last cleared through the RESET register. Typically, the IP core asserts this bit in case of a catastrophic problem such as one or more lanes going down.
9'h29	TX_LOA	RO	Bit [0] – Sticky flag indicating loss of TX side lane to lane alignment since this bit was last cleared through the RESET register. Typically, the IP core asserts this bit in case of a TX FIFO underflow / overflow caused by a significant deviation from the expected data flow rate through the TX PCS.
9'h30	PCS_6SEL	RO	Transceiver block selection for PCS test bus. (Factory use only).
9'h31	PCS_LNSEL	RO	Lane selection within transceiver block for PCS test bus. (Factory use only).
9'h32	PCS_TB	RO	PCS test bus. (Factory use only).
9'h33	Reserved		
9'h34	RX_PRBS_DONE	RO	[NUM_LANES-1:0] – Indicates whether enough bits have been received on the corresponding RX lane for one complete pass through the PRBS polynomial.
9'h35	RX_PRBS_ERR	RO	[NUM_LANES-1:0] – Sticky flag that indicates whether a PRBS error has occurred on the corresponding RX lane after RX_PRBS_DONE has attained the value of 1.
9'h36	RX_PRBS_COUNT	RO	[7:0] – This eight-bit counter holds the number of words that had PRBS errors across all lanes. Saturates at the value of 0xFF.
9'h37	RX_PRBS_CTRL	RW	Bit [0] – If you set this bit to the value of 1, the IP core clears the RX_PRBS_DONE, RX_PRBS_ERR, and RX_PRBS_COUNT registers. Reset this bit to the value of 0 to capture new PRBS status.

Offset	Name	R/W	Description
9'h38	CRC32_ERR_INJECT	RW	[NUM_LANES-1:0] - When a bit has the value of 1, the IP core injects CRC32 errors on the corresponding TX lane. When it has the value of 0, the IP core does not inject errors on the TX lane. You must maintain each bit at the value of 1 for the duration of a Meta Frame, at least, to ensure that the IP core transmits at least one CRC32 error.

**Related Information**[Avalon Interface Specifications](#)

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Your 50G Interlaken IP core supports the following test features:

**Internal Serial Loopback Mode** on page 7-1

The 50G Interlaken IP core supports an internal TX to RX serial loopback mode.

**External Loopback Mode** on page 7-2

The 50G Interlaken IP core operates correctly in an external loopback configuration.

**PRBS Generation and Validation** on page 7-2

**CRC32 Error Injection** on page 7-7

## Internal Serial Loopback Mode

The 50G Interlaken IP core supports an internal TX to RX serial loopback mode.

To turn on internal serial loopback:

- Reset the IP core by asserting and then deasserting the active low `reset_n` signal.
- After reset completes, set the value of bits [NUM\_LANES-1:0] of the `LOOPBACK` register at offset 0x12 to all ones.

**Note:** Refer to "IP Core Reset" for information about the required wait period for register access.

- Monitor the RX lanes aligned bit (bit 0) of the `ALIGN` register at offset 0x20 or the `rx_lanes_aligned` output signal. After the RX lanes are aligned, the IP core is in internal serial loopback mode.

Resetting the IP core turns off internal serial loopback. To turn off internal serial loopback:

- Reset the IP core by asserting and then deasserting the active low `reset_n` signal. Resetting the IP core sets the value of bits [NUM\_LANES-1:0] of the `LOOPBACK` register at offset 0x12 to all zeroes.
- Monitor the RX lanes aligned bit (bit 0) of the `ALIGN` register at offset 0x20 or the `rx_lanes_aligned` output signal. After the RX lanes are aligned, the IP core is in normal operational mode.

### Related Information

**IP Core Reset** on page 4-5

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## External Loopback Mode

The 50G Interlaken IP core operates correctly in an external loopback configuration.

To put the IP core in external loopback mode, connect the TX lanes to the RX lanes of the IP core. This mode does not require any special programming of the IP core.

## PRBS Generation and Validation

The 50G Interlaken IP core supports generation and validation of several predetermined pseudo-random binary sequences (PRBS) for Interlaken link testing.

**Table 7-1: PRBS Polynomials Available in the 50G Interlaken IP Core**

Pattern Name	Polynomial	Defined in Interlaken Specification	Available in 50G Interlaken IP Core Variations with Target Device Family	
			Arria V or Stratix V	Intel Arria 10
PRBS7	$x^7 + x^6 + 1$	Yes	Yes	No
PRBS9	$x^9 + x^5 + 1$	No	Yes	Yes
PRBS15	$x^{15} + x^{14} + 1$	No	No	Yes
PRBS23	$x^{23} + x^{18} + 1$	Yes	Yes	Yes
PRBS31	$x^{31} + x^{28} + 1$	Yes	Yes	Yes

For instructions to activate and use the PRBS test feature in your 50G Interlaken IP core IP core, refer to one of the following two topics:

[Setting up PRBS Mode in Arria V and Stratix V Devices](#) on page 7-2

[Setting up PRBS Mode in Intel Arria 10 Devices](#) on page 7-4

### Setting up PRBS Mode in Arria V and Stratix V Devices

To enable the IP core to generate PRBS output, you must program the relevant hard PCS registers to enable the PRBS generator clock, to set the test\_enable bit, and to select the PRBS polynomial. To enable the IP core to receive PRBS input, you must program the relevant hard PCS registers to enable the PRBS receiver clock, to set the test\_enable bit, and to select the expected PRBS polynomial. If you perform your PRBS testing in loopback mode, you must enable the IP core to both generate and receive PRBS sequences.

This section describes the register values you must program. For instructions to program the registers that activate the PRBS test feature in your Arria V or Stratix V 50G Interlaken IP core, refer to the hard PCS register programming instructions in the Native PHY IP Core chapter for your target device family and in the Transceiver Reconfiguration Controller chapter of the *Intel Transceiver PHY IP Core User Guide*.

**Table 7-2: Programming the Hard PCS Registers in Arria V and Stratix V Devices**

To turn on the PRBS feature in the hard PCS, you must program the following hard PCS registers in the order shown, for each of the TX and RX sides. These registers are not accessible using the 50G Interlaken

IP core Management interface. You must access these registers through the Transceiver Reconfiguration Controller that connects to the IP core.

Ensure you set these register bits using a read-modify-write register access sequence (per register), to avoid modifying the other register fields.

TX	Register Offset	Bits	Meaning	Action
1	0x141	[0]	Invert TX channels	Set this bit to the value of 0 to specify that the outgoing PRBS be inverted, or set this bit to the value of 1 to specify that the outgoing PRBS not be inverted. The default value of this register bit is 0. By default, the outgoing PRBS is inverted.
2	0x135	[10]	Enable PRBS7	Set one of these bits to the value of 1, and the others to the value of 0, to select the TX polynomial.
		[8]	Enable PRBS23	
		[6]	Enable PRBS9	
		[4]	Enable PRBS31	
		[3]	TX test enable	Set this bit to the value of 1 to enable the PRBS pattern generator in the transmitter.
3	0x137	[2]	Enable TX PRBS clock	Set this bit to the value of 1 to enable the TX PRBS clock.
RX	Register Offset	Bits	Meaning	Action
1	0x16D	[2]	Invert RX channels	Set this bit to the value of 0 to specify that the PCS should expect the incoming PRBS to be inverted, or set this bit to the value of 1 to specify that the PCS should not expect the incoming PRBS to be inverted. The default value of this bit is 0. In loopback mode, you should set this bit to match the setting in the PRBS transmitter.
2	0x15E	[14]	Enable PRBS7	Set one of these bits to the value of 1, and the others to the value of 0, to select the expected polynomial.
		[13]	Enable PRBS23	
		[12]	Enable PRBS9	
		[11]	Enable PRBS31	
		[10]	RX test enable	Set this bit to the value of 1 to enable the PRBS pattern verifier in the receiver.
3	0x164	[10]	Enable RX PRBS clock	Set this bit to the value of 1 to enable the RX PRBS clock.

After you activate an IP core that targets an Arria V or Stratix V device to generate PRBS output, it immediately begins transmitting PRBS output on the Interlaken link. After you enable the IP core to receive PRBS input, you can check the receive PRBS status in the 50G Interlaken IP core PRBS status registers (`RX_PRBS_DONE`, `RX_PRBS_ERR`, and `RX_PRBS_COUNT`).

After your testing is complete, you must reset these register bits to their default values to enable normal operation.

#### Related Information

- [50G Interlaken IP Core Register Map](#) on page 6-1  
Describes the PRBS status registers.
- [PRBS Generation and Validation](#) on page 7-2  
Lists the supported PRBS polynomials.
- [Intel Transceiver PHY IP Core User Guide](#)

## Setting up PRBS Mode in Intel Arria 10 Devices

To enable the IP core to generate PRBS output, for each Interlaken lane, you must program the relevant hard PCS registers to enable the PRBS generator clock, to set the test\_enable bit, and to select the PRBS polynomial. To enable the IP core to receive PRBS input, for each Interlaken lane, you must program the relevant hard PCS registers to enable the PRBS receiver clock and to select the expected PRBS polynomial, in addition to some bookkeeping tasks. If you perform your PRBS testing in loopback mode, you must enable the IP core to both generate and receive PRBS sequences. After you set the hard PCS registers for PRBS mode, you must perform a soft reset of the transceiver.

This section describes the register values you must program. For instructions to program the registers that activate the PRBS test feature in your Intel Arria 10 50G Interlaken IP core, refer to the hard PCS register information in the *Intel Arria 10 Transceiver PHY User Guide*. You program the hard PCS registers using the 50G Interlaken IP core Intel Arria 10 transceiver reconfiguration interface.

**Table 7-3: Programming the Hard PCS Registers in Intel Arria 10 Devices**

To turn on the PRBS feature in the hard PCS for IP core variations that target an Intel Arria 10 device, you must program the following hard PCS registers in the order shown, for each of the TX and RX sides. These registers are not accessible using the 50G Interlaken IP core management interface. You must access these registers through the Arria 10 transceiver reconfiguration interface of the 50G Interlaken IP core.

Ensure you set these register bits using a read-modify-write register access sequence (per register), to avoid modifying the other register fields.

TX	Register Offset	Bits	Meaning	Action
1	0x6	[2:0]	TX test enable	Set this field to the value of 3'b100 to enable the PRBS pattern generator in the transmitter.
		[3]	PRBS width select	Set this bit to the value of 0 to specify that the PRBS width is 64 bits.
		[7:6]	Enable TX PRBS clock	Set this field to the value of 2'b01 to enable the TX PRBS clock.

TX	Register Offset	Bits	Meaning	Action
2	0x7	[2]	Invert TX channels	Set this bit to the value of 0 to specify that the outgoing PRBS be inverted, or set this bit to the value of 1 to specify that the outgoing PRBS not be inverted. The default value of this register field is 0. By default, the outgoing PRBS is inverted.
		[5]	Enable PRBS9	
		[6]	Enable PRBS15	
		[7]	Enable PRBS23	
3	0x8	[4]	Enable PRBS31	Set one of these bits to the value of 1, and the others to the value of 0, to select the TX polynomial.
RX	Register Offset	Bits	Meaning	Action
1	0xA	[4]	Invert RX channels	Set this bit to the value of 0 to specify that the PCS should expect the incoming PRBS to be inverted, or set this bit to the value of 1 to specify that the PCS should not expect the incoming PRBS to be inverted. The default value of this bit is 0. In loopback mode, you should set this bit to match the setting in the PRBS transmitter.
		[7]	Enable RX PRBS clock	

RX	Register Offset	Bits	Meaning	Action
2	0xB	[1]	Enable 10G PCS mode	Set this bit to the value of 1 to specify the PCS is in 10G PCS mode.
		[3:2]	Verifier counter threshold	Set this field to the value your design requires to ensure adequate lead time before the PRBS checker begins counting PRBS errors. The field value specifies the wait time in number of <code>clk_rx_common</code> clock cycles. A counter begins counting <code>clk_rx_common</code> clock cycles after the soft reset, and triggers the start of PRBS checking when the specified threshold is reached. This field has the following valid values: <ul style="list-style-type: none"> <li>2'b00—Specifies the counter threshold (the wait time) is 127.</li> <li>2'b01—Specifies the counter threshold is 255.</li> <li>2'b10—Specifies the counter threshold is 511.</li> <li>2'b11—Specifies the counter threshold is 1023.</li> </ul>
		[5]	Enable PRBS9	Set one of these bits to the value of 1, and the others to the value of 0, to select the expected polynomial.
		[6]	Enable PRBS15	
		[7]	Enable PRBS23	
3	0xC	[0]	Enable PRBS31	Set this bit to the value of 1 to confirm the PCS is in 10G mode.
		[1]	Confirm 10G PCS mode	
		[3]	PRBS width select	
4	0x13F	[3:0]	RX Deserializer width select	Set this field to the value of 4'b1110 to specify that the data width after deserialization is 64 bits.

After you enable the IP core to generate or receive PRBS output, by setting the relevant register field values for each Interlaken lane, you must perform a soft reset of the transceiver transmitters and receivers. To perform a soft reset of the transceiver transmitters and receivers, on the 50G Interlaken IP core management interface, program bit [2] of the 50G Interlaken IP core `RESET` register at offset 0x13 with the value of 1. On the following `mm_clk` cycle, or later, program the bit 0x13[2] with the value of 0 to clear the reset. After you reset the transceivers and subsequently clear the reset bit, the IP core immediately begins transmitting PRBS output on the Interlaken link. You can check the receive PRBS status in the 50G Interlaken IP core PRBS status registers (`RX_PRBS_DONE`, `RX_PRBS_ERR`, and `RX_PRBS_COUNT`).

After your testing is complete, you must reset these register bits to their default values and perform the soft reset to enable normal operation.

### Related Information

- [50G Interlaken IP Core Register Map](#) on page 6-1  
Describes the PRBS status registers and the soft reset register.
- [Intel Arria 10 Transceiver Reconfiguration Interface Signals](#) on page 5-15  
Describes the interface to program the Arria 10 hard PCS registers, including the information you need to address the registers for each individual lane.
- [50G Interlaken IP Core Management Interface](#) on page 5-12  
Describes the interface to program the 50G Interlaken IP core registers, including the RESET register.
- [PRBS Generation and Validation](#) on page 7-2  
Lists the supported PRBS polynomials.
- [Intel Arria 10 Transceiver PHY User Guide](#)  
Information about the Intel Arria 10 transceiver reconfiguration interface.
- [Intel Arria 10 Transceiver Registers](#)  
Information about the Intel Arria 10 transceiver registers.

## CRC32 Error Injection

The 50G Interlaken IP core supports the injection of CRC32 errors on the Interlaken link for validation of the Interlaken link partner's error handling, and for validation of this IP core's error handling in a loopback configuration. Variations that target an Arria V or Stratix V device require that you first enable the feature in the hard PCS; variations that target an Intel Arria 10 device do not require this step.

To enable the CRC32 error injection feature in your 50G Interlaken IP core that targets an Arria V or Stratix V device, set the value of bit [15] of the hard PCS register at offset 0x138 (offset 0xC from the hard PCS base address of 0x12C) to the value of 1. Ensure you set the register bit using a read-modify-write register access sequence, to avoid modifying the other register fields. This step is not necessary in 50G Interlaken IP core devices that target an Intel Arria 10 device, because CRC32 error injection is enabled by default in these variations.

For instructions to program the hard PCS registers in Arria V and Stratix V devices, refer to the Native PHY IP Core chapter for your target device family and to the Transceiver Reconfiguration Controller chapter of the *Intel Transceiver PHY IP Core User Guide*.

After you enable the IP core to inject CRC32 errors in the output to the Interlaken link, you can turn on the feature using the 50G Interlaken IP core CRC32\_ERR\_INJECT register. You must maintain each register bit at the value of 1 for the duration of a Meta Frame, at least, to ensure that the IP core transmits at least one CRC32 error on the corresponding lane.

After your testing is complete, in Arria V and Stratix V devices, you must reset the hard PCS register bit to its default value of zero to enable normal operation.

The 50G Interlaken IP core CRC32 error injection feature does not keep a count of the errors injected.

### Related Information

- [50G Interlaken IP Core Register Map](#) on page 6-1  
Describes the CRC32\_ERR\_INJECT register.
- [Intel Transceiver PHY IP Core User Guide](#)

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Advanced users can further customize the 50G Interlaken IP core by modifying hidden parameters that are not displayed in the 50G Interlaken parameter editor. These parameters can only be modified in the Verilog RTL instantiation in the generated `ilk_core_50g.sv` file and the instantiation of the 50G Interlaken IP core in the top level design file.

The following topics describe the hidden parameters and tell you how to modify their values.

[Hidden Parameters](#) on page 8-1

[Modifying Hidden Parameter Values](#) on page 8-4

## Hidden Parameters

The advanced parameters affect the behavior of the 50G Interlaken IP core.

**Note:** Intel recommends that you do not modify any RTL parameters that are not listed here. Some undocumented modifications might overwrite settings you specify in the parameter editor.

To customize your 50G Interlaken IP core, you can modify parameters to specify the following properties:

[Required User Clock Frequency](#) on page 8-1

[Counter Reset Bits](#) on page 8-2

[Include Temp Sense](#) on page 8-2

[RXFIFO Address Width](#) on page 8-2

[SWAP\\_TX\\_LANES and SWAP\\_RX\\_LANES \(Data Word Lane Swapping\)](#) on page 8-2

[Use ATX or CMU PLL](#) on page 8-4

[Lane Profile](#) on page 8-4

## Required User Clock Frequency

The `TX_USR_CLK_MHZ` parameter specifies the expected frequency of the input clocks `tx_usr_clk` and `rx_usr_clk`.

The default value of this parameter is 250 MHz. The range of allowed values is 200 MHz to 300 MHz. You must drive the two input clocks at the frequency specified by this parameter.

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## Counter Reset Bits

The **Counter Reset Bits** parameter (CNTR\_BITS) specifies the counter configuration for the IP core internal reset sequence.

This parameter is not available in IP core variations that target an Intel Arria 10 device. In Intel Arria 10 variations, the size of the reset counters in the internal reset controller is set when the IP core is generated.

For simulation, set this parameter to the value of 6. For hardware testing, set this parameter to the value of 20.

The default value of this parameter is 20.

### Related Information

[Modifying Hidden Parameter Values](#) on page 8-4

## Include Temp Sense

The **Include Temp Sense** parameter specifies whether the IP core includes logic to sense the device's case temperature. If the value is set to **1**, the IP core is configured with internal temperature sensing. If the value is set to **0**, this logic is synthesized away.

This parameter is not available in IP core variations that target an Intel Arria 10 device.

The default value of this parameter is 1.

### Related Information

[Modifying Hidden Parameter Values](#) on page 8-4

## RXFIFO Address Width

The **RXFIFO Address Width** parameter specifies the number of bits in the address (offset) of an entry in the RX Reassembly FIFO. The number of bits is  $\log_2$  of the depth of this FIFO. Each RX Reassembly FIFO entry is a 64-bit word.

The default value for the **RXFIFO Address Width** parameter is 12, specifying this FIFO can hold  $2^{12}$  (==4K) 64-bit words. Adjusting this parameter may affect your ability to close timing for your design. However, you can adjust this parameter subject to the successful closure of the timing.

### Related Information

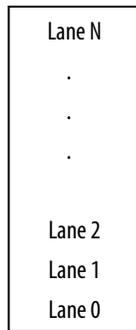
[Modifying Hidden Parameter Values](#) on page 8-4

## SWAP\_TX\_LANES and SWAP\_RX\_LANES (Data Word Lane Swapping)

The 50G Interlaken IP core supports a lane reversal feature (lane swapping). Lane swapping parameters determine the order in which blocks are distributed and gathered from the lanes. The 50G Interlaken IP core provides the following two options for the lane order:

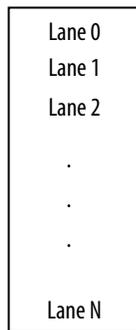
- Straight Lane order. The transmitter sends Interlaken blocks sequentially across the lanes starting with the top lane, ending with Lane 0. The receiver takes in Interlaken blocks starting with the top lane, ending with Lane 0.

**Figure 8-1: Straight Lane Order**



- Swapped Lane order. The transmitter sends Interlaken blocks sequentially across the lanes starting with Lane 0, ending with Lane N. The receiver takes in Interlaken blocks starting with Lane 0, ending with Lane N.

**Figure 8-2: Swapped Lane Order**



Two parameters determine lane order:

SWAP\_TX\_LANES

SWAP\_RX\_LANES

When a parameter is set to **0**, the 50G Interlaken IP core implements the Straight Lane order. When a parameter is set to **1**, the 50G Interlaken IP core implements the Swapped Lane order. The TX and RX parameters are independent and can be set separately.

To conform with the Interlaken specification, the default value of SWAP\_TX\_LANES and SWAP\_RX\_LANES is 1.

**Note:** Running traffic with incompatible lane swapping configuration results in CRC24 errors and incorrect data at the receiver.

**Related Information**

[Modifying Hidden Parameter Values](#) on page 8-4

## Use ATX or CMU PLL

The `USE_ATX` parameter specifies whether the transceivers use the ATX PLL or the CMU PLL. If this parameter has the value of 0, the 50G Interlaken IP core transceivers are configured to use the CMU PLL. If this parameter has the value of 1, the 50G Interlaken IP core transceivers are configured to use the ATX PLL.

This parameter is not available in IP core variations that target an Intel Arria 10 device. These variations do not include a TX PLL. Instead, you must configure an external PLL and connect it to the IP core.

If the transceivers use the ATX PLL, more transceiver block logical channels are available for the eight Interlaken lanes. However, some lower `pll_ref_clk` frequencies are not available with the ATX PLL.

The default value of this parameter is 0, specifying that the IP core transceivers use the CMU PLL and have available the full range of `pll_ref_clk` frequencies documented for this input clock.

### Related Information

[Modifying Hidden Parameter Values](#) on page 8-4

## Lane Profile

The `LANE_PROFILE` parameter specifies the mapping of Interlaken lanes to transceiver logical channels on one side of the device.

This parameter is not available in IP core variations that target an Intel Arria 10 device.

The Interlaken lane order is fixed: Interlaken Lane 0 maps to the lowest numbered logical channel to which a lane is mapped; Interlaken Lane 1 maps to the next lowest numbered logical channel to which a lane is mapped; etc. You determine the side of the device outside the IP core, with pin assignments. Your pin assignments must be consistent with the value of the `LANE_PROFILE` parameter.

The default value of this parameter is `24'b000000_000000_101101_101101`, for use with the CMU PLL. This lane profile specifies that the eight 50G Interlaken IP core Interlaken lanes map to the logical channels in the two bottom transceiver blocks that are consistent with use of the CMU PLL. These logical channels are logical channels 0, 2, 3, 5, 7, 9, 10, and 12.

If you want to use the ATX PLL, you can set this parameter to specify the use of the full bottom transceiver block and two channels from the adjacent transceiver block.

### Related Information

- [Transceiver Logical Channel Numbering](#) on page 2-9  
Illustrates the logical channel mapping for the default lane profile.
- [Use ATX or CMU PLL](#) on page 8-4  
Describes the hidden parameter to specify whether the IP core transceivers use the CMU PLL or the ATX PLL.
- [Modifying Hidden Parameter Values](#) on page 8-4

## Modifying Hidden Parameter Values

To modify the value of a hidden parameter, you must edit one or more generated files. Every time you regenerate the 50G Interlaken IP core, the files are overwritten and you must edit them again.

**Table 8-1: Files to Edit to Modify the Value of a Hidden Parameter**

In each entry, the first file controls the RTL parameter value for synthesis, and the second file controls the RTL parameter value for simulation.

Parameter	Intel Arria 10 Variations	Other Variations
CNTR_BITS LANE_PROFILE	—	<instance name>.v
RXFIFO_ADDR_WIDTH	<instance name>/synth/ <instance name>.v  <instance name>/sim/ <instance name>.v	<instance name>_ sim/<instance name> .v
TX_USR_CLK_MHZ SWAP_TX_LANES SWAP_RX_LANES	<instance name>/ilk_core_ 50g_<version>/synth/ilk_ core_50g.sv  <instance name>/ilk_core_ 50g_<version>/sim/ilk_ core_50g.sv	<instance name>/ilk_core_50g.sv <instance name>_sim/ilk_core_50g.sv
INCLUDE_TEMP_SENSE USE_ATX	—	

# Out-of-Band Flow Control in the 50G Interlaken IP core

# 9

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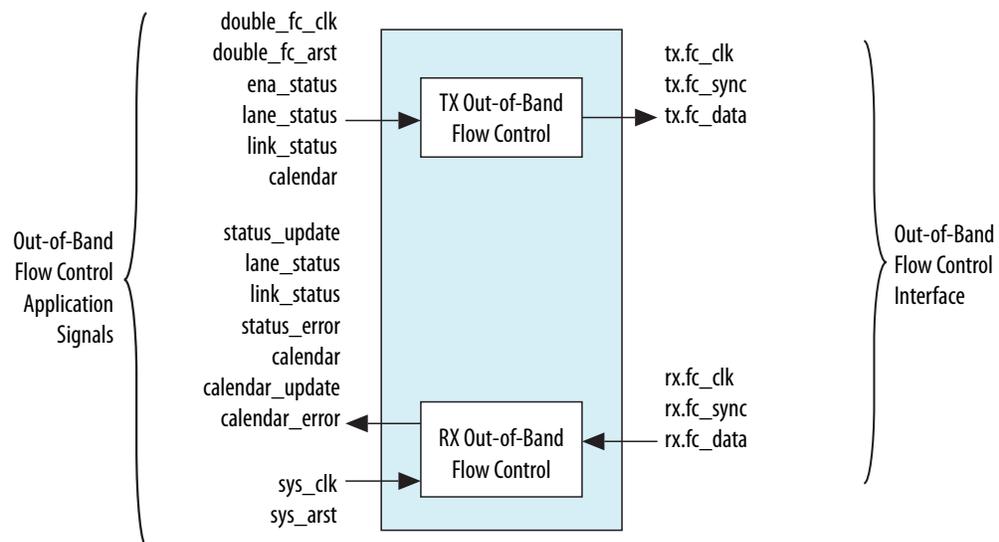


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The 50G Interlaken IP core includes logic to provide the out-of-band flow control functionality described in the *Interlaken Protocol Specification, Revision 1.2*, Section 5.3.4.2. This optional feature is intended for applications that require transmission rate control.

**Figure 9-1: Out-of-Band Flow Control Block Interface**

This figure lists the signals on the four interfaces of the out-of-band flow control block.



The out-of-band flow control block is provided as two separate modules that can be stitched to the 50G Interlaken IP core and user logic. You can optionally instantiate these blocks in your own custom logic. To enable the use of these out-of-band modules, the signals on the far left side of the figure must be connected to user logic, and the signals on the far right side of the figure should be connected to the complementary flow control blocks of the Interlaken link partner.

When you generate a 50G Interlaken IP core, the Intel Quartus Prime software generates the out-of-band flow control blocks in the following location:

```
<your_ip>/ilk_core_<version>/synth/ilk_oob
```

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You must connect the out-of-band flow control receive and transmit interface signals to device pins.

[Out-of-Band Flow Control Block Clocks](#) on page 9-2

[TX Out-of-Band Flow Control Signals](#) on page 9-3

[RX Out-of-Band Flow Control Signals](#) on page 9-4

#### Related Information

[Interlaken Protocol Specification, Revision 1.2](#)

## Out-of-Band Flow Control Block Clocks

Table 9-1: 50G Interlaken IP core Out-of-Band Flow Control Block Clocks

Clock Name	Interface	Direction	Recommended Frequency (MHz)	Description
RX <code>fc_clk</code>	RX Out-of-band	Input	100	Clocks the incoming out-of-band flow control interface signals described in the Interlaken specification. This clock is received from an upstream TX out-of-band flow control block associated with the Interlaken link partner. The recommended frequency for the RX <code>fc_clk</code> clock is 100 MHz, which is the maximum frequency allowed by the Interlaken specification.
TX <code>fc_clk</code>	TX Out-of-band	Output	100	Clocks the outgoing out-of-band flow control interface signals described in the Interlaken specification. This clock is generated by the out-of-band flow control block and sent to a downstream RX out-of-band flow control block associated with the Interlaken link partner. The frequency of this clock must be half the frequency of the <code>double_fc_clk</code> clock. The recommended frequency for the TX <code>fc_clk</code> clock is 100 MHz, which is the maximum frequency allowed by the Interlaken specification.
<code>sys_clk</code>	RX Application	Input	200	Clocks the outgoing calendar and status information on the application side of the block. The frequency of this clock must be at least double the frequency of the RX input clock <code>fc_clk</code> . Therefore, the recommended frequency for the <code>sys_clk</code> clock is 200 MHz.
<code>double_fc_clk</code>	TX Application	Input	200	Clocks the incoming calendar and status information on the application side of the block. The frequency of this clock must be double the frequency of the TX output clock <code>fc_clk</code> . Therefore, the recommended frequency for the <code>double_fc_clk</code> clock is 200 MHz.

## TX Out-of-Band Flow Control Signals

The transmit out-of-band flow control interface receives calendar and status information, and transmits flow-control clock, data, and sync signals. The TX Out-of-Band Flow Control Interface Signals table describes the transmit out-of-band flow control interface signals specified in the *Interlaken Protocol Specification, Revision 1.2*. The TX Out-of-Band Flow Control Block Signals for Application Use table describes the signals on the application side of the TX out-of-band flow control block.

**Table 9-2: TX Out-of-Band Flow Control Interface Signals**

Signal Name	Direction	Width (Bits)	Description
fc_clk	Output	1	Output reference clock to a downstream out-of-band RX block. Clocks the fc_data and fc_sync signals. You must connect this signal to a device pin.
fc_data	Output	1	Output serial data pin to a downstream out-of-band RX block. You must connect this signal to a device pin.
fc_sync	Output	1	Output sync control pin to a downstream out-of-band RX block. You must connect this signal to a device pin.

**Table 9-3: TX Out-of-Band Flow Control Block Signals for Application Use**

Signal Name	Direction	Width (Bits)	Description
double_fc_clk	Input	1	Reference clock for generating the flow control output clock fc_clk. The frequency of the double_fc_clk clock must be double the intended frequency of the TX fc_clk output clock.
double_fc_arst	Input	1	Asynchronous reset for the out-of-band TX block.
ena_status	Input	1	Enable transmission of the lane status and link status to the downstream out-of-band RX block. If this signal is asserted, the lane and link status information is transmitted on fc_data. If this signal is not asserted, only the calendar information is transmitted on fc_data.
lane_status	Input	Number of Lanes	Lane status to be transmitted to a downstream out-of-band RX block if ena_status is asserted. Width is the number of lanes.
link_status	Input	1	Link status to be transmitted to a downstream out-of-band RX block if ena_status is asserted.
calendar	Input	16	Calendar status to be transmitted to a downstream out-of-band RX block.

## Related Information

[Interlaken Protocol Specification, Revision 1.2](#)

## RX Out-of-Band Flow Control Signals

The receive out-of-band flow control interface receives input flow-control clock, data, and sync signals and sends out calendar and status information. The RX Out-of-Band Flow Control Interface Signals table describes the receive out-of-band flow control interface signals specified in the *Interlaken Protocol Specification, Revision 1.2*. The RX Out-of-Band Flow Control Block Signals for Application Use describes the signals on the application side of the RX out-of-band flow control block.

**Table 9-4: RX Out-of-Band Flow Control Interface Signals**

Signal Name	Direction	Width (Bits)	Description
<code>fc_clk</code>	Input	1	Input reference clock from an upstream out-of-band TX block. This signal clocks the <code>fc_data</code> and <code>fc_sync</code> signals. You must connect this signal to a device pin.
<code>fc_data</code>	Input	1	Input serial data pin from an upstream out-of-band TX block. You must connect this signal to a device pin.
<code>fc_sync</code>	Input	1	Input sync control pin from an upstream out-of-band TX block. You must connect this signal to a device pin.

**Table 9-5: RX Out-of-Band Flow Control Block Signals for Application Use**

Signal Name	Direction	Width (Bits)	Description
<code>sys_clk</code>	Input	1	Reference clock for capturing RX calendar, lane status, and link status. Frequency must be at least double the frequency of the TX <code>fc_clk</code> input clock.
<code>sys_arst</code>	Input	1	Asynchronous reset for the out-of-band RX block.
<code>status_update</code>	Output	1	Indicates a new value without CRC4 errors is present on at least one of <code>lane_status</code> or <code>link_status</code> in the current <code>sys_clk</code> cycle. The value is ready to be read by the application logic.
<code>lane_status</code>	Output	Number of Lanes	Lane status bits received from an upstream out-of-band TX block on <code>fc_data</code> . Width is the number of lanes.
<code>link_status</code>	Output	1	Link status bit received from an upstream out-of-band TX block on <code>fc_data</code> .

Signal Name	Direction	Width (Bits)	Description
status_error	Output	1	Indicates corrupt lane or link status. A new value is present on at least one of <code>lane_status</code> or <code>link_status</code> in the current <code>sys_clk</code> cycle, but the value has at least one CRC4 error.
calendar	Output	16	Calendar bits received from an upstream out-of-band TX block on <code>fc_data</code> .
calendar_update	Output	1	Indicates a new value without CRC4 errors is present on <code>calendar</code> in the current <code>sys_clk</code> cycle. The value is ready to be read by the application logic.
calendar_error	Output	1	Indicates corrupt calendar bits. A new value is present <code>calendar</code> in the current <code>sys_clk</code> cycle, but the value has at least one CRC4 error.

**Related Information**[Interlaken Protocol Specification, Revision 1.2](#)

# Performance and Fmax Requirements for 40G Ethernet Traffic



2019.03.15

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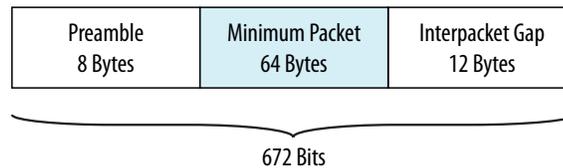
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To achieve 40G Ethernet line rates through the application interface of your 50G Interlaken IP core, you must run the transmit side and receiver side user interface clocks `tx_usr_clk` and `rx_usr_clk` at a minimum frequency of 200 MHz.

The following discussion describes the packet rate calculation that supports this requirement.

## Figure A-1: Interlaken Ethernet Packet

To transmit a minimum size (64-byte) Ethernet packet, the Interlaken link transmitter must send 672 bits of data.



To support an Ethernet line rate of 40Gb/s, the Interlaken link must process 400 bits in 10ns. The following calculation derives the required clock frequency.

$$40 \times 1,000,000,000 \text{ bits/sec} \div 672 = 59.5 \text{ million packets/sec} \\ \approx 60 \text{ million packets/sec}$$

This packet rate requires that the user interface handle one packet per two cycles if the operating clock runs at 200 MHz.

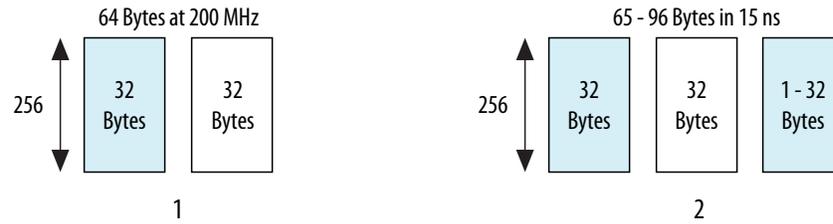
The following figures explain the derivation of the minimum frequency requirements.

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Figure A-2: Packet Processing Requirements



A 65-byte packet comprises  $(65 + 20) \times 8 = 680$  bits. Therefore, for traffic that consists mainly of 65-byte packets, the most inefficient traffic possible, the user interface must handle:

$40 \times 1,000,000,000 \text{ bits/sec} \div 680 = 58.8 \text{ Million packets/sec}$ , or one packet every 17 ns.

Case 2 in the figure shows that the user interface requires three cycles to process each 65-byte packet. At 200 MHz, three cycles take 15 ns, which is a sufficiently small amount of time.

The same calculations applied to lower frequencies yield an average time per packet that is not sufficiently short. Therefore, 200 MHz is the recommended frequency for the two user data transfer interface clocks in your 50G Interlaken IP core.

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This section provides additional information about the document and Intel.

## 50G Interlaken IP core User Guide Archives

If an IP core version is not listed, the user guide for the previous IP core version applies.

IP Core Version	User Guide
15.1	<a href="#">50G Interlaken IP core User Guide 15.1</a>
15.0	<a href="#">50G Interlaken IP core User Guide 15.0</a>
14.1	<a href="#">50G Interlaken IP core User Guide 14.1</a>

## Document Revision History for 100G Interlaken User Guide

Table B-1: 50G Interlaken MegaCore Function User Guide Revision History

Date	ACDS Version	Changes Made
2019.03.15	16.0	Clarified the file location of the out-of-band flow control blocks in section <i>Out-of-Band Flow Control in the 50G Interlaken MegaCore Function</i> .
2018.03.05	16.0	Corrected bit range of <code>reconfig_address</code> signal in <i>Arria 10 Transceiver Reconfiguration Interface Signals</i> section.
2016.05.02	16.0	<ul style="list-style-type: none"> <li>Added a new topic titled <i>Creating a SignalTap II Debug File to Match Your Design Hierarchy</i>.</li> <li>Removed callouts to <code>set_global_assignment -name DISABLE_EMBEDDED_TIMING_CONSTRAINT ON</code>.</li> <li>Removed the chapter <i>Arria 10 Hardware Example Design and 50G Interlaken IP Core Testbench</i>, instead refer to the <a href="#">50G Interlaken Example Design User Guide</a>.</li> </ul>

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Date	ACDS Version	Changes Made
2015.11.02	15.1	<ul style="list-style-type: none"> <li>• Updated for new Quartus Prime software v15.1 release.</li> <li>• Added new <b>Enable Native XCVR PHY ADME</b> parameter for Arria 10 variations.</li> <li>• Updated with change in process to generate legacy testbench.</li> <li>• Added new Arria 10 hardware example design.</li> <li>• Updated generated directory structure for non-Arria 10 variations and location of testbench files for all variations.</li> <li>• Corrected descriptions of TX out-of-band flow control interface signals <code>fc_clk</code>, <code>fc_data</code>, and <code>fc_sync</code> to indicate they are intended to connect to an upstream RX out-of-band block rather than a downstream block.</li> <li>• Corrected 50G Interlaken IP Core Transceiver Initialization Sequence figure. Corrected descriptions of use of <code>reset_n</code> signal to indicate user must assert (low) and deassert (raise) the signal to initiate the reset sequence.</li> </ul>
2015.05.04	15.0	<ul style="list-style-type: none"> <li>• Added new <b>TX scrambler seed</b> parameter. Previously this parameter was hidden (<code>SCRAM_CONST</code>) and unavailable for Arria 10 devices. In the IP core version 15.0 and later, you must modify the scrambler seed from the parameter editor.</li> <li>• Improved description of <b>itx_ifc_err</b> output signal.</li> <li>• Improved description of <b>itx_hungry</b> output signal.</li> <li>• Updated filenames for hidden parameter editing to include the filenames for Arria 10 variations.</li> </ul>
2014.12.15	14.1	<ul style="list-style-type: none"> <li>• Updated release-specific information for the software release v14.1, including new resource utilization numbers and new Arria 10 speed grade notation and information. Resource utilization numbers improved by 20% in the v14.0 release.</li> <li>• Updated for new Quartus II IP Catalog, which replaces the MegaWizard Plug-In Manager starting in the Quartus II software v14.0. Changes are located primarily in Getting Started with the 50G Interlaken IP Core chapter. Reordered the chapter to accommodate the new descriptions.</li> <li>• Corrected instructions to connect the external TX PLL to include the <code>tx_cal_busy</code> signal, and added example figure to illustrate the required connections between the IP core and an ATX PLL. Changes are located in Adding the External PLL section. .</li> <li>• Added information about the required wait from reset to successful register access in IP Core Reset section. .</li> <li>• Corrected width of <code>reconfig_waitrequest</code> signal to one bit. This signal has been a single bit in all versions that support Arria 10 devices, starting with the IP core version 13.1 Arria 10 Edition.</li> <li>• Added information about turning on and off loopback mode in two new sections, External Loopback Mode and Internal Serial Loopback Mode, in IP Core Test Features chapter.</li> <li>• Clarified that <b>Counter Reset Bits</b> is the <code>CNTR_BITS</code> advanced parameter, in Counter Reset Bits section.</li> </ul>

Date	ACDS Version	Changes Made
		<ul style="list-style-type: none"> <li>Added new advanced parameter, <code>TX_USR_CLK_MHZ</code>, that specifies the required frequency of the two input clocks <code>tx_usr_clk</code> and <code>rx_usr_clk</code>. Added new section in Advanced Parameter Settings chapter, and clarified required frequencies in 50G Interlaken IP Core Clock Interface Signals section. This advanced parameter is included in the IP core version 14.0 and later.</li> <li>Corrected instructions to modify the <code>USE_ATX</code> advanced parameter by moving the parameter to the correct list in Modifying Hidden Parameter Values section.</li> <li>Clarified that the testbench and example design are generated only if you specify the IP core synthesis and simulation models are in Verilog HDL. The IP core does not support VHDL models, despite the fact that in the IP core v14.0 and later, the parameter editor appears to offer that option.</li> <li>Fixed assorted typos and formatting issues.</li> </ul>
December 2013	13.1 Arria 10 Edition (2013.12.02)	<ul style="list-style-type: none"> <li>Added preliminary support for Arria 10 devices.</li> <li>Documented features of new Arria 10 variations: <ul style="list-style-type: none"> <li>User logic must configure external PLLs.</li> <li>IP core includes reconfiguration controller.</li> <li>IP core includes new Avalon-MM interface to program Arria 10 Native PHY IP core registers.</li> <li>IP core does not support all of the hidden parameters.</li> <li>IP core does not support temperature register and other registers related to unsupported parameters.</li> <li>IP core provides a different process to enable the PRBS and CRC32 error injection testing features in Arria 10 variations.</li> </ul> </li> <li>Corrected recommended simulation value for <b>Meta frame length in words</b> parameter, from 64 (an unsupported value) to 128 (the minimum supported value).</li> </ul>
November 2013	13.1 (2013.11.04)	<ul style="list-style-type: none"> <li>Updated IP core generation instructions to indicate the MegaWizard Plug-In Manager no longer prompts the user to generate or not generate the example design. Instead, the example design is generated in all cases.</li> <li>Provided additional information about <code>TEMP_SENSE</code> register.</li> <li>Corrected typo in width of <code>itx_hungry</code> signal.</li> <li>Modified introduction of resource utilization information to clarify that the numbers do not include the out-of-band flow control block.</li> <li>Added OpenCore Plus feature support in Installation and Licensing section.</li> </ul>
May 2013	13.0	Initial release.