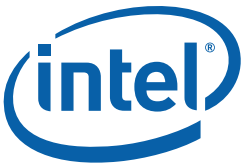

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PCB Stack-up Overview for Intel® Architecture Platforms

Layout and Signal Integrity Considerations

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Executive Summary

Designing a proper stack-up is critical to achieve the lowest cost and highest reliability PCB design. This is getting increasingly more difficult as high speed digital design is getting more complex. A stack-up refers to the arrangement of the copper and insulating layers that make up a Printed Circuit Board (PCB). The stack-up must consider several job functions to ensure success. A collaborative effort between the layout, signal integrity, hardware engineer and manufacturing (fabrication/assembly) vendor is key to ensuring that all parameters are met and incorporated into the stack-up. It is critical that the stack-up is generated and agreed upon by all parties early in the design phase. This ensures that each discipline knows what the final layout will entail and prevents any issues during the critical layout phase of a design. It is strongly recommended to follow the associated Platform Design Guide (PDG) whenever possible.

A collaborative effort between the layout, signal integrity, hardware engineer and manufacturing (fabrication/assembly) vendor is key to ensuring that all parameters are met and incorporated into the stack-up.

There are numerous items to consider in determining the best stack-up for a specific design. These items include the following:

- **PCB Material**
    - Use standard fiberglass epoxy-resin or flame retardant 4 (FR4) material when possible. Alternate materials may be needed

depending on the design; however, there may be a significant cost adder when selecting certain materials.

- Restriction of Hazardous Substances (RoHS) and halogen-free compliance
- Material availability from vendor to vendor may vary limiting selection. This should be evaluated for the life of the design to prevent any future stack-up changes.

- **PCB Layout**
  - Trace width and spacing requirements based on physical limitations of the board/components (breakout areas) along with the recommended impedance requirements
  - Copper weight of signal vs. power/ground layers
- **Signal Integrity**
  - Reference planes
  - Dielectric constant
  - Loss tangent
  - Fiber weave
  - Electrical impact

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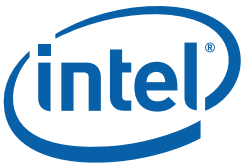


Business Challenge

An increase in the speed and frequency of a design combined with a need to reduce cost has created a challenge in defining an acceptable stack-up to meet the needs of high-speed designs. Often, a low layer count design using standard FR4[1] material is desired. This combination has created numerous challenges such as selecting a material to meet the needs of the interface speeds, reliability, and availability of the vendor along with meeting industry standards such as RoHS or halogen-free requirements.

Proper selection of the material involves working with the vendor to determine what materials are available while avoiding being locked to one particular vendor. One must also consider the location of the vendor as materials vary across geographies. Proper involvement with the signal integrity team early in the design phase is a must as the material properties (frequency, dielectric constant, glass/fiber weave) are a critical part of the simulation activity. The vendor must also be included in the development stages to provide recommendations on the material and to calculate and/or approve the stack-up with respect to dielectric constant/thickness.

Failure to properly research and plan early in the design may lead to issues during the PCB layout phase. As each design may have unique challenges, it is impossible to have one standard checklist available to ensure the success of the design. Issues may range from routing challenges to degraded signal quality which could cause unexpected design failures. In addition to these issues, improper planning and research may lead to a higher cost PCB.

This paper will focus only on designs using through hole via technology. Type 4 PCBs[2] using High Density Interconnects (HDI[2]) will require additional stack up requirements.

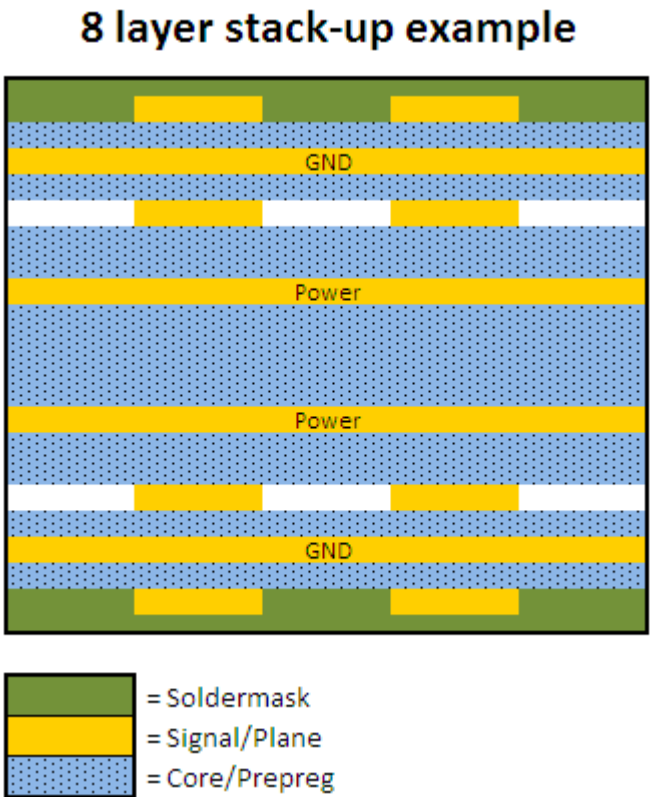
PCB Stack-up Overview

Figure 1 represents an example of an 8-layer stack up to be used only as a reference for this document. As there are numerous stack-up options that are design specific, this example may or may not be applicable in all cases.

[1] FR4 material refers to Flame Retardant 4 which is an insulating material used in most standard PCBs.

[2] Type 4 (aka HDI) PCBs are defined as PCBs utilizing blind, buried or microvia technologies. A blind via is drilled from the surface layer with an end target on an internal layer while a buried via is only drilled on internal layers and does not exist on the surface layers. A microvia is commonly referred to as a via with a hole diameter of 0.005’ or less.

Figure 1. 8-layer stack-up example



This example in Figure 1 is constructed of the following items:

- Two external signal routing layers (microstrip)
- Two internal signal routing layers (stripline)
- Four internal layers which are dedicated for power and GND planes.
- Soldermask on the outer layers
- Core or Prepreg layers between each signal layer. Typically a prepreg layer will be used on the outer layers then it will alternate between prepreg and core material. Core material or cured fiberglass epoxy resin refers to a thin piece of dielectric with copper foil bonded to both sides. Prepreg material or uncured fiberglass epoxy resin will cure during the heating and press stage of fabrication.

Depending on the design, the material selection, dielectric thickness and copper weight will have a significant impact on the trace widths and spacing needed for proper controlled impedance values.

Layout and Signal Integrity considerations

When starting a layout utilizing Intel IA, the layout and signal integrity engineers must discuss the stack-up in detail to define a clear plan. This will need to include:

- **The total number of signal layers needed to route the design.** Care must be taken to properly review the PDG as there are numerous guidelines provided which may restrict routing on certain layers, limit layer transitions or specific requirements for referencing to GND or power planes.
- **Trace width and spacing limitations in the layout.** Typically BGA packages are the most challenging areas of the layout to route and will determine the minimum trace width and spacing that must be used. The designer will need to determine the number of signals that must route between vias in the breakout region. The minimum line width should also be discussed with the signal integrity engineer to determine any negative impacts on the signal quality. The fabrication vendor should also provide a capabilities matrix which will list the standard technologies offered to avoid any additional cost.
- **Controlled impedance requirements for both single-ended and differential structures.** The required values will be defined in the PDG along with a recommended stack-up. These requirements must be mapped to each signal layer to determine the trace width and/or spacing requirements.
- **Power delivery requirements.** Careful planning of the number of power nets along with the required current will assist in determining the number of power planes required. The component placement will also be a significant factor in determining how the planes must be done on each layer. It is recommended that each dedicated power and GND layer are a minimum of 1 oz copper. Increasing the copper weight beyond 1 oz may help reduce the width of the copper plane needed to each device. An increase to the copper weight or Z-axis height will allow a reduction in copper area on the PCB as compared to thinner copper weights. This should be discussed with the manufacturing vendor to determine if any additional cost will incur.

Reference planes

As discussed in this document, proper layout of reference planes is mandatory to ensure a dedicated return path exists. As a general rule, the GND plane is most commonly used as the reference plane. Depending on the

interface, some instances require a power plane reference. This is design specific and will be addressed in the corresponding PDG.

Signals that cross over plane splits or voids will result in an impedance discontinuity and must be avoided.

Figure 2. Signals crossing over a split in the reference plane

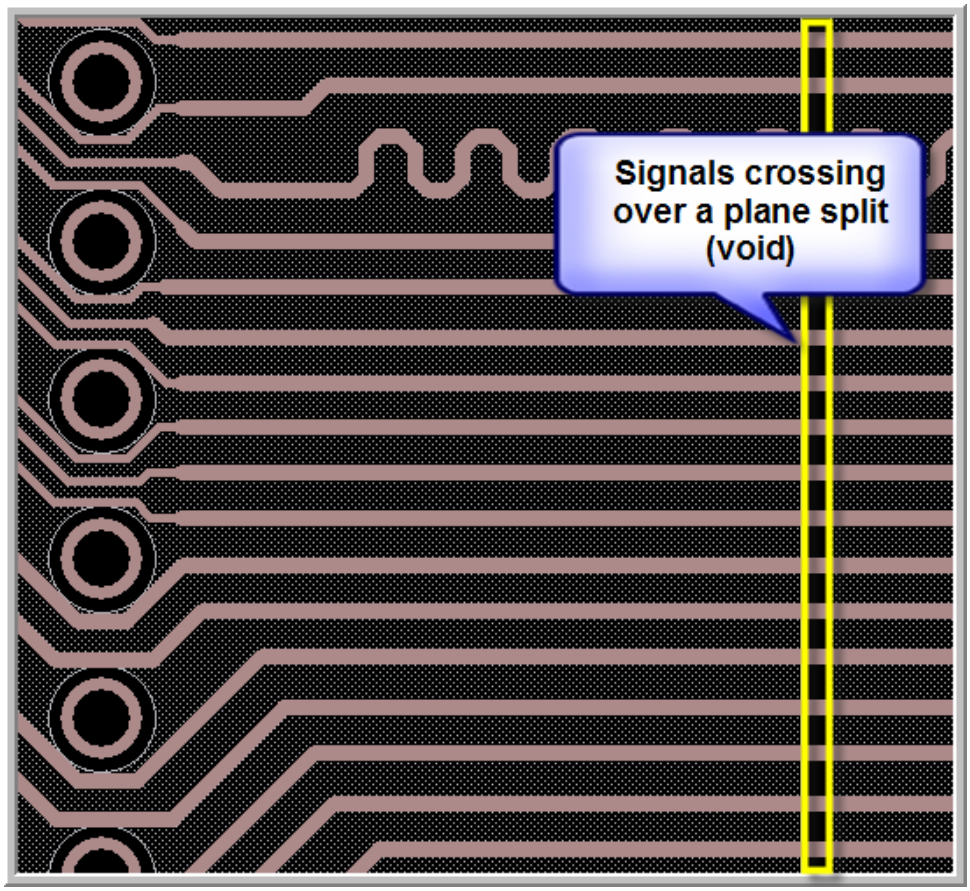
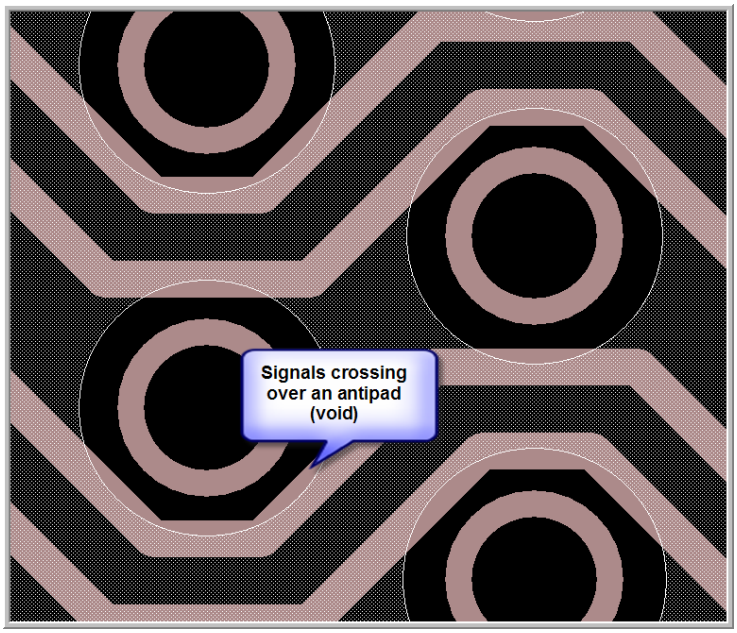


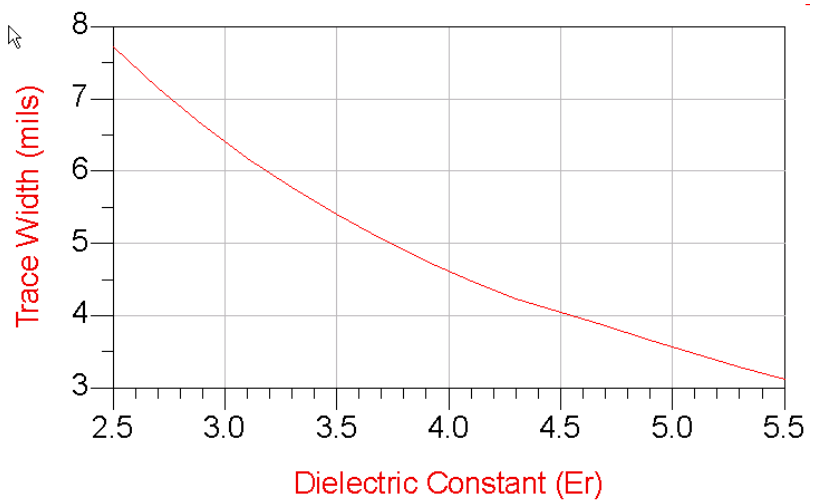
Figure 3. Signals crossing over a void in the reference plane



Dielectric Constant of the PCB Material and the Influence on the Platform

Dielectric properties of the PCB material will affect both impedance and signal loss through the traces. Figure 4 illustrates how to hit a given target impedance, the trace width must decrease if the dielectric constant (Er) increases.

Figure 4. Trend of trace width vs. dielectric constant - Impedance fixed



Let us consider the effect of Er to the Platform Signal Integrity, with an example from a Halogen Free material. FR4 material has an Er of approximately 4.0 at 1GHz. Halogen-free materials have a higher Er, in the range of 4.3 to 5.2, than the standard FR4.

From Figure 4 you can see that a thinner trace is required to achieve the same impedance for a Halogen Free material. Thinner traces give more space for isolation and hence help cross talk. However, the loss increases both because the traces are thinner and Er increases.

The trend on impact of higher Er is increased loss and reduced cross talk.

This can have a different effect on different interfaces. For example, High Speed Differential interfaces are usually limited by loss and hence will suffer if Er increases, but DDR memory interfaces on the other hand are generally limited by cross talk and hence benefit from increased Er.

Figure 5 shows the trend of impedance of a trace when dielectric constant changes for a given trace width.

Figure 5. Trend of impedance vs. Dielectric constant – Trace width fixed

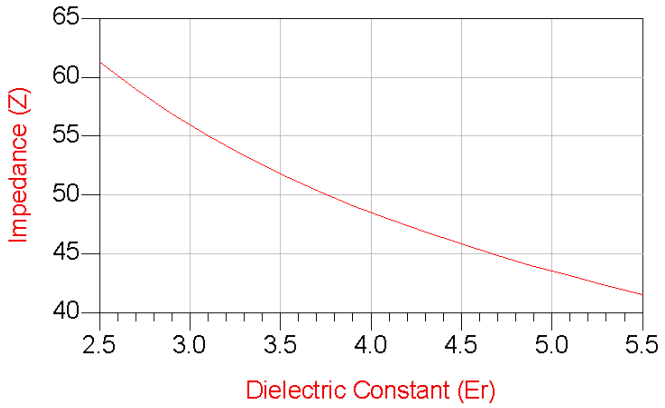


Figure 5 illustrates that for a given trace width, increasing Er will decrease the impedance. If the stack-up is adjusted to get back the impedance, the trend will increase the reference plane height from the signal trace and hence can take more routing space to get the same isolation spacing.

Note: A similar analysis can be done for the opposite case when the dielectric constant decreases.

Loss Tangent of the PCB Material and the Influence on the Platform

Loss tangent (tanD) is a property of the dielectric material, characterizing the signal loss throughout the material. Choose material with lower loss tangent, if possible, if you deal with both longer lengths and higher speed.

Figure 6 shows the trend of signal loss in dB/in for three different frequencies.

Figure 6. Signal Loss vs. Loss Tangent of the Material

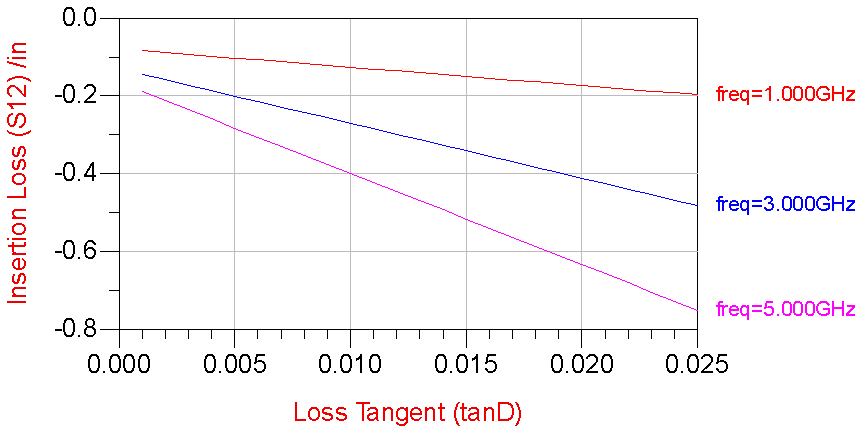
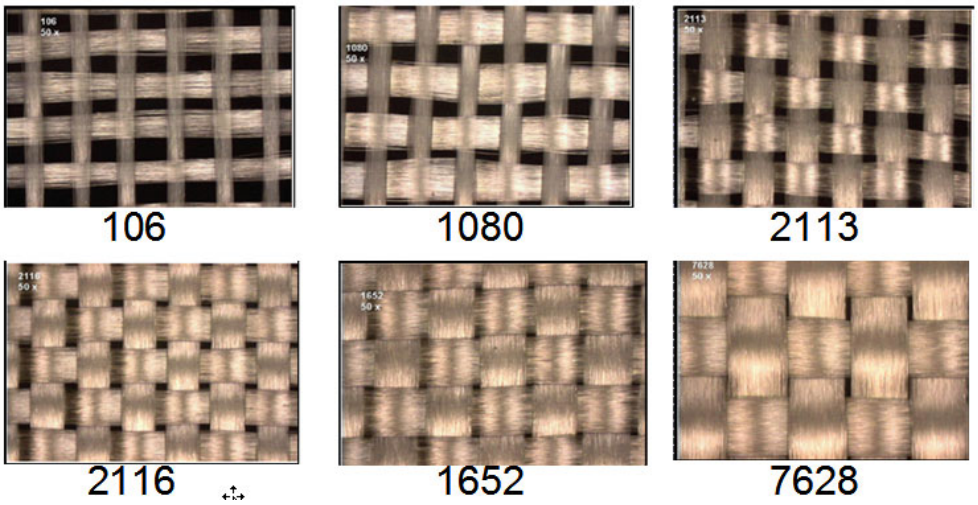


Figure 6 shows the importance of tanD is much less on frequencies below 1GHz, whereas they influence trace loss significantly at higher frequencies.

Fiber Weave

The fiberglass weave pattern in a dielectric material can affect high speed differential interface signals. Figure 7 shows the weave pattern of different dielectric materials.

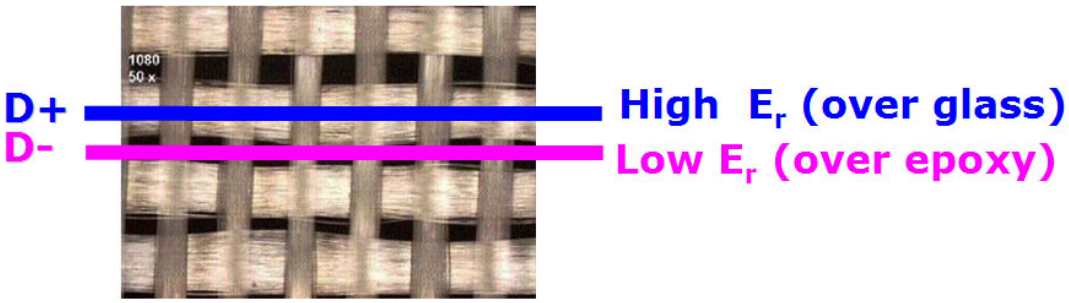
Figure 7. Fiber Weave Patterns for Different PCB Materials



Electrical Impact

The two halves of a differential pair see different effective dielectric constants (and corresponding velocities) due to the difference in Er of the fiberglass weave (Er ~6) and epoxy (Er ~3). Signals travel faster when Er is lower, hence signals routed over a glass bundle travels more slowly due to the higher Er as shown in Figure 8.

Figure 8. Differential traces



The extent of the problem is dependent on bus speed, length of traces, trace geometries (differential pair spacing), weave types used, alignment of traces to weave, etc. Figure 9 gives a comparison quantitative for different speed and length on a typical topology.

Figure 9. Electrical Impact from Fiber Weave

EH reduction Unit: mV

Length	2"	4"	5"	6"	8"	10"	12"	14"	18"
2.5GT	0	0	0	0	0	0	24	47	124
4GT	0	5	30	55	110	160	267		
5GT	0	40	68	71	127	246	305		
6.4GT	0	84	94	115	218	303			
8GT	0	70	100	140	240				

EW reduction Unit: UI

Length	2"	4"	5"	6"	8"	10"	12"	14"	18"
2.5GT	0	0	0	0.01	0.025	0.04	0.07	0.1	0.2
4GT	0	0	0	0	0.056	0.12	0.17		
5GT	0	0	0	0.04	0.1	0.3	0.49		
6.4GT	0	0.02	0.02	0.1	0.3	1			
8GT	0.02	0.01	0.07	0.14	0.79				

Reducing Fiber Weave Effect

If you decide that the effect is a problem at a particular bus frequency and length, you may consider one of these options:

Special Routing: Angled routing within the layout database. A 10° trace is sufficient to accommodate manufacturing variations in the weave pattern.

Image Rotation (panel): The artwork may be rotated at 10° on the panel during fabrication. This option may incur additional cost and should be discussed with the fabricator before starting the layout. Depending on the overall board size, this may not be possible on a standard 18" x 24" panel.

Conclusion

This document outlines numerous items that must be carefully reviewed when determining the proper printed circuit board (PCB) stack-up to use. The best method is to follow your Platform Design Guide (PDG) recommendations whenever possible. If deviations are necessary, this document should be used as an aid to achieving the correct stack-up along with any other requirements that may be specific to your design.

A team consisting of layout, signal integrity, hardware engineers along with the manufacturing vendor should carefully review the material selection and properties, layout limitations, signal integrity drivers, cost, and reliability of the design based on the material and stack-up used. In addition to these items, any deviation from the PDG must be reviewed by experienced individuals to ensure that the design will still meet the requirements provided by Intel.

Early interaction with the teams listed above is key to ensuring that all design parameters are met and avoiding potential issues that may result later in the design phase.

Authors

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Acronyms

PDG	Product Design Guide
IA	Intel Architecture
PCB	Printed Circuit Board
RoHS	Restriction of Hazardous Substances
HDI	High Density Interconnect
BGA	Ball Grid Array
Er	Dielectric Constant
GHz	Gigahertz
HSD	High Speed Design
DDR	Double Data Rate
Z	Impedance
tanD	Loss Tangent
dB	Decibel